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DOCUMENT

SEL Heavy Ion Test Report of Maxim HI-201 Quad SPST CMOS Analog Switch

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1 INTRODUCTION

This study was undertaken in the frame of the Aeolus project to determine the single event latch-up susceptibility of Maxim HI-201 Quad SPST CMOS Analog Switch. The device was monitored for destructive events induced by exposing it to a heavy ion beam at the UCL Heavy ion facility.

2 APPLICABLE DOCUMENTS

AD1: ESCC25100 Single Event Effects Test Method and Guidelines
AD2: H-201 Datasheet, year 1990 version.

3 DEVICES TESTED

Part Type	HI-201
Manufacturer	Maxim
Part Function	Quad SPST CMOS Analog Switch
Technology	CMOS
Date Code	6C1228
Part Marking	MAXIM 7705302EA
Package	CERDIP 16

The parts were mechanically delidded with a scalpel after it had been soldered on the test board.

Figure 1

the part marking on the package top and bottom lid respectively.

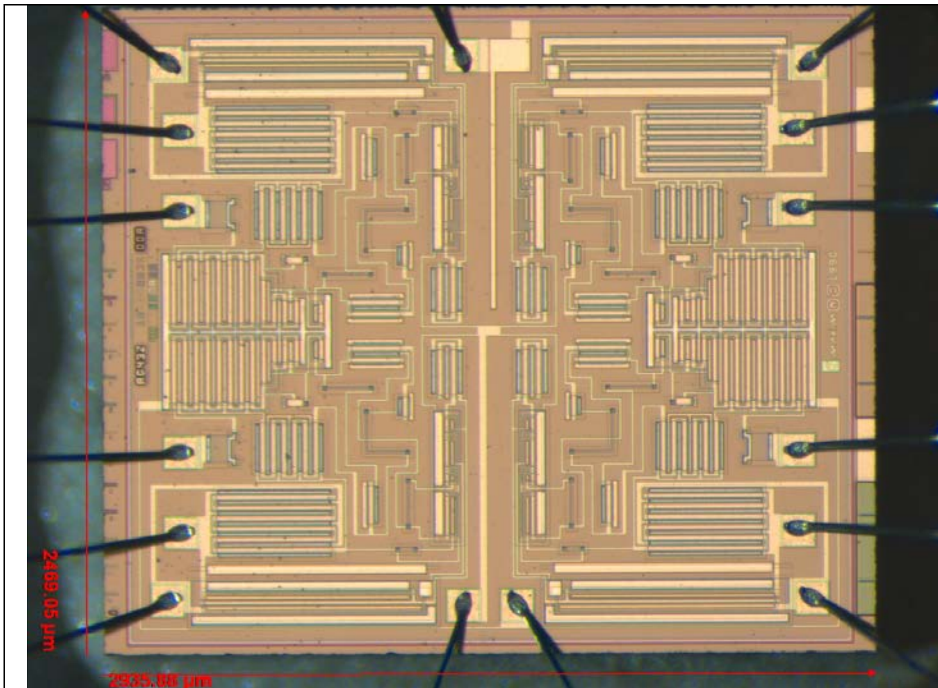


Figure 2

The exposed die after scalpel delid of the package.
The measured die size is about 7.3 mm².

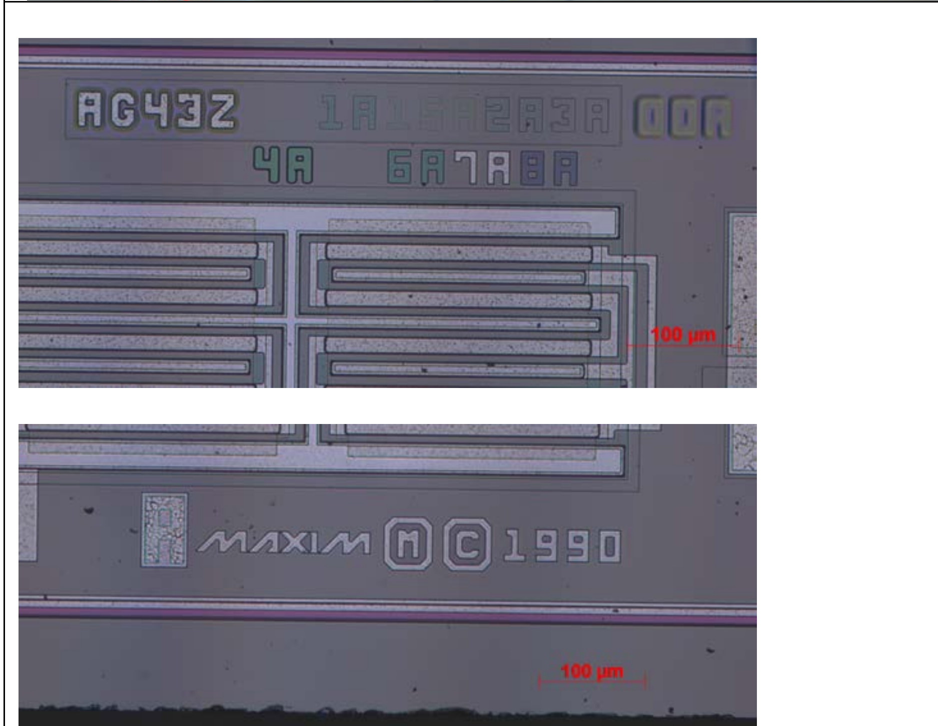


Figure 3

Detail of the die markings

4 TEST FACILITY

Facility: UCL HIF with high LET cocktail., the new high energy Xe beam has been used (Energy = 995MeV, LET = 62.5MeV.cm^2/mg, range = 73.1µm)
Flux: Maximum 1 x 10^4 particles/cm^2/s
Fluence: All tests were run up to a fluence of 1 x 10^7 particles/cm^2

Characteristics of HIF high LET cocktail ions is shown in the Table below.

Ion	Energy (MeV)	LET(Si) (MeV•cm^2/mg)	Range (µm Si)
$^{13}C^{4+}$	131	1.1	292
$^{22}Ne^{7+}$	235	3	216
$^{40}Ar^{12+}$	372	10.2	117
$^{58}Ni^{18+}$	567	20.4	100
$^{83}Kr^{25+}$	756	32.6	92
Xe	995	62.5	73

The following test equipment has been used:

- Keithley 2612B s/n 1285173 (last cal. 25.08.15)
- Guard Latch-up Tester 30463 TRAD
- Yokogawa scope-corder 850
- 34970 Data Acquisition unit with PT- 100 sensor for temperature control.
- E3646E Dual Power Supply.
- E3645 Single Power Supply.

5 TEST CONDITIONS

Test Temperature: DUT was kept at stable temperature greater than 73◦C under vacuum

Bias Conditions: DUT will be biased according to the following conditions:

- V+= +15V, V-=15V (E3646E Dual Power Supply)
- Digital input A1 and A3 to 5V (Keithley 2612B Channel B)
- IN1 , IN2, connected to 15V (E3645 Single Power Supply)
- OUT1, OUT2 connected to GND via a 2 KΩ resistor
- Digital inputs A2 and A4 connected to GND
- IN3, IN4 connected to 2V (Keithley 2612B Channel A)
- OUT3, OUT4 connected to GND via 2 KΩ resistor

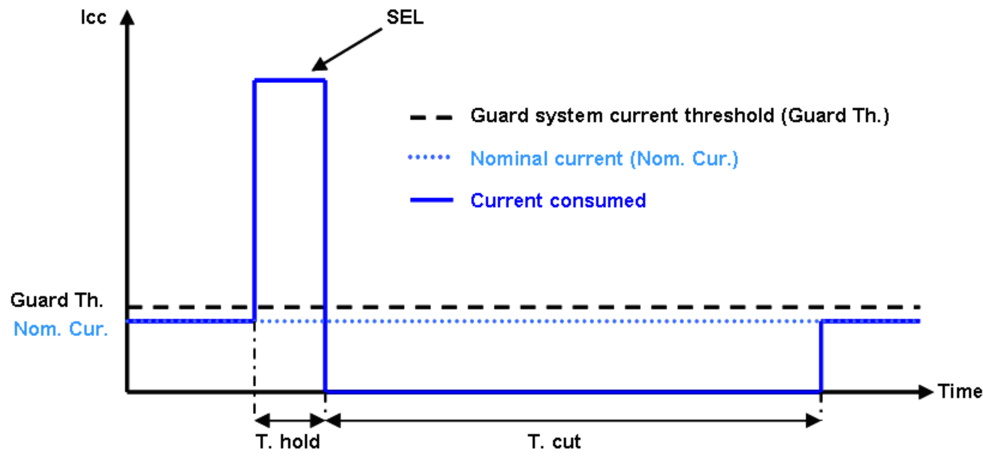
Operating frequency: Static condition.

6 TEST METHOD

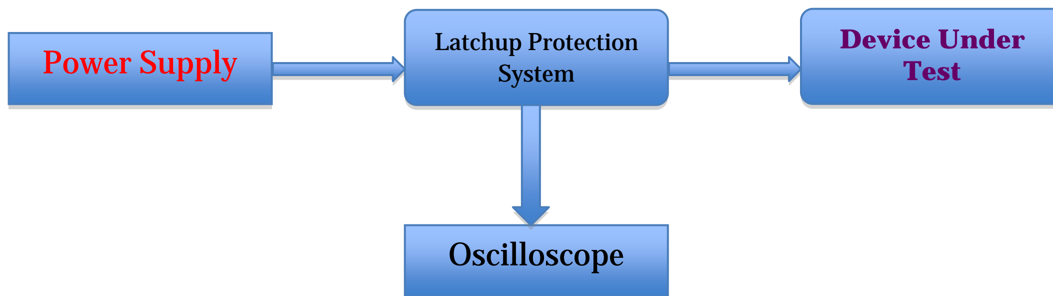
The supplies (power and input) was be applied to the DUT through the GUARD system. The threshold current of the GUARD system was set to 10 mA for the supply and 20 mA for the inputs. If the supply power current or any of the two input currents exceeds the threshold, the GUARD system is triggered. Then, the GUARD system send a trigger command to the oscilloscope, maintains the power supply during a define “time hold” of 1ms, and if the current still exceeds the threshold after time hold, supply is cutoff during a “time cut” of 5 ms. Then the supply is restarted and the event is counted as a SEL. All power supply voltages were protected by GUARD during the test.

V+ = + 15V / I+ = 0.3 mA / I+ threshold = 10 mA
V- = - 15V / I- = 0.3 mA / I- threshold = 10 mA
VIN3 = +15V, Vout3 = -15V / IIn3 = 3 mA / IIN3 threshold = 20 mA
VIN4 = +15V, Vout4 = -15V / IIn4 = 3 mA / IIN4 threshold = 20 mA

The figure below illustrates the latchup detection and protection scheme of the DUT.



A synoptic view of the test bench is given below:



7 TEST BOARD & FINAL TEST SETUP

The test board and related schematics are shown below:

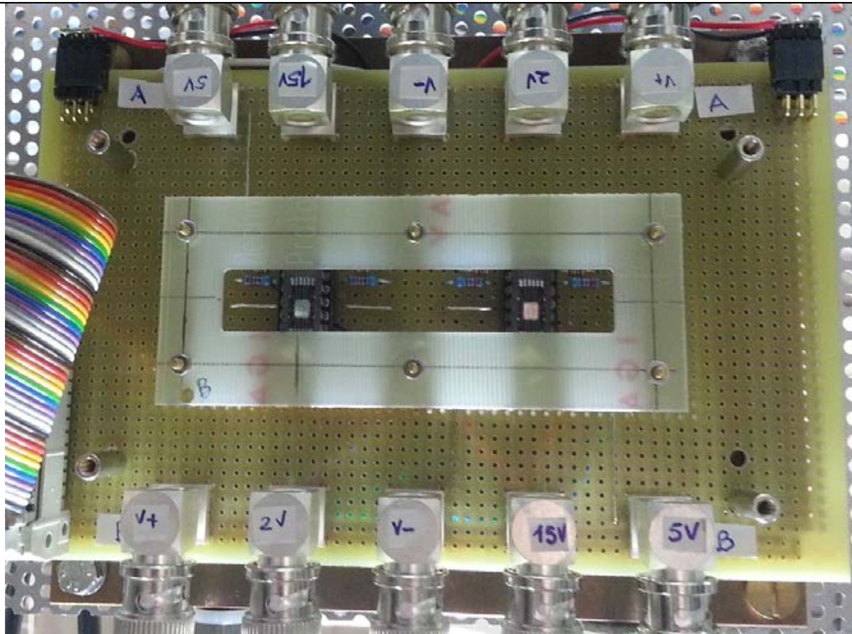


Figure 4. Test board containing two devices under test.

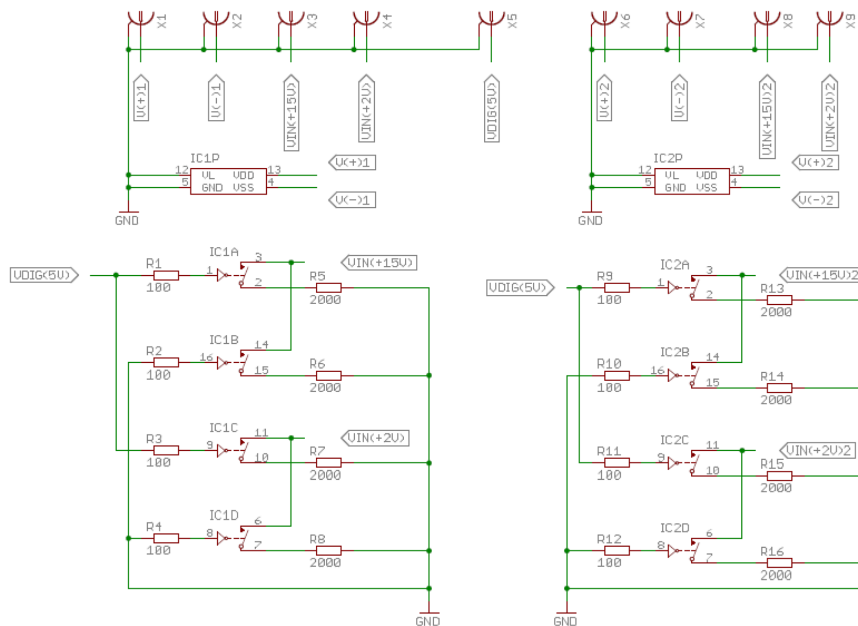


Figure 5. Test board schematics.

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The final test setup setup at UCL used during the test is shown below:

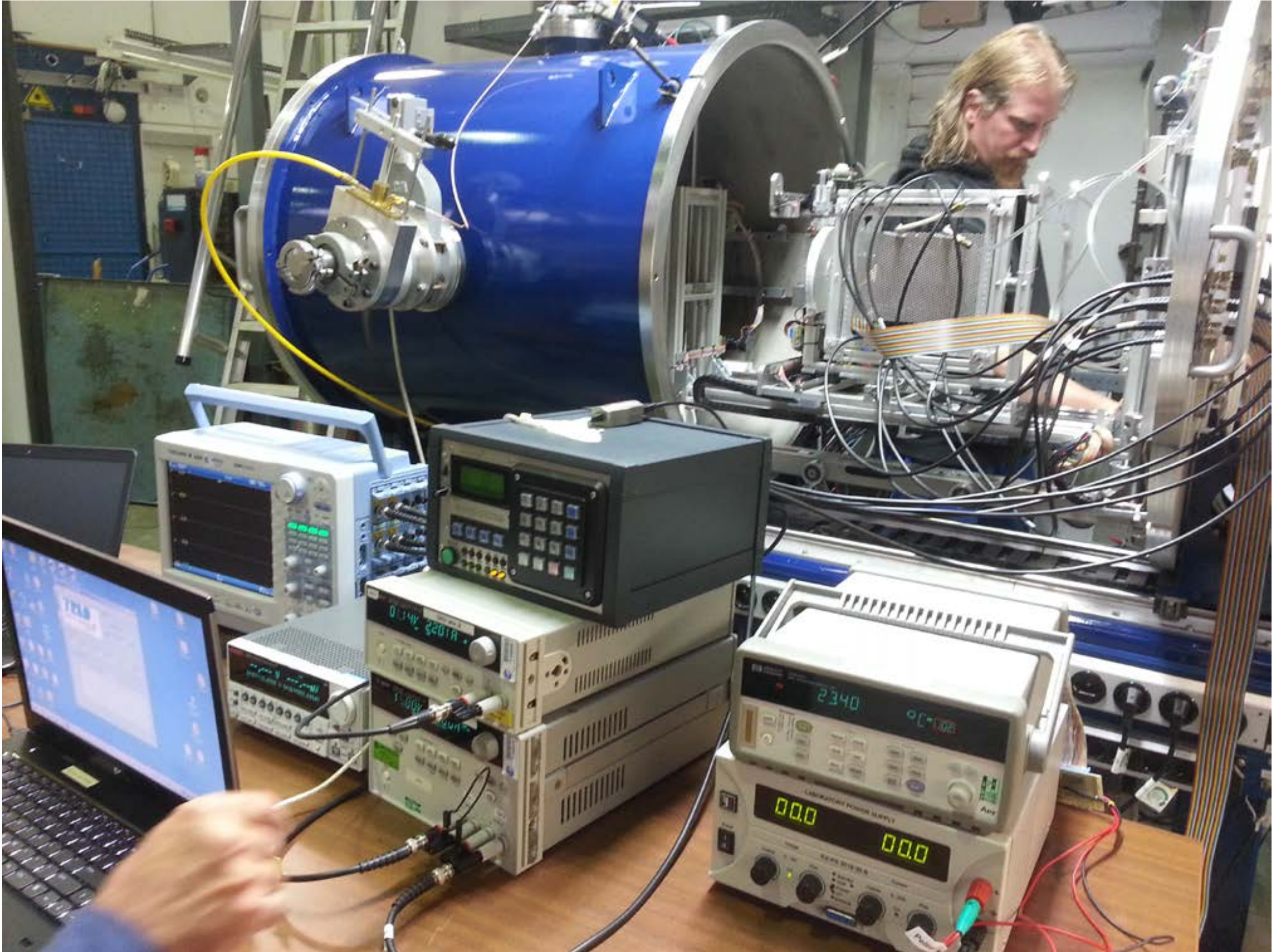

Figure 6. Overview of test setup used at UCL

8 TEST RESULTS

During testing, 4 devices were irradiated with Xenon beam at normal incidence up to a fluence of 1E7/cm². No latch-up occurred during the experiment yielding a threshold LET for latch-up > 62.5MeV.cm²/mg.

9 CONCLUSIONS

The goal of this test was to assess the single event latch-up susceptibility of Maxim HI-201 Quad SPST CMOS Analog Switch. No latch-up event was detected up to an LET of 62.5MeV.cm²/mg, which is compliant with the AEOLUS requirements.

10 APPENDIX

The test sequence for the three tested devices is shown in the table below:

Time	Run	DUT	Ion	Ion range	Energy (MeV)	LET (MeVcm2/mg)	Angle (deg)	LETeff (MeVcm2/mg)	Fluence (#/cm2)	TID (krad)	Vbias1	Isb1	Vbias2	Isb2
	11	part #1 position A (Temp 72C)	Xe	73um	995	62.5	0	62.5	1E7	10.00	**15V**	< 1mA	**- 15V**	< 1mA
16:05	12	part #2 position B (Temp 81C)	Xe	73um	995	62.5	0	62.5	1E7	10.00	**15V**	< 1mA	**- 15V**	< 1mA
16:50	13	part #3 position A (73.5temp C)	Xe	73um	995	62.5	0	62.5	1E7	10.00	**15V**	< 1mA	**- 15V**	< 1mA
17:05	14	part #4 position B (81 temp C)	Xe	73um	995	62.5	0	62.5	1E7	10.00	**15V**	< 1mA	**- 15V**	< 1mA