SINGLE EVENT EFFECTS
TEST REPORT

Test Type:	Heavy Ion
Test facility:	RADEF/JYFL, FINLAND
Test Date:	December 2009
Part Type:	HM5225165BTT-75
Part Description:	256 Mbit SDR-SDRAM
Part Manufacturer:	ELPIDA
ESA reference	ESA_QEC1003S_C
Issue	03
Date	June 17, 2010

ESA COO No2 under Contract No 22327/09/NL/SFe dated 15/10/09

Technical Officer: Fredrik Sturesson

Hirex reference :	HRX/SEE/0287	Issue : 03	Date : June 17, 2010
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RESULTS SUMMARY

Facility RADEF, JYFL, Finland

Test date December 2009

Device description

Part type: HM5225165BTT-75
Description: 256 Mbit SDR-SDRAM
Package: 54-pin TSOP II
Technology: -
Die dimensions: 8011.66 x 14501.46 µm

This test is the follow-up of a test campaign performed at JYFL on October 2009 where only SEL events were monitored. In the present test, 4 fresh samples were prepared by thinning and were found fully functional at ambient and at 85°C during set-up check prior to exposure. As a consequence, monitoring of SEUs and SEFIs was made possible.
As this test was primarily focused on SELs and SEFIs, only Xenon ion was used with a relatively high flux.

Main results is that SEL occurrence with Xenon is confirmed and also the effect of temperature on SEL rate; no SEL events was recorded with Xenon at normal incidence angle at ambient temperature, while rare events was recorded at 50°C and 85°C .

Tilting the device increases SEL rate drastically. The saturation cross-section is more than 1e-4 cm2 at 85°C which is the highest recorded SEL cross-section throughout all test runs.

With tilting angles and the used ion source, having a limited range, the true cross-section cannot be established. With tilting angles the actual LET drops and as die thickness varies along the die area also the actual LET varies over the die. This has a strong impact on the measured cross sections using tilting angles.

The actual LET at normal incidence angle is between 60 and 69 MeV/(mg/cm2) over the full die area for all devices. It still involves some uncertainty, but the cross section data and LET can be considered valid at normal incidence angle.

Previous results from October 2009 showed events of step current increases, which never was observed here. Most likely the processing of SEFIs by power reset of the device has mitigated the current step events.

On two runs performed at a lower flux, it was possible to analyse SEU data, SEU cross-section per bit is about 1.5 E-09 cm^2 for Xenon at normal incidence.

Some stuck bits (leaky cells) were counted and for each sample, stuck bits occurrence increase with the accumulation of the runs.

DOCUMENTATION CHANGE NOTICE

Issue	Date	Page	Change Item	
01	08/01/2010	All	Original issue	
02	19/02/2010	All	As per Esa comments	
03	17/06/2010	All	Final Esa comments	

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1 Introduction

This report presents the results of Heavy Ion test program carried out on ELPIDA 256 Mbit SDR-SDRAM referenced HM5225165BTT-75. This test was primary performed in order to confirm the SEL results achieved in tests performed in October 2009 where the devices under test were not fully functional. The results from October 2009 are reported in RD-2.

The devices were heavy ion tested at RADEF, University of Jyväskylä, Department of Physics, Jyväskylä, Finland 3th December 2009.

This work was performed for ESA under COO No2 under Contract No 22327/09/NL/SFe dated 15/10/09.

2 Applicable and Reference Documents

2.1 Applicable Documents

AD-1. HM5225165B Datasheet reference Elpida E0082H10 1st edition
AD-2. Hirex proposal HRX/PRO/2739 Issue 02, dated June17, 2009

2.2 Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100
RD-2 Singel Event Effects Test report; HM5225165BTT-75, HM5257805BTD-75, (HRX/SEE/0276)

3 DEVICE INFORMATION

3.1 Device description

The HM5225165B is a 256-Mbit Simple Data Rate SDRAM organized as 4,194,304-word x 16-bit x 4 bank. All inputs and outputs are referred to the rising edge of the clock input.

Part Description:	256 Mbit SDR-SDRAM
Package:	54-pin TSOP II
Samples Used:	S/N 1, S/N 516, S/N 525, S/N 526
Top Marking:	5225165BTT75
Die dimensions:	8011.66 x 14501.46 µm

3.2 Sample identification

Eight samples were prepared to test by Hirex Engineering. Three of them were delivered by Astrium; the rest was bought through Oxygen distributor. The tests were performed on three samples from Astrium with a lot datecode stock “0232” and one commercial sample with a lot datecode stock “0423”.

Photo 1 - Top Marking (HM5225165BTT-75)
Astrium Part

Photo 2 - Die Marking (HM5225165BTT-75)

Photo 3 - Top Marking (HM5225165BTT-75)
Commercial Part

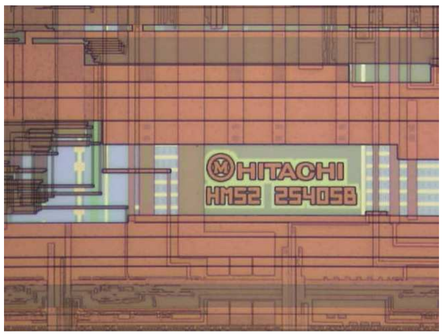


Photo 4 - Die Marking (HM5225165BTT-75)

Figure 1: Device identification

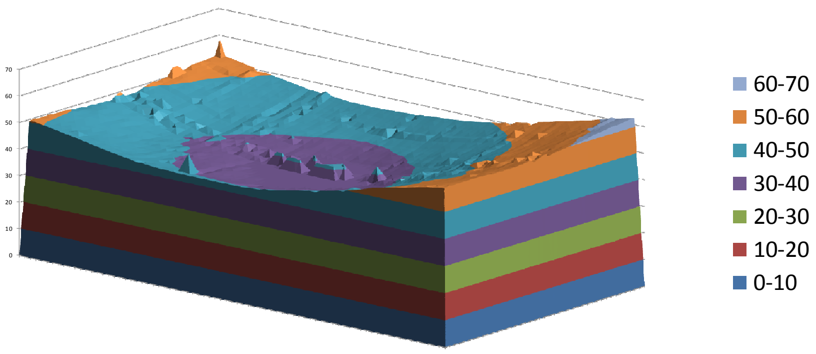
3.3 Sample preparation

The HM5225165B sample consists of one die. It is polished down to a thickness compatible with the penetration depth of the ions. At JYFL, minimum range is 89µm with 1.2 GeV Xenon.
Once the samples are polished down the measurement of their thickness is executed. For this purpose the CHRocodile IT measuring system[1] made by PROSITEC Company is used with 1 µm accuracy. The data obtained from the system is treated with the software made by Hirex Engineering.

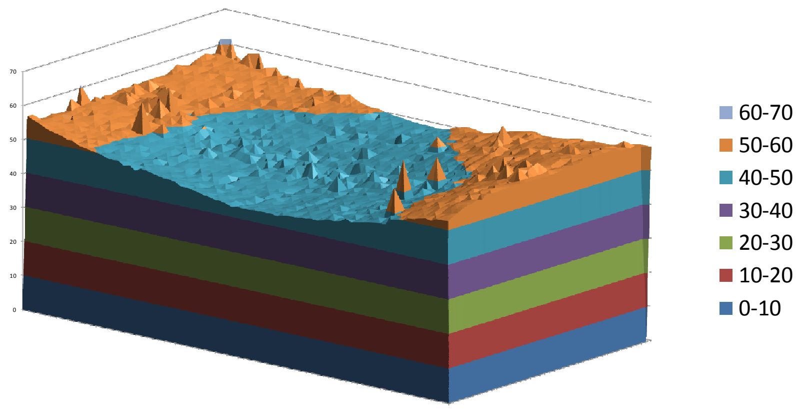
Figure 3 provides the % of die area as a function of die thickness and on the same graph, the LET value as a function of penetration depth is also plotted.

This figure helps for seeing the eventual variation of the LET value computed with SRIM2008[2] over a % of die area for the three samples prepared.

3.4 Thickness of the samples

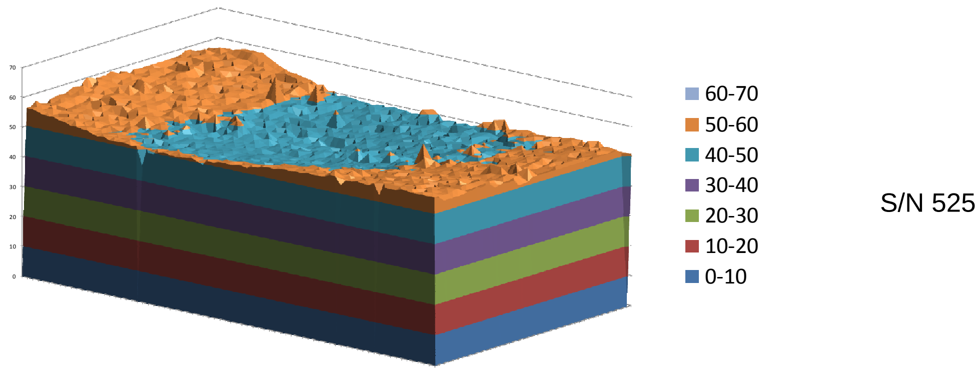


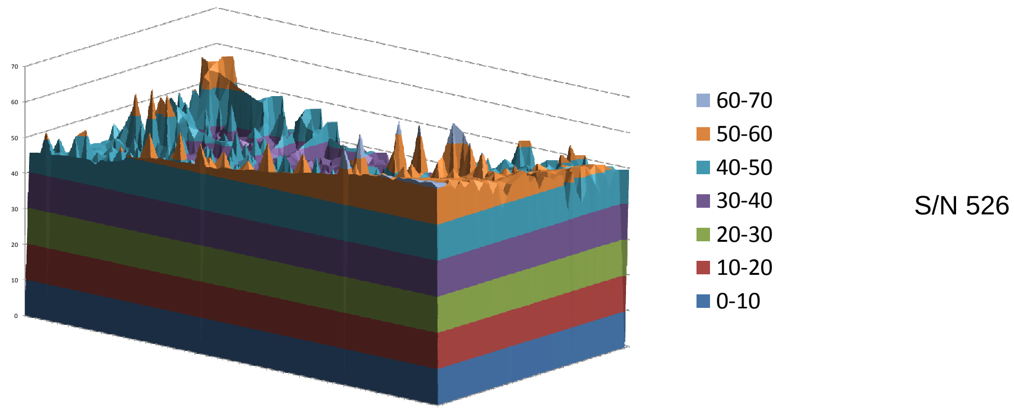
S/N 4



S/N 516

[1] http://www.precitec.com/measuring-technology/contactless-measuring-sensor-chrocodile-it.html
[2] http://www.srim.org/SRIM/SRIMLEGL.htm





X and Y axis units are in mm, Z axis in µm.

Figure 2: Thickness of the devices

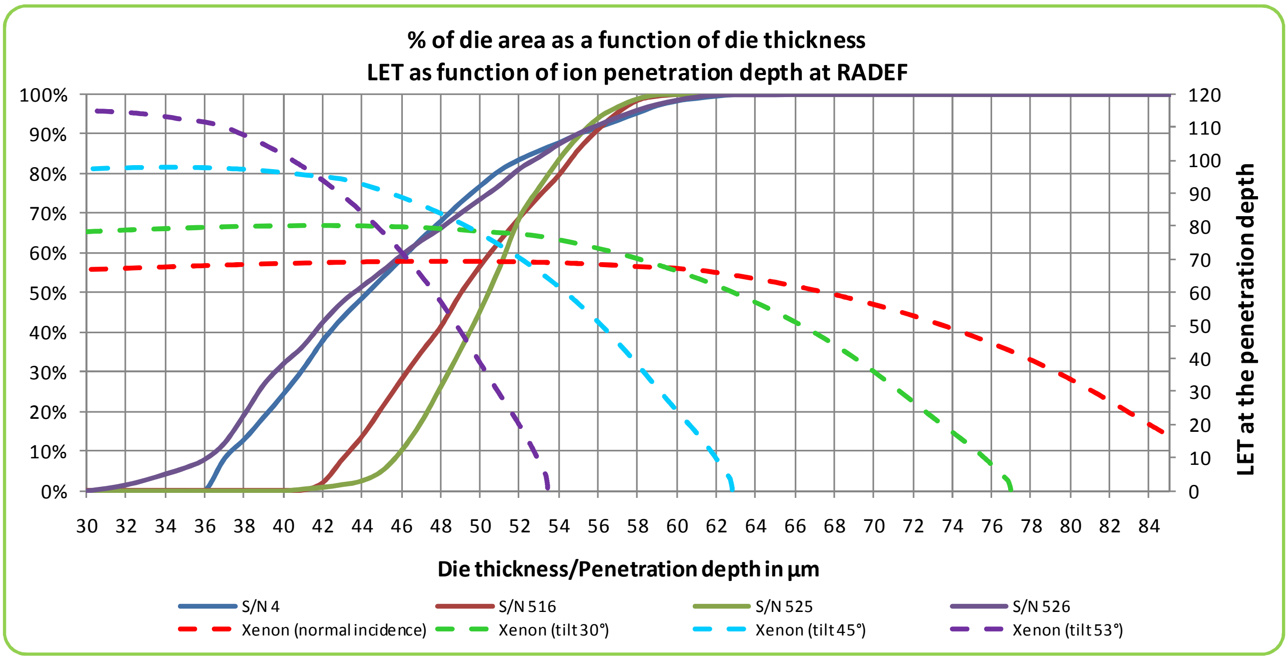


Figure 3 - % of die area as a function of die thickness together with LET values as a function of penetration depth at RADEF

4 Test definition

4.1 Test board

Figure 4 shows the principle of the Heavy Ion test system.

The devices are clocked at 50 MHz with signals generated by a Virtex 5 FPGA (Xilinx). Each memory has a dedicated +3.3V analogue supply with current limit set at 200 mA, which is approximately twice the nominal memory supply current of 100 mA. The supply voltage of the memory can reach +3.6 V.

The Xilinx FPGA is powered from a separate external bench supply.

The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 16 independent channels.

A temperature Control system is used to heat the DUT. Tests are executed at different temperatures.

The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.

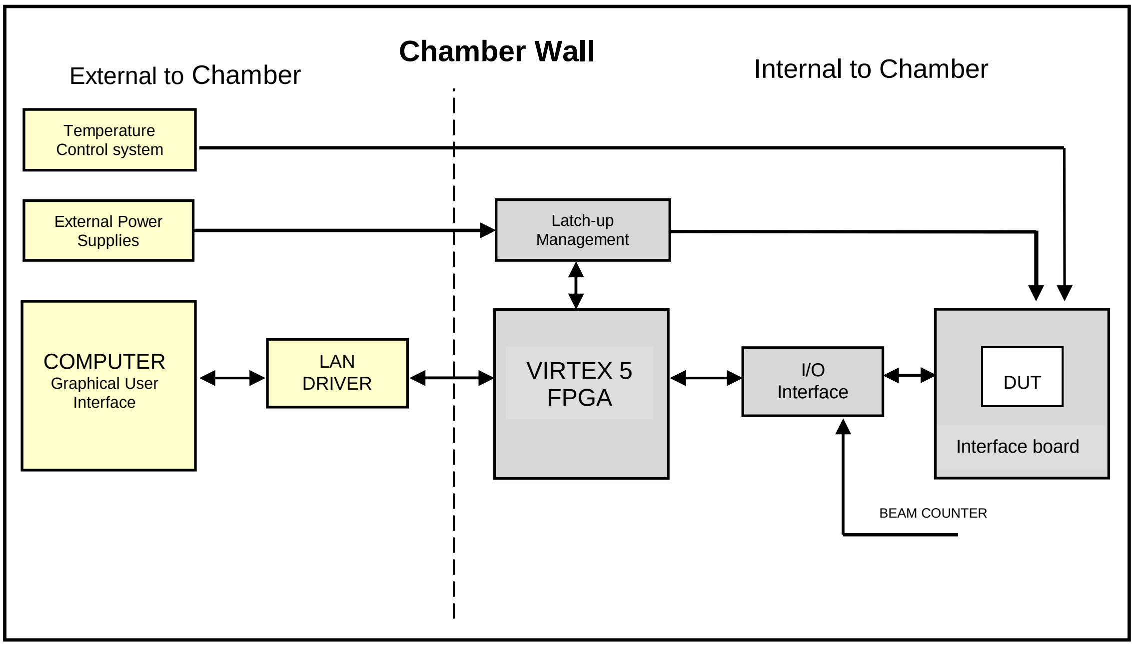


Figure 4: Heavy Ion test set-up

4.2 SDR-SDRAM Test principle

SDR- SDRAM is a memory with a complex internal architecture that controls its operations. Figure 6 shows a bloc diagram of a 256 Megabit SDRAM internal architecture (HM5225165B).

The internal state machine controls all reads and writes processes. These operations are specified by CS (Chip Select), RAS (Row Address Strobe Command), CAS (Column Address Strobe Command), WE (Write Enable) and address pins.

In order to set the operational parameters of the memory the mode register is used. The memory is configured with the burst length of 1, sequential burst type, CAS latency of 2, and single write mode.

OPCODE								CAS latency			Burst Type	Burst Length		
BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	1	0	0	0	1	0	0	0	0	0

Figure 5: Mode Register Configuration

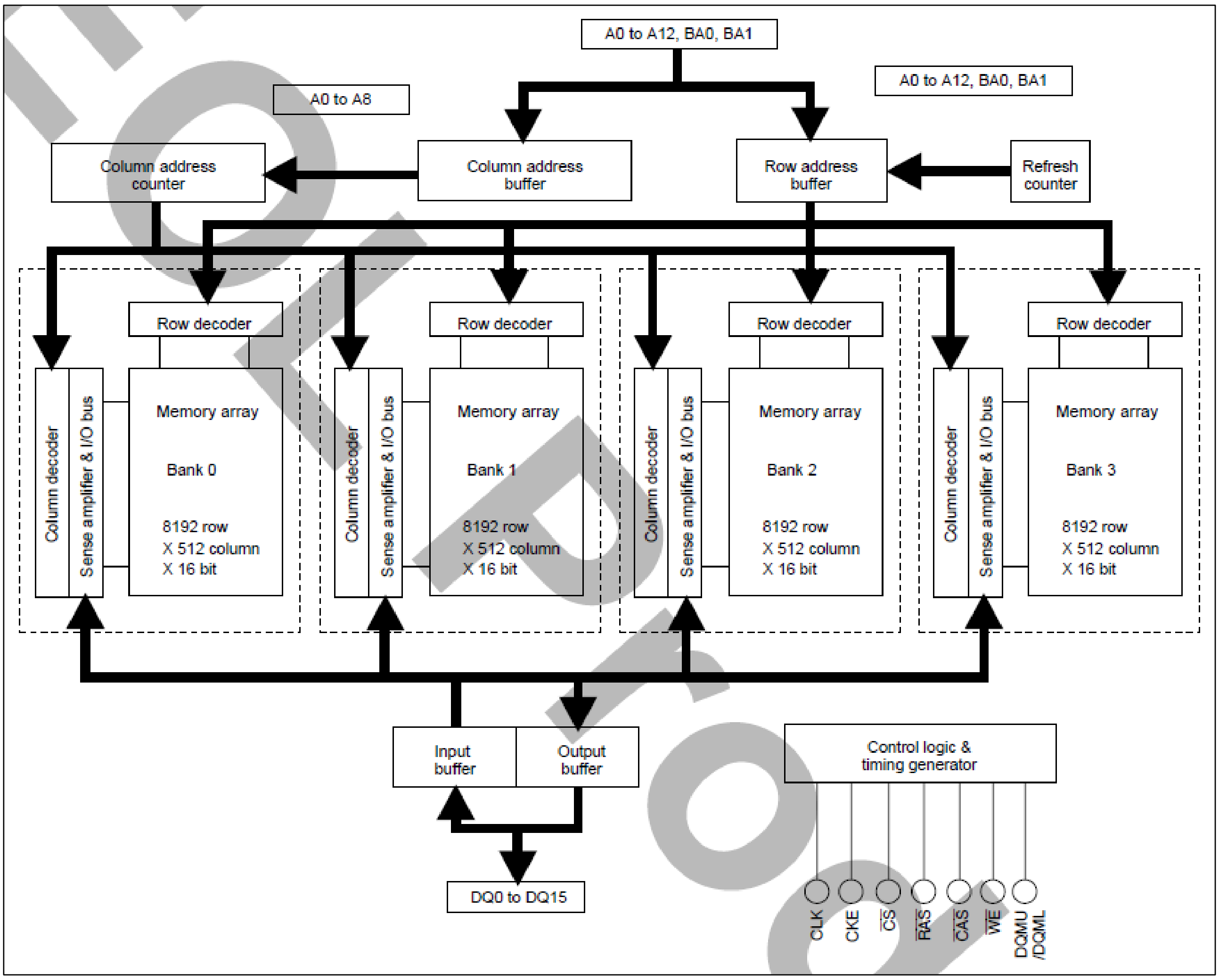


Figure 6: Block of a 256 Megabit SDRAM internal architecture

For the purpose of reading and writing to the memory the following steps are executed:

- The memory is initialized (**Precharge all bank** command, **Auto Refresh** command) and the mode register is configured (**Mode register set** command); The DUT stays in an idle state.
- The row is activated (**Row address strobe and bank active** command), and then write (**Column address and write** command) or read (**Column address and read** command) operation is executed.
- The row is precharged (**Precharge all bank** command) and the DUT returns to the idle state waiting for the next operation.

To maintain the contents of the memory area, the memory needs to be refreshed. Two commands are dedicated for that: Auto Refresh and Self Refresh. In our test only Auto Refresh is used.

The memory test sequence consists in successive iteration cycles. The time frame of one iteration cycle is approximately twelve seconds. That corresponds to the time for reading the memory plus the time to write to the entire memory and the auto refresh cycles. In case of errors detection, this cycle time can increase. During each cycle auto refresh command is sent to the memory. The memory is continuously exposed to the beam all along the test sequence.

SEL detection is performed by monitoring the DUT supply current. The SEL threshold can be adjusted during the test, but in general adjusted before starting the test.

In order to detect SEU events, the entire memory is written with the Memory fill algorithm (see Figure 7) then read with the Memory check algorithm (see Figure 8).

While an error appears the error vector is registered. It is composed of address of error, type of error, send pattern and received pattern.

LE (Large Error) threshold sets the number of the error vectors to be recorded during the test.
Crossing this threshold the system will stop to register the errors; however the test cycle will be proceeded. It avoids the saturation of the test system in case of a high number of errors. LE threshold can be selected from 0 (which means no SEU detection applied) to 2^{32}.

SEFI (Single Event Functional Interrupt) threshold defines the minimum numbers of errors to be reached to consider the error as SEFI event. It can be selected from 0 (which means no SEFI detection applied) to 2^{32}.

SEFI threshold cannot be smaller than LE threshold.

A SEFI management system is integrated in the test sequence. It allows classifying the SEFI in three different types: Soft SEFI type 1 and type 2 as well as hard SEFI. Figure 9 shows the details of the SEFI classification. Two first SEFI types can be recovered by re-initializing the device; the third can only be recovered after power off/on cycle.

The run test sequence is manually defined from the Graphical User Interface (GUI) providing the choice of test mode, auto refresh period, exposition time, device configuration, selected banks, SEL threshold, LE threshold, SEFI threshold, DUT supply voltage etc…

Error type	**Possible causes**
Large Error	row or column error
Write error type 1	Write error
Write error type 2	Write error
Write error type 3	Write error
Write error type 4	Stuck bit
Read error type 1	Read error
Read error type 2	Upset
Read error type 3	Read error
Read error type 4	Stuck bit

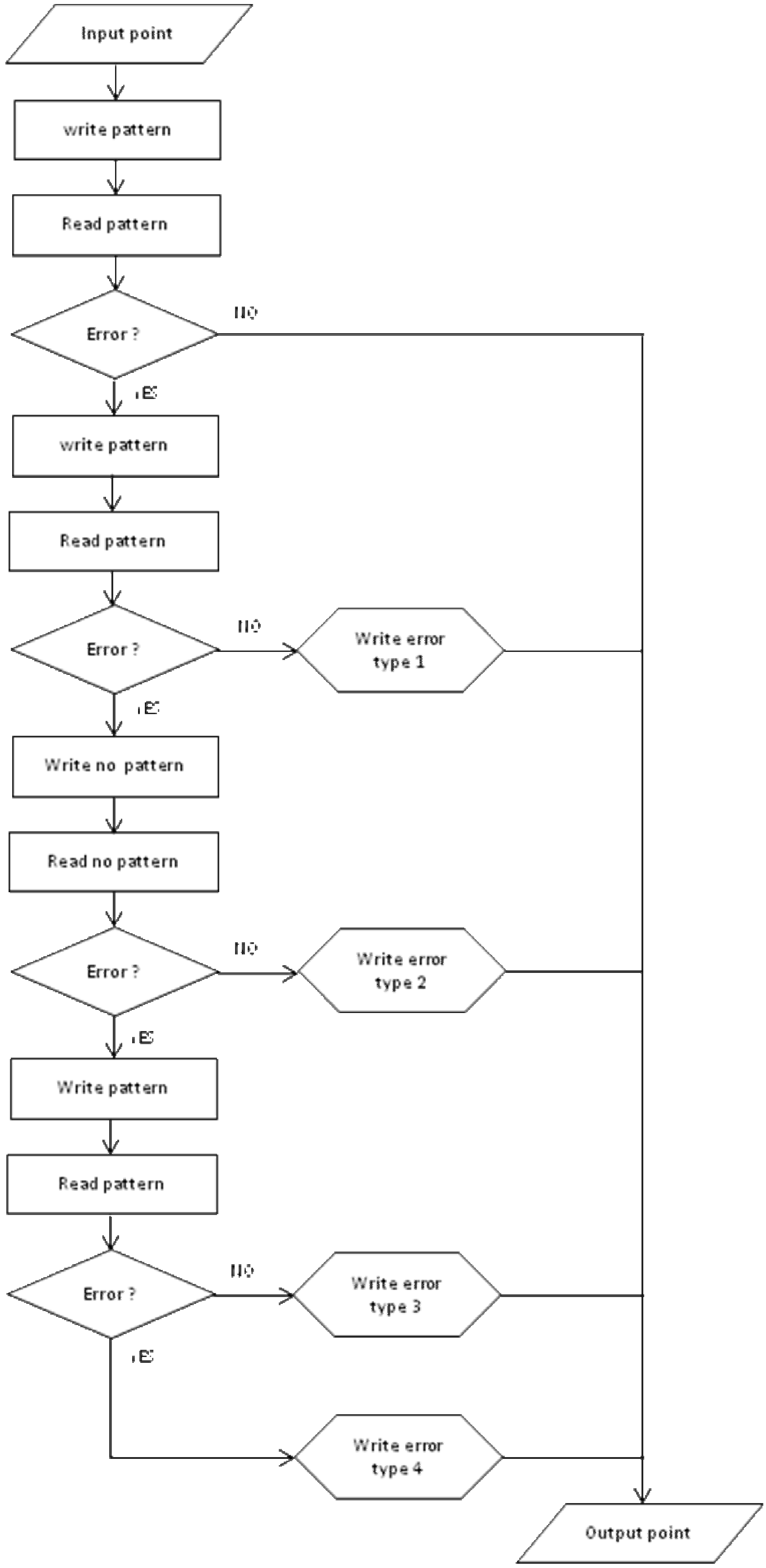


Figure 7: Memory fill algorithm

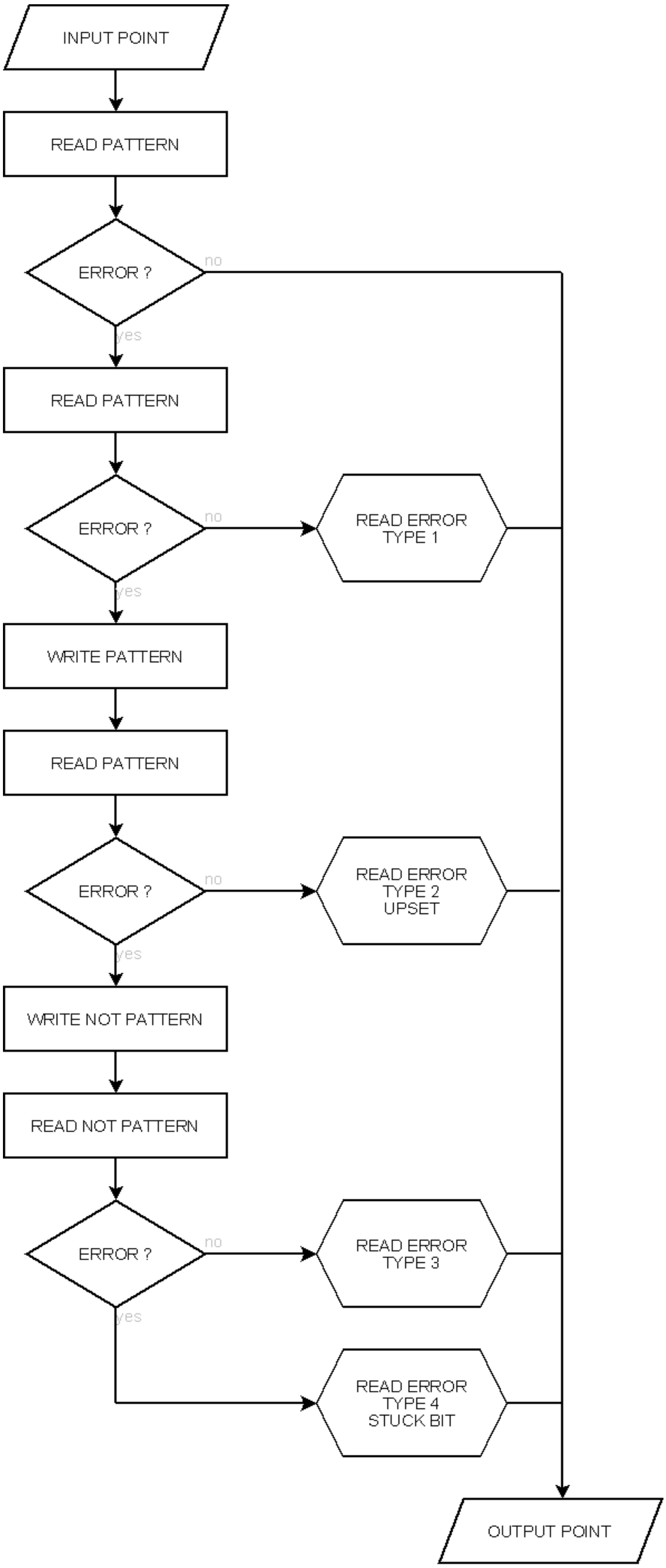


Figure 8: Memory check algorithm

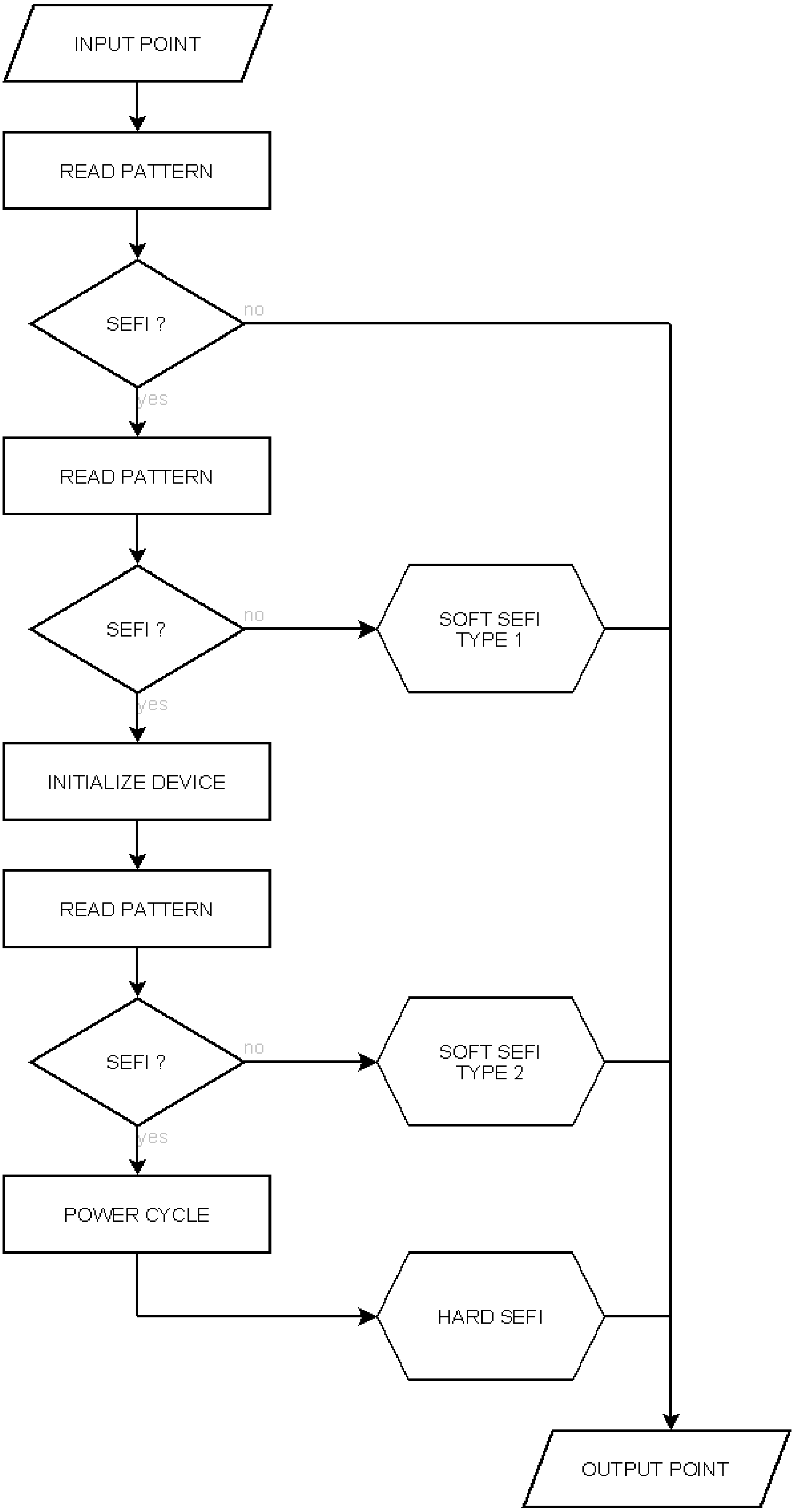


Figure 9: SEFI management algorithm

4.3 Test conditions

The value of the DUT supply voltage is +3.6V (maximum rated) in all test runs. Detection SEL threshold is set at twice the nominal current value.

All runs have been performed with Xenon at different tilt angles.

The tests are done at three different temperatures: ambient chamber temperature, 50 °C and 85 °C.

Patterns used for SEU and SEFI detection were Checkerboard and invert Checkerboard.

The type of test sequence presented in Figure 10 is used for testing the memory. During the Pre Run the DUT is out off beam. When the Run starts the beam is switched on.

As the flux is high, the number of upsets per iteration is too high to reliably gather SEU data. The test conditions allow mainly detection of Latch-up and SEFI events.

In the first test runs the LE threshold is set at fifteen thousand and then decreased to fifty (from RUN35).

In the first test runs the SEFI Threshold equals thirty five thousand. Since the number of observed SEFI events is high the SEFI threshold changes for fifty thousand from RUN 24 and then for one hundred thousand from RUN34.

All the tests are performed with the auto-refresh function. Since the temperature increases during the test, the refresh rate needs to be increased as well. In the two first runs the auto-refresh period equals 49 milliseconds then it is set to 25 milliseconds.

Sequence	1
Pre Run (Turn off beam)	Memory Initialization Memory Fill Algorithm with Checkerboard Pattern
Run (Turn on beam)	Memory Check Algorithm Memory Fill Algorithm with invert Checkerboard Pattern Memory Check Algorithm Memory Fill Algorithm with Checkerboard Pattern

Figure 10: Test sequence used as iteration cycle

5 RADEF Test Facility

Test at the cyclotron accelerator was performed at University of Jyvaskyla (JYFL) (Finland) under HIREX Engineering responsibility.

The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.
The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula

$$130\ Q^2/M,$$

where Q is the ion charge state and M is the mass in Atomic Mass Units.

Test chamber

Irradiation of components is performed in a vacuum chamber with an inside diameter of 75 cm and a height of 81 cm.
The vacuum in the chamber is achieved after 15 minutes of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the X, Y and Z directions. The possibility of rotation around the Y-axis is provided by a round table. The free movement area reserved for the components is 25 cm x 25 cm, which allows one to perform several consecutive irradiations for several different components without breaking the vacuum.
The assembly is equipped with a standard mounting fixture. The adapters required accommodating the special board configurations and the vacuum feed-throughs can also be made in the laboratory's workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components.
A CCD camera with a magnifying telescope is located at the other end of the beam line to determine accurate positioning of the components. The coordinates are stored in the computer's memory allowing fast positioning of various targets during the test.

Beam quality control

For measuring beam uniformity at low intensity, a CsI(Tl) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis.
A set of four collimated PIN-CsI(Tl) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.
Two beam wobblers and/or a 0.5 microns diffusion Gold foil can be used to achieve good beam homogeneity. The foil is placed 3 m in front of the chamber. The wobbler-coils vibrate the beam horizontally and vertically, the proper sweeping area being attained with the adjustable coil-currents.

Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI(Tl) detectors. Three collimators of different size and shape are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.
At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(Tl) detectors.
JYFL facility is an ESA qualified heavy ion facility. Compliance for beam uniformity and fluence dosimetry to ESA/SCC 25100 requirements are under JYFL responsibility.
For the present test, beam rectangular collimator was set to 20mm by 40 mm.

Used ions

The RADEF ion used is listed in the table below.

Ion	**Energy** (MeV)	**LET** (MeV.cm²/mg)	**Range (Si)** (µm)
131Xe35+	1217	32.10	89

Table 1: Used ion and features thereof

6 SEE Test Results

All along the test sequence the SEE events are recorded in a log file, and then treated in order to classify the type of SEE events. The following events are detected:

- SEL
- Soft SEFI Type 1, Soft SEFI Type 2 and Hard SEFI
- SEU Large error:
  - Row errors
  - Column errors
- SEU errors
  - Write Error Type 1
  - Write Error Type 4 (Stuck Bit)
  - Read Error Type 1
  - Read Error Type 2 (Upset)
  - Read Error Type 4 (Stuck Bit)
  - MBU/SBU

Remarks:

i. As the memory organization (descrambling) is not known on this device SCU and MCU cannot be computed.

Detailed results of tests are provided in the Table 2 and Table 3.

6.1 Effective fluence

Test sequence consists in successive cycle iterations. Each time a SEL event occurs, the iteration cycle is aborted and eventual SEU errors are skipped.

The effective fluence corresponds to the total run fluence, minus the time period during which the memory is powered off. This time period corresponds to the number of SELs and Hard SEFIs multiplied by one second (one second was the duration programmed for power off time after SEL event and Hard SEFI event).

6.2 Actual LET

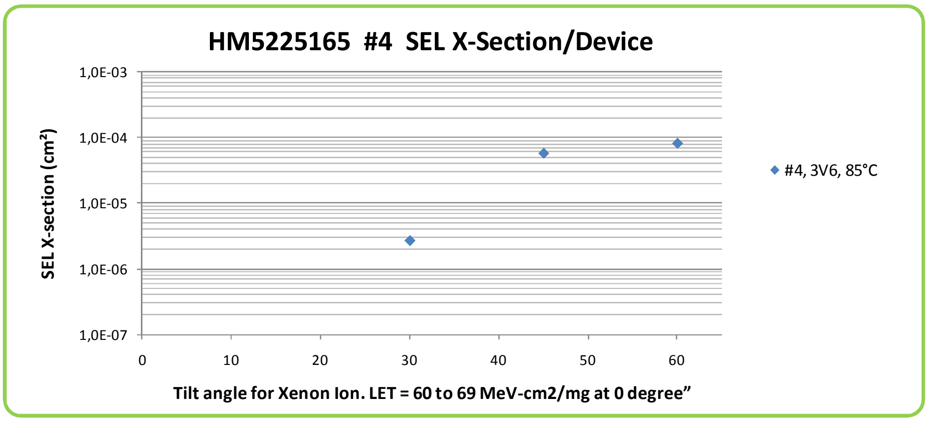
All LET data provided is the LET at the back side surface. The actual LET at the active region (near front side of the die) is a strong function of the thickness of the die and the tilting angle. Figure 3 gives the computed LET as a function of the vertical penetration into the die for different tilting angles.

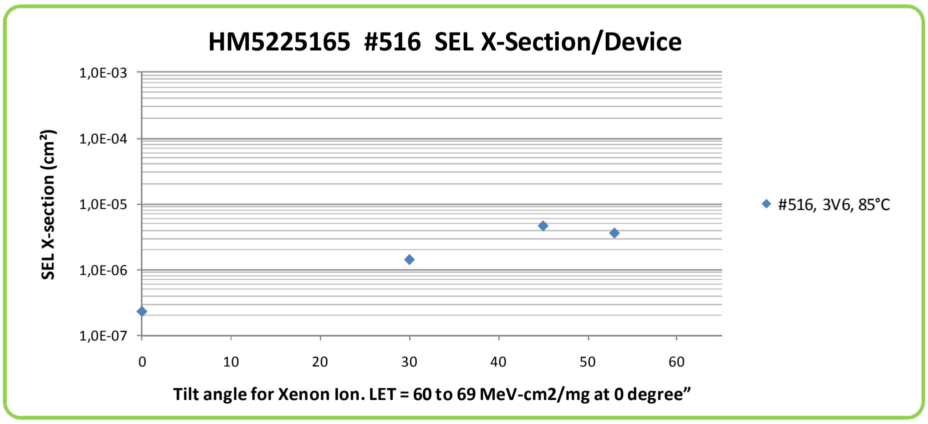
6.3 SEL

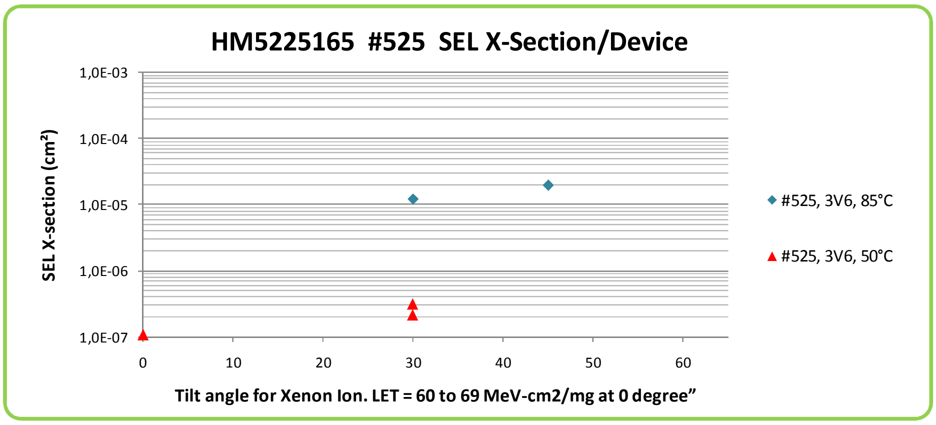
No SEL has been observed at ambient temperature with Xenon at normal incidence. At 50°C and 85°C only rare events of SEL has been recorded with a corresponding SEL cross-section / die near 1.0E-7 cm^2.

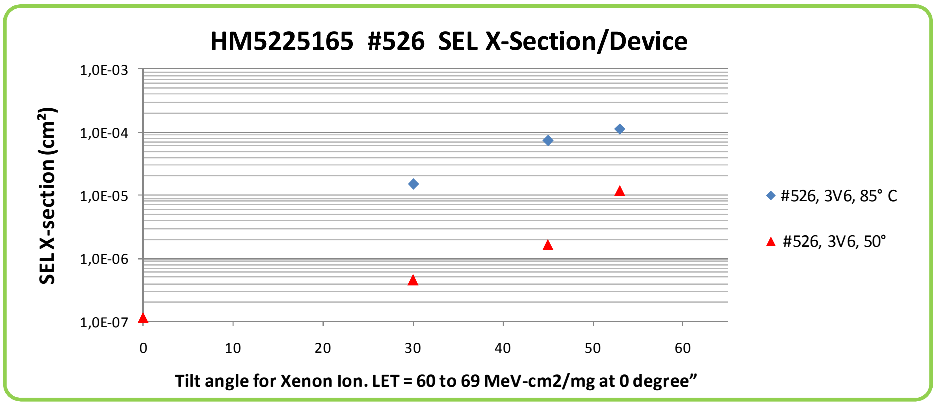
At 85°C SELs were observed at tilt of 30° with a corresponding SEL cross-section / die between 1.5E-06 and 1.5E-5 cm^2.

At about 50°C and with tilt of 30°, some SELs have been observed with a corresponding SEL cross-section / die between 2 and 4E-07 cm^2.









LET values used are the one at the DUT backside surface

Figure 11:SEL cross-section/device

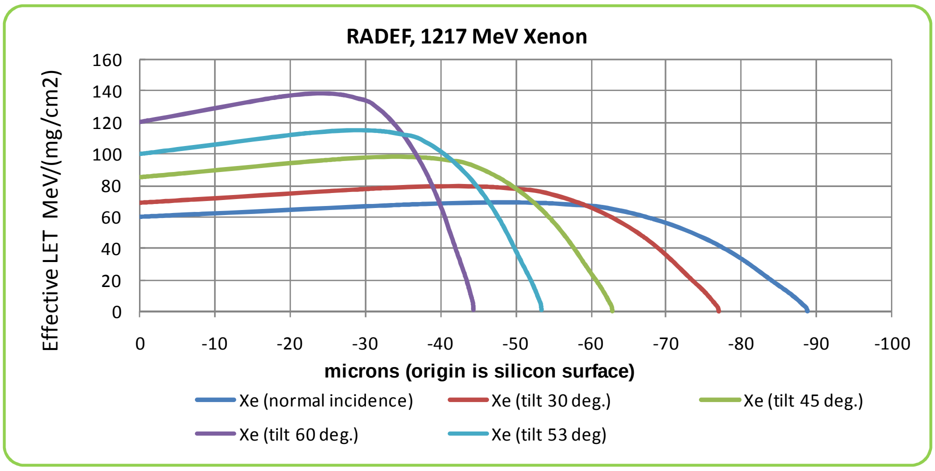
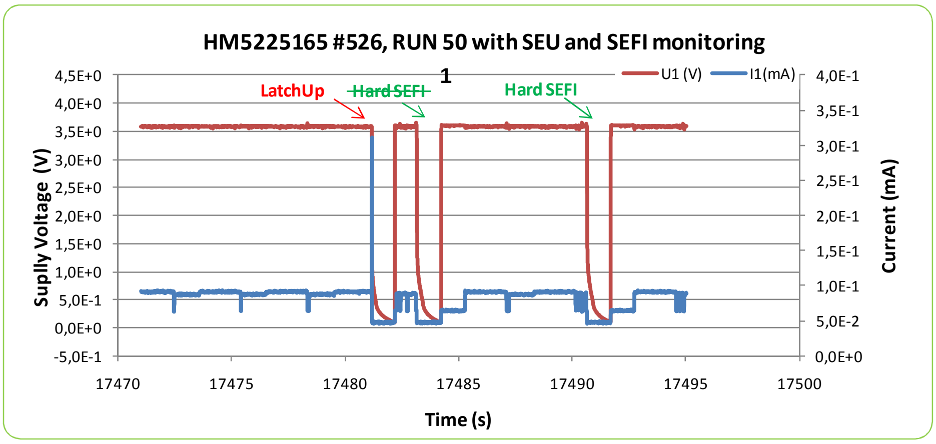


Figure 12: RADEF, 1217 MeV Xenon (LET is computed with SRIM 2008[3])



[1]Nota: There is a test artifact when a Latch-up occurs; it is followed by a hard SEFI due to a wrong memory reading. These Hard SEFIs have been deduced from SEFI Type Statistics.

Figure 13: HM5225165BTT-75, #526, RUN 50

6.4 SEFI

Three types of SEFI have been detected. Figure below presents the statistic of SEFI type occurrence. Hard SEFI Cross-sectional area per device has been plotted for each tested die.

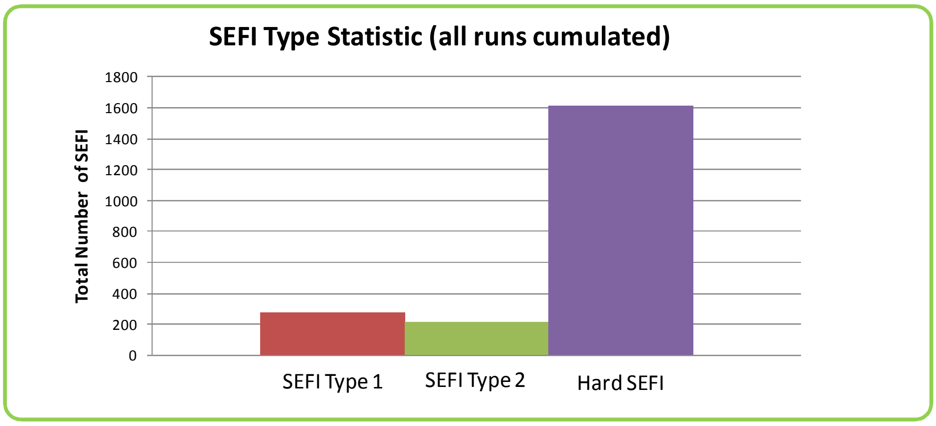
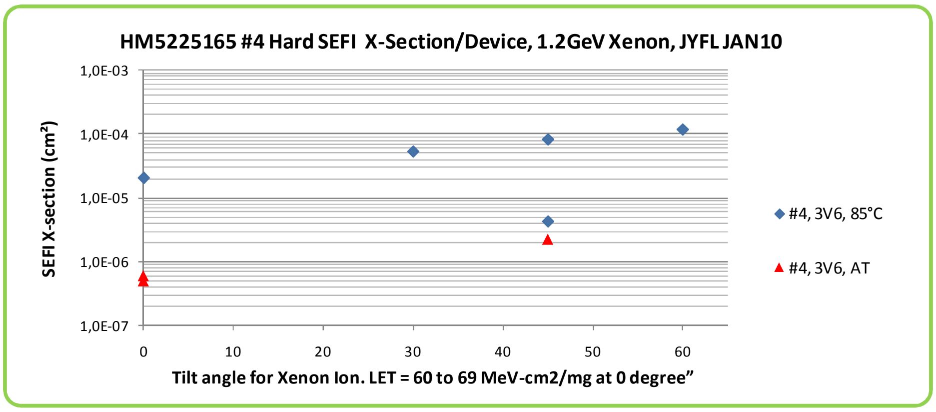
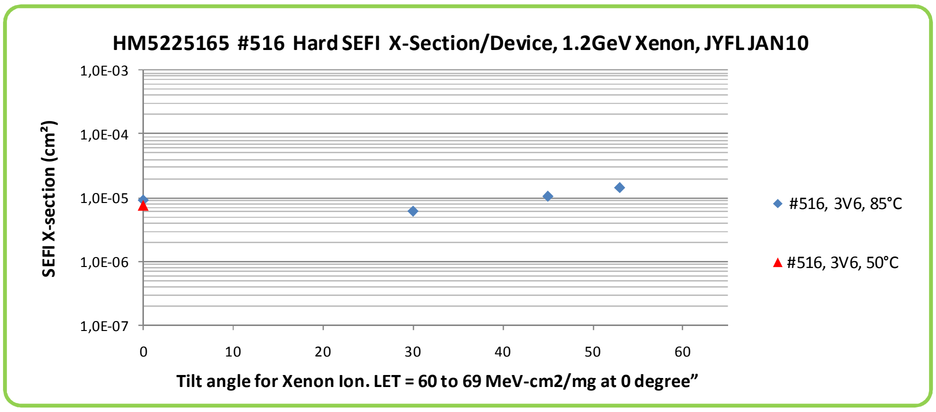
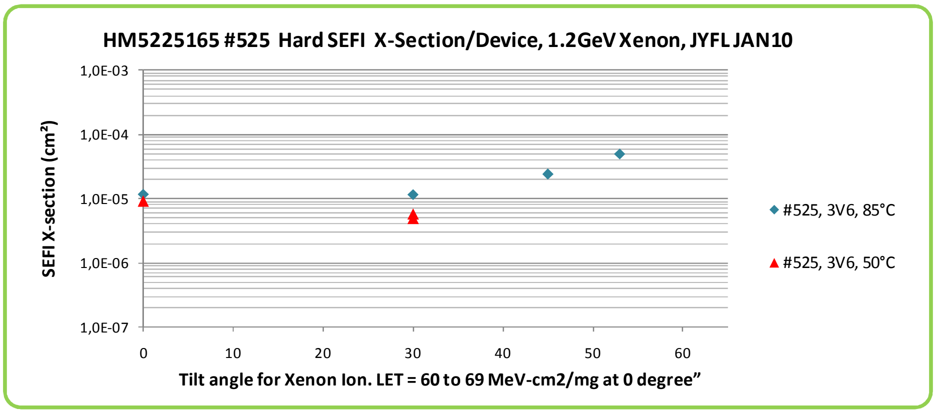


Figure 14: SEFI Type Statistic

[3] http://www.srim.org/SRIM/SRIMLEGL.htm







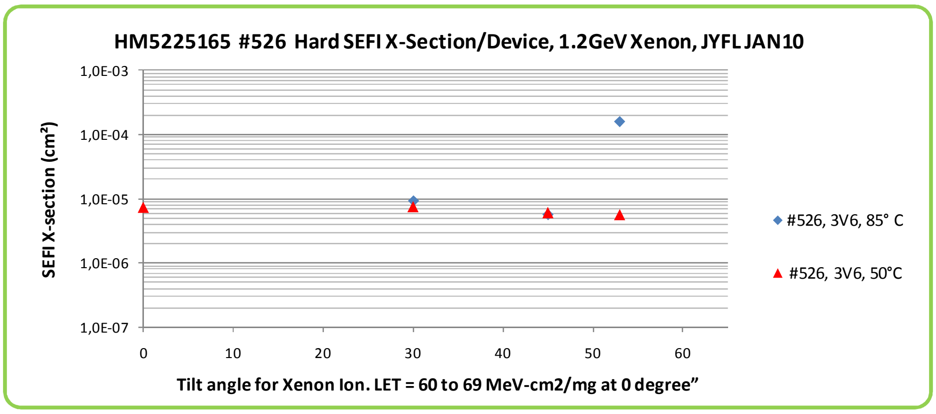


Figure 15: SEFI Cross-sectional area per device

6.5 SEU

It must be noted that the four samples have been tested prior to irradiation at 85°C and were 100% functional on fourteen bits. Due to a poor connection on the interface board, only fourteen bits out of sixteen could be monitored.

Two runs (RUN11 and RUN29) have been performed on S/N4 with a lower flux so that all SEU data could be recorded (i.e. the actual number of word errors / iteration << LE threshold set at fifteen thousand / bank).

The statistics for the SEU events have been plotted in the Figure 16. One can see that the contribution of Multi Bit Upset (MBU) is preponderant. Most of these MBUs consist of words with two bits in error.

Detailed Results per bank are presented in Table 3

Average SEU/cross-section per bit is:

RUN11,
$LET_{surface}$ = 60 MeV/(mg/cm²)) X-section/ bit = 1.4E-09 cm^2

RUN29.
$LET_{surface}$= 84.85 MeV/(mg/cm²)) X-section/ bit= 6.44E-10 cm^2

In RUN11 the beam had a normal incidence compared to RUN29 when the beam was tilted with 45 degree. When the die thickness is below ~53µm the actual LET at active region is higher when tilted with 45 degree (see Figure 3). The die thickness of S/N4 varies between ~37 and ~62 µm (see section 3.4). This means that the actual LET in RUN29 was higher than in RUN11; however the Auto-Refresh time in RUN11 is twice larger than in RUN29. The more often execution of Auto-Refresh cycles in RUN29 might lead to a reduction of SEU events. That could explain the lower cross section recorded in RUN29.

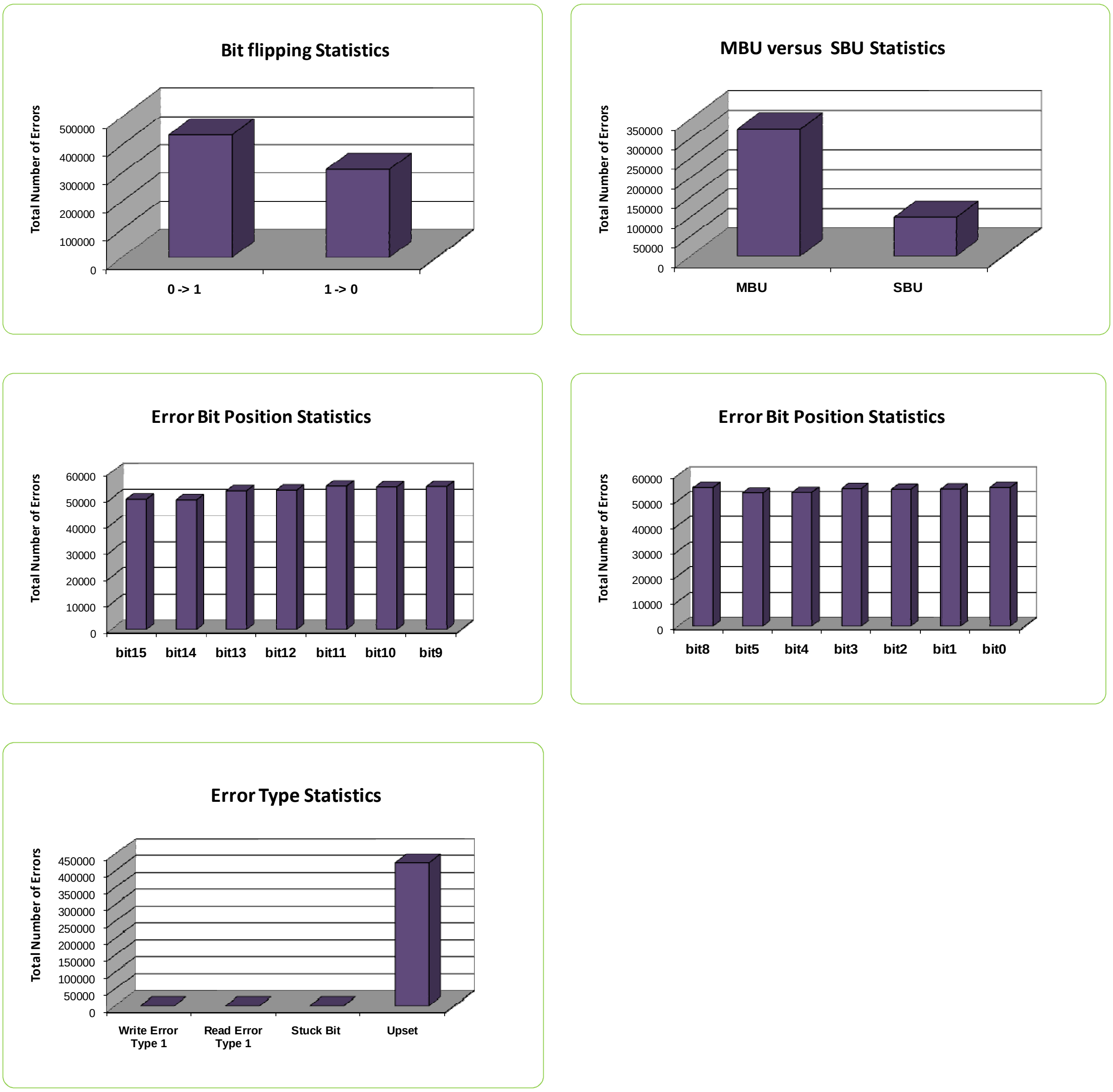


Figure 16: SEU Statistics

7 Detailed results per run

SEL run results table:

HRX RUN	Hirex test run number
Part Type	Type of sample
S/N	Hirex sample number
DUT Voltage	DUT supply voltage1 (V)
DUT Temp	DUT temperature (°C)
Ion	Ion specie
Energy	Ion incident energy (MeV)
LET	Linear Energy Transfer (MeV/(mg/cm²))
TILT	DUT tilt angle with beam direction (deg)
Eff LET	LET / (cos(tilt angle) (MeV/(mg/cm²))
Eff Range	Ion range in Silicon (microns)
Fluence	Cumulated number of ions over the test run (cm^{-2})
Total Time	Time with beam (s)
Flux	Effective Fluence (cm^{-2} x s^{-1})
SEL	Number of SELs
SEL X section	SEL error cross-section per device (cm^2)

7.1 Detailed run table

HRX Run #	Part type	S/N	TEST COND	Auto-Refresh (ms)	test pattern	DUT VOLTAGE	DUT TEMP	ION	RANGE	LET at DUT back surface	TILT	EFF. LET at DUT back surface	FLUENCE	FLUX	TIME	Eff Fluence (K.p/cm²)	dose / run	SEL	SEFI SOFT 1	SEFI SOFT 2	Hard SEFI	SEFI X-Section / Device (cm²)	SEL X-Section / Device (cm²)
11	HM5225165BTT-75	Commercial #4	Auto-refresh	49	checkerboard	3,6	RT	131Xe+35	89	60	0	60,00	2,00E+06	1,61E+03	1242	2,00E+06	1,92E+03	0	0	1	1	5,00E-07	
12	HM5225165BTT-75	Commercial #4	Auto-refresh	49	checkerboard	3,6	RT	131Xe+35	89	60	0	60,00	1,00E+07	1,20E+04	830	9,93E+06	9,60E+03	0	1	10	6	6,04E-07	
17	HM5225165BTT-75	Commercial #4	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	0	60,00	2,00E+06	1,97E+03	1015	1,92E+06	1,92E+03	0	0	1	39	2,03E-05	
20	HM5225165BTT-75	Commercial #4	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	30	69,28	2,00E+06	1,67E+03	1200	1,83E+06	1,92E+03	5	0	0	96	5,24E-05	2,73E-06
22	HM5225165BTT-75	Commercial #4	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	45	84,85	2,00E+06	1,15E+03	1733	1,72E+06	1,92E+03	99	14	9	140	8,12E-05	5,74E-05
24	HM5225165BTT-75	Commercial #4	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	60	120,00	2,00E+06	7,04E+02	2839	1,76E+06	1,92E+03	142	26	23	204	1,16E-04	8,09E-05
29	HM5225165BTT-75	Commercial #4	Auto-refresh	25	checkerboard	3,6	45	131Xe+35	89	60	45	84,85	8,97E+05	2,32E+03	387	8,92E+05	8,61E+02	0	0	2	2	2,24E-06	
30	HM5225165BTT-75	Commercial #4	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	45	84,85	2,00E+06	1,26E+04	159	1,90E+06	1,92E+03	0	0	0	8	4,21E-06	
33	HM5225165BTT-75	astrium #525	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	0	60,00	2,00E+06	1,30E+04	154	1,74E+06	1,92E+03	0	0	1	20	1,15E-05	
35	HM5225165BTT-75	astrium #525	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	30	69,28	2,00E+06	1,12E+04	179	1,59E+06	1,92E+03	19	0	0	18	1,13E-05	1,20E-05
36	HM5225165BTT-75	astrium #525	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	45	84,85	2,00E+06	4,73E+03	423	1,66E+06	1,92E+03	32	1	2	40	2,41E-05	1,93E-05
37	HM5225165BTT-75	astrium #525	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	53	99,70	2,00E+06	3,82E+03	524	1,68E+06	1,92E+03	0	0	1	84	5,00E-05	
38	HM5225165BTT-75	astrium #525	Auto-refresh	25	checkerboard	3,6	50	131Xe+35	89	60	30	69,28	1,00E+07	7,70E+03	1298	9,61E+06	9,60E+03	3	44	6	47	4,89E-06	3,12E-07
39	HM5225165BTT-75	astrium #525	Auto-refresh	25	checkerboard	3,6	50	131Xe+35	89	60	0	60,00	1,00E+07	1,07E+04	935	9,10E+06	9,60E+03	1	77	4	83	9,12E-06	1,10E-07
40	HM5225165BTT-75	astrium #525	Auto-refresh	25	checkerboard	3,6	42	131Xe+35	89	60	30	69,28	1,00E+07	1,38E+04	726	9,24E+06	1,11E+04	2	12	35	53	5,73E-06	2,16E-07
42	HM5225165BTT-75	astrium #516	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	30	69,28	1,00E+07	1,42E+04	702	9,03E+06	9,60E+03	13	26	20	55	6,09E-06	1,44E-06
43	HM5225165BTT-75	astrium #516	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	45	84,85	1,00E+07	1,11E+04	897	8,56E+06	9,60E+03	40	5	25	89	1,04E-05	4,67E-06
44	HM5225165BTT-75	astrium #516	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	53	99,70	1,00E+07	9,94E+03	1006	8,49E+06	9,60E+03	31	1	4	121	1,43E-05	3,65E-06
45	HM5225165BTT-75	astrium #516	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	0	60,00	1,00E+07	1,91E+04	523	8,49E+06	9,60E+03	2	0	2	77	9,07E-06	2,36E-07
46	HM5225165BTT-75	astrium #516	Auto-refresh	25	checkerboard	3,6	50	131Xe+35	89	60	0	60,00	1,00E+07	2,13E+04	470	8,60E+06	9,60E+03	0	0	1	66	7,68E-06	
50	HM5225165BTT-75	astrium #526	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	30	69,28	2,00E+06	9,09E+03	220	1,64E+06	1,92E+03	25	2	2	15	9,17E-06	1,53E-05
51	HM5225165BTT-75	astrium #526	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	45	84,85	2,00E+06	4,96E+03	403	1,43E+06	1,92E+03	107	10	16	8	5,60E-06	7,49E-05
52	HM5225165BTT-75	astrium #526	Auto-refresh	25	checkerboard	3,6	85	131Xe+35	89	60	53	99,70	1,00E+06	9,70E+02	1031	7,91E+05	9,60E+02	90	4	3	125	1,58E-04	1,14E-04
54	HM5225165BTT-75	astrium #526	Auto-refresh	25	checkerboard	3,6	50	131Xe+35	89	60	53	99,70	5,00E+06	8,29E+03	603	4,36E+06	4,80E+03	52	18	10	25	5,73E-06	1,19E-05
55	HM5225165BTT-75	astrium #526	Auto-refresh	25	checkerboard	3,6	50	131Xe+35	89	60	45	84,85	1,00E+07	1,26E+04	795	9,11E+06	9,60E+03	15	34	30	56	6,15E-06	1,65E-06
56	HM5225165BTT-75	astrium #526	Auto-refresh	25	checkerboard	3,6	50	131Xe+35	89	60	30	69,28	1,00E+07	1,90E+04	527	8,67E+06	9,60E+03	4	0	4	66	7,61E-06	4,61E-07
57	HM5225165BTT-75	astrium #526	Auto-refresh	25	checkerboard	3,6	50	131Xe+35	89	60	0	60,00	1,00E+07	2,11E+04	475	8,63E+06	9,60E+03	1	0	4	64	7,41E-06	1,16E-07

Table 2: RADEF, DEC 09, run table for the HM5225165 – BTT75 die

Cut name	Runs #	Row Errors	Row word errors	Col Errors	Col word errors	Write error type 1	Write error type 4	Read error type 1	Read error type 2	Read error type 4	1bit word error	2bit word error	3bit word error	4bit word error	5bit word error	>5bit word error	total word error	total word error/iteration	0->1	1->0	total bit error
bank0	RUN11	215	88713	5477	32506	1	9	4	89896	5	22559	67317	10	15	0	14	89915	1873	90631	66765	157396
bank1	RUN11	70	18676	10766	70806	4	10	6	92123	3	22120	69979	16	17	1	13	92146	1920	93019	69279	162298
bank2	RUN11	35	5029	5424	36683	2	8	4	90916	3	22321	68589	8	5	0	10	90933	1894	93342	66293	159635
bank3	RUN11	19	614	4577	31735	2	9	2	92140	13	23032	69092	8	12	1	21	92166	1920	93656	67837	161493
bank0	run29	149	15425	6208	53949	1	2	0	12534	1	3385	9146	1	3	0	3	12538	1045	12631	9084	21715
bank1	run29	54	13303	3429	23615	3	10	0	15618	0	680	14938	0	1	2	10	15631	1303	18418	12223	30641
bank2	run29	154	6473	5251	47612	2	4	2	13736	1	3568	10164	2	5	0	6	13745	1145	14634	9341	23975
bank3	run29	23	6564	3175	23842	1	4	2	16227	3	1371	14859	1	1	0	5	16237	1353	19078	12065	31143

Cut name	Runs #	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	total bit error
bank0	RUN11	11240	11344	11248	11257	11189	11225	11209	11278	0	0	11248	11257	11189	11225	11209	11278	157396
bank1	RUN11	11068	11082	11851	11950	11759	11538	11428	11548	0	0	11851	11950	11759	11538	11428	11548	162298
bank2	RUN11	11145	11196	11151	11276	11435	11430	11579	11776	0	0	11151	11276	11435	11430	11579	11776	159635
bank3	RUN11	11686	11383	11833	11746	11515	11419	11184	11515	0	0	11833	11746	11515	11419	11184	11515	161493
bank0	run29	1726	1663	1652	1636	1661	1597	1368	1249	0	0	1652	1636	1661	1597	1368	1249	21715
bank1	run29	355	336	1561	1569	2668	2763	3256	3158	0	0	1561	1569	2668	2763	3256	3158	30641
bank2	run29	1780	1797	1737	1758	1706	1825	1600	1573	0	0	1737	1758	1706	1825	1600	1573	23975
bank3	run29	702	677	1882	1954	2713	2556	2835	2942	0	0	1882	1954	2713	2556	2835	2942	31143

Nota 1: Bits six and seven have not been tested
Nota 2: The row and column errors are excluded from word error data

Table 3: RADEF, DEC 09, SEU run table for the HM5225165 – BTT75, S/N 4