Title : Evaluation of the TID Radiation Test Results of SHAMROC Phase 1 ADC

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Document Change Record

Version	Date	Changed	Description of Change
0.1	12-02-2009		New Document
0.2	09-03-2009		Added Environment section Added Sine Wave section
0.9	16-03-2009		Revised Sine Wave section to ADC Function Section
1.0	31-03-2009		Comments from SRON integrated
1.1	14-07-2009		Distributionlist has been modified

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Abbreviations and acronyms

Item	Meaning
ADC	Analog To Digital Converter
ASIC	Application Specific Integrated Circuit
DUT	Device Under Test
ESA	European Space Agency
ESPAX	EXOMARS ASIC Space Qualification of Mixed-Signal ASICS
ESTEC	European Space Research and Technology Centre
HD3	Harmonic Distortion of Third Component
HIPO	Hi-Resist Poly
IO	Input Output
LSB	Least Significant Bit
SEIS	Seismometer
SHAMROC	SEIS High Accuracy Mixed-Signal Read-out Chip
TID	Total Ionizing Dose

Applicable Documents

[AD#]	Doc. Reference	Version	Title
[AD1]	SRON-SHAMROC-RS-2007-001	3.0	SHAMROC ASIC Design Specification
[AD2]	SRON-ED-ASIC-PEP-2006-01	1	Project Plan ESPAX
[AD3]	SRON/ESPAX/PL/2008-001	1	Project Plan ESPAX (revised)

Reference Documents

[RD#]	Doc. Reference	Version	Title
[RD1]	XENSOR-SHAMROC-TR-2009-002	1.0	Evaluation of TID Radiation Test Results of SHAMROC Phase 1 ADC Data Compendium
[RD2]	SRON-SHAMROC-PL-2007-015	2.0	Radiation testplan (TID)

1 Introduction

During the lifetime of the SHAMROC ASIC, it will be subjected to radiation on its mission to mars. To study the effect of ionizing radiation, the SHAMROC ASIC will be subjected to a Total-Ionization-Dose (TID) test, as part of the space qualification process. Within the frame of the ESPAX project, the phase 1 sub-blocks of the SHAMROC ASIC are individually TID tested to investigate if major TID induced problems can be expected.

During the EXOMARS mission the electronics of the SHAMROC ASIC will endure a maximum TID of 6.2kRad (SHAMROC-0080 in [AD1]). In order to investigate the influence of this TID radiation on the performance of the ADC 5 devices will be subjected to a low dose of up to 16krad.
To further assess the radiation tolerance *limits* of the ADC, 5 devices are subjected to a high dose of up to 409krad.
For this purpose, two setups have been created.
In order to separate systematic influence of the measurement setup from the radiation effects, 1 reference device is added to the test. This device has not been irradiated.

The evaluation results are an essential input for the SHAMROC design team and - if deemed necessary – may lead to design optimization measures that improve the radiation hardness of the integrated chip at a later stage of the project. Table 1 will show which device belongs to which category.

Table 1: Device categorization for TID test.

Device	Category	Dose Measurements (kRad)
6210A-1002	High Dose	0, 43.8, 135.7, 409.5
6210A-1012	High Dose	0, 43.8, 135.7, 409.5
6210A-1014	High Dose	0, 43.8, 135.7, 409.5
6210A-1016	High Dose	0, 43.8, 135.7, 409.5
6210A-1018	High Dose	0, 43.8, 135.7, 409.5
6210A-1001	Low Dose	0, 1.97, 4.11, 16.32
6210A-1005	Low Dose	0, 1.97, 4.11, 16.32
6210A-1009	Low Dose	0, 1.97, 4.11, 16.32
6210A-1011	Low Dose	0, 1.97, 4.11, 16.32
6210A-1019	Low Dose	0, 1.97, 4.11, 16.32
6210A-1003	Reference	No Irradiation

Measuring only five devices per dose implies that the amount of measurements will not be enough to draw statistically proven conclusions. The conclusions will thus be formulated as indications. Later in the space qualification process, a TID test will be performed where the sample size is in-line with the requirements of ESCC22900, that is 10 samples + 1 reference sample. The goal of this test is to investigate if there are major TID induces issues to be solved, which this test will show.
All the devices were tested 8 times:

T10. Once at SRON before irradiation,
T20. Once at ESTEC before irradiation,
T30. Once after 1 day of irradiation,
T40. Once after 3 days of irradiation,
T50. Once after 9 days of irradiation,
T60. Once back at SRON,
T70. Once after annealing, and
T80. Once after accelerated ageing.

The annealing process consists of biasing the devices for one day at 20˚ C, while the accelerated ageing process consists biasing the devices for seven days at 100˚ C. The reference device is not irradiated, annealed or aged in any way.

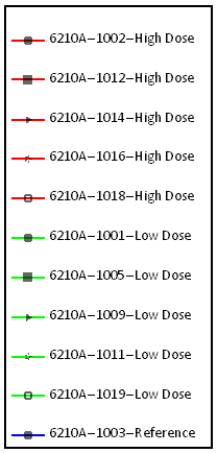

Figure 1: The common legend for all figures in this document.

Figure 1 shows the common legend for all figures in this document. In order to save space this legend is not included on every page. Generally speaking, all the high-dose devices are drawn in red, the low-dose devices are drawn in green, and the reference device is drawn in blue.

Sometimes the output of the ADC is presented as a voltage. The real output of an ADC is of course a digital word which is related to the ratio of the input voltage and the reference voltage. The conversion to voltage is performed by dividing the filter output by the maximum filter output of 50 million. The normalized result is multiplied by a gain of 2.85 and an offset of 1.425 is subtracted from the result.

Chapter 2 will show the housekeeping measurements performed of the reference and ADC temperature. These measurements can be used to interpret the ADC specification measurements presented in chapter 3. Chapter 4 represents the radiation influence with regards to the ADC requirements. Finally conclusions are drawn and recommendations are presented in chapter 5.

2 House Keeping Measurements

As part of the TID test, the supply power, supply voltage and supply current, the reference voltage, as well as the DUT, reference temperature, and reference converter temperature are measured. The supply parameters have been individually measured for digital, analog and IO circuits.

In section 3.6 the power supply measurements are presented. In section 2.1 the reference voltage measurements are presented. Section 2.2 will show the temperature measurement results. Housekeeping parameters cannot be influenced by radiation, since the irradiated samples are measured on a test board that is located outside the radiation chamber.

2.1 Reference Voltage

The reference voltage shows a radiation effect for the high-dose devices at 409kRad (Figure 2 Left). The reference drops up-to 2mV due to radiation, which is mended by annealing and accelerated ageing.

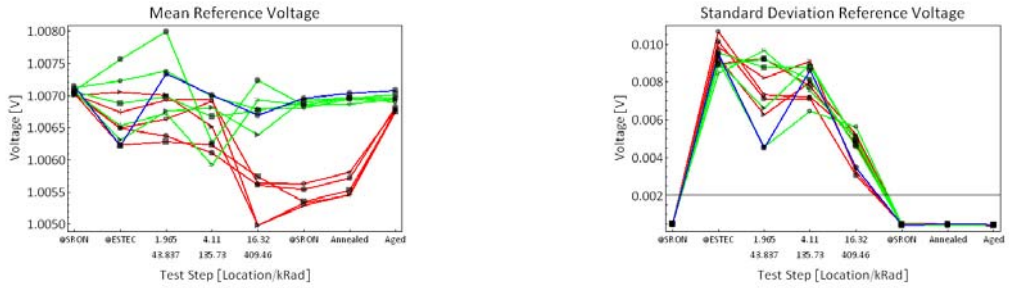

Figure 2: Mean (left) & standard deviation (right) of the reference voltage during TID testing.

In Figure 2 right the standard deviation of the reference voltage is shown.

2.2 Temperature Measurements

From the measurements below, it can be seen that the device-under-test (DUT) is slightly higher in temperature at ESTEC compared to the temperature at SRON (See Figure 3). The reference temperature does not seem to be influenced by location (See Figure 4), since it is placed in a temperature controlled box. There is no correlation between temperature and radiation level, which is as expected.

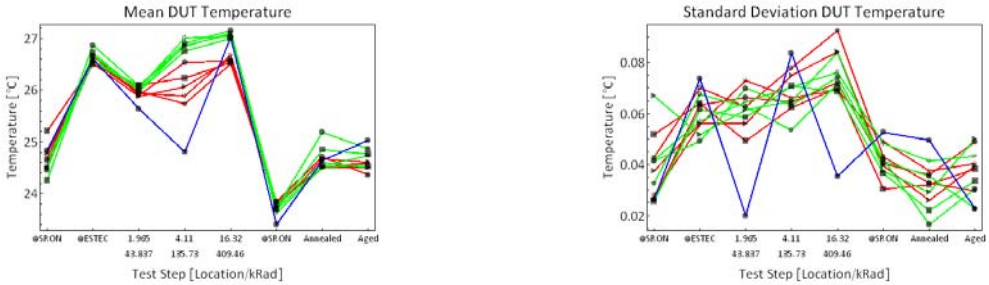

Figure 3: Mean (left) & standard deviation (right) of the ADC chip's temperature during TID testing.

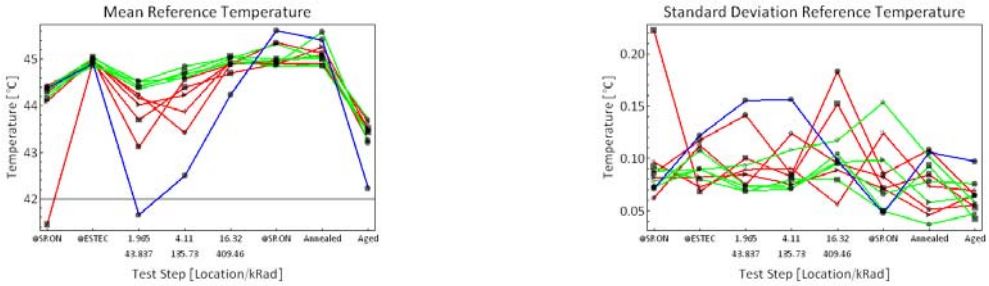

Figure 4: Mean (left) & standard deviation (right) of the reference temperature during TID testing.

3 ADC Specification Measurements

3.1 ADC Offset

The ADC offset is definitely affected by radiation. Two types of offset can be distinguished:

- offset without chopping,
- offset with chopping.

Offset with chopping is further categorized as:

- offset with vi chopping,
- offset with common mode chopping,
- offset with vi & common mode chopping.

The most interesting case is when both VI and common mode choppers are activated which is normal operation. The offset with chopping is well below 100LSB. The influence of the radiation is limited to 10LSB for the low-dose devices (from step 2 to step 5). For the high-dose devices the offset change is limited to 30LSB before the devices fail (below 409kRad, from step 2 to step 4). Even with this small drift the offset requirement of 500LSB is met (SHAMROC-0440 [AD1]). The offset drift of the low-dose devices is negligibly small. Accelerated ageing shows a slight annealing effect on the ADC offset drift of the low-dose devices (from step 7 to step 8). It seems that the annealing effect occurs not during the annealing step itself which is at 20˚ C, but during accelerated ageing which occurs at 100˚ C. The reference device shows a similar effect, so this could also be a drift due to environmental changes of the setup.

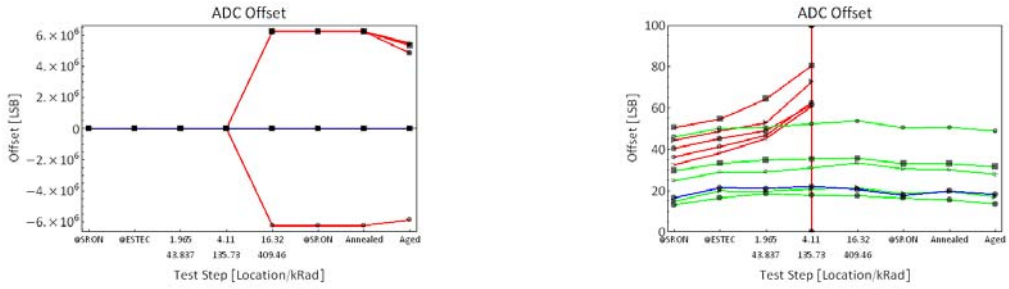

Figure 5: ADC Offset with VI chopper at 2kHz and CM chopper at 5kHz: full view right, zoomed view left.

In Figure 6 the offset without chopping is shown. Generally this offset is in the range of ±10000LSB. The low-dose devices and the reference device show little to no offset change. The high-dose devices, however, do show a significant offset change of up-to 1500LSB due to radiation before failing at 409kRad (between step 2 and step 4 in Figure 6 right).

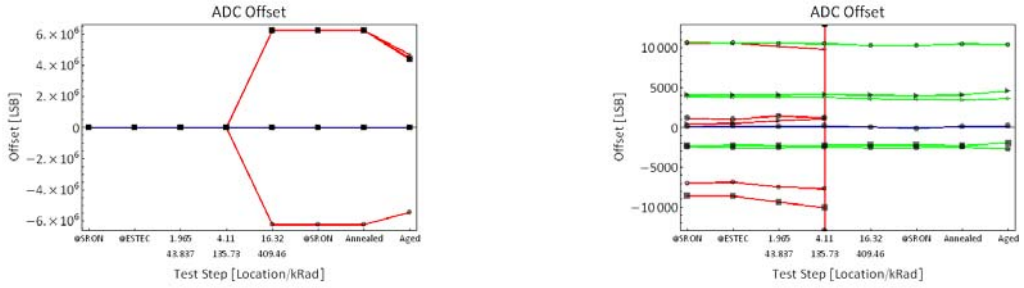

Figure 6: ADC Offset with VI chopper off and CM chopper off: full view right, zoomed view left.

Both high-dose and low-dose devices show an offset drift during accelerated ageing (between step 7 and step 8). For the low-dose devices this effect is even higher than when the offset drift during radiation. Table 2 shows the change in offset between measurements for all devices. The low-dose devices in green show a significant offset change due to accelerated ageing (last column) of up-to 500 LSB. This effect is larger than the effects from radiation in columns 3, 4, and 5, which is up-to 280LSB cumulatively.
A possible explanation is that the radiation effect becomes only apparent after the irradiation itself at high temperatures. Another possibility is that this annealing effect takes place even without irradiation of the devices. Introduction of a second reference device which is not irradiated, but is annealed and acceleratedly aged, could give us the answer to this question.

Table 2: ADC offset drift in lsb. The change in offset per device is shown from measurement to measurement. The choppers are off.

Devices	SRON→ESTEC	→44/2kRad	→136/4kRad	→409/16kRad	ESTEC→SRON	→Anneal	→Ageing
6210A-1002	-179.1	458.948	-300.123	6.25E+06	0	0	-1.87E+06
6210A-1012	-54.7923	-777.012	-695.335	6.26E+06	0	0	-1.85E+06
6210A-1014	95.3808	316.256	265.323	6.25E+06	0	0	-1.77E+06
6210A-1016	5.55769	-436.513	-399.004	6.24E+06	0	0	-1.56E+06
6210A-1018	155.562	-593.317	-221.271	-6.24E+06	0	0	788323
6210A-1001	-122.688	-1.58269	88.4462	-97.5923	11.4423	59.5962	-241.479
6210A-1005	51.1923	-19.75	9.56154	84.4365	-33.6423	-88.1788	375.331
6210A-1009	-51.7731	41.8942	35.7904	-57.9077	-104.46	121.981	494.242
6210A-1011	-105.513	50.5	-28.8231	-225.767	-25.6846	-120.279	188.573
6210A-1019	-80.1019	-20.6404	-47.45	-209.519	-2.20385	169.825	-73.3596
6210A-1003	81.7865	-26.425	31.5635	-116.75	-207.294	302.765	32.8038

When the choppers around the VI (signal input stage) are activated, the offset with chopping drops to below 3000 LSB (See Figure 7). The TID induced offset change is reduced as well to a few hundred LSB's, while the offset drift below 409 kRad in negligible. A similar offset change during accelerated ageing is seen as when the choppers are off.

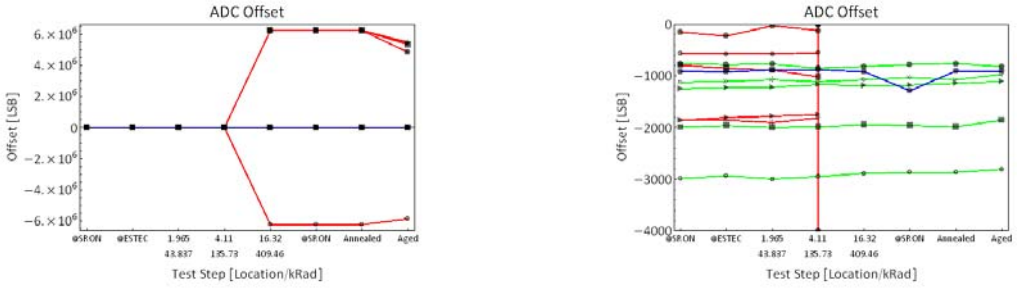

Figure 7: ADC Offset with VI chopper at 2kHz and CM chopper off: full view right, zoomed view left.

When the common mode chopper is activated the offset is reduced for some devices and slightly worse for others (See Figure 8. Apparently the offsets of the VIC and common-mode control circuits are sometimes compensating.
For the low dose rate devices no observable drift can be detected as a function of radiation, where for the high dose devices the drift is in the same order of magnitude as seen without the choppers active. Again a similar offset change during accelerated ageing is seen as when the choppers are off.

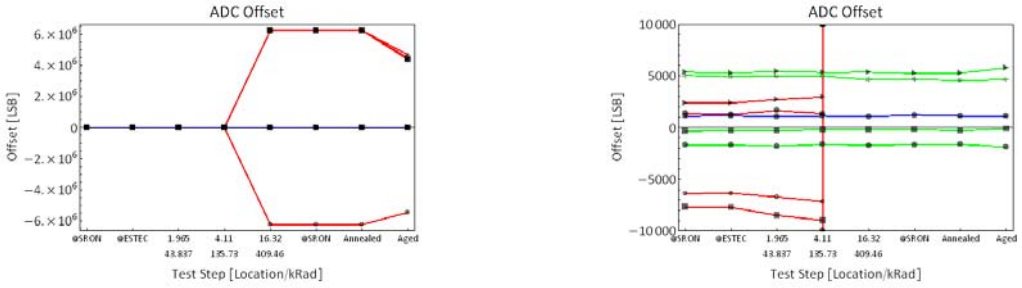

Figure 8: ADC Offset with VI chopper off and CM chopper at 5kHz: full view right, zoomed view left.

3.2 ADC Gain Measurements

In order to measure the influence of the TID on the ADC gain, a sine wave of 2.05078Hz is applied to the ADC input. This is done twice, first with 1V amplitude and second with 1.25V amplitude. By measuring the output, the gain is calculated by dividing the peak-to-peak LSB output value by the peak-to-peak input voltage. Figure 9 & Figure 10 show the results for 1V and 1.25V amplitude sine wave input respectively. On the left of both figures the absolute gain is plotted, while on the left the relative gain is plotted. The relative gain percentage is calculated by dividing the gain by the gain of step 2 (@ESTEC before irradiation) and multiplying the result by 100. During both measurements the choppers of the ADC were switched on (VI @ 2kHz, CM @ 5kHz).

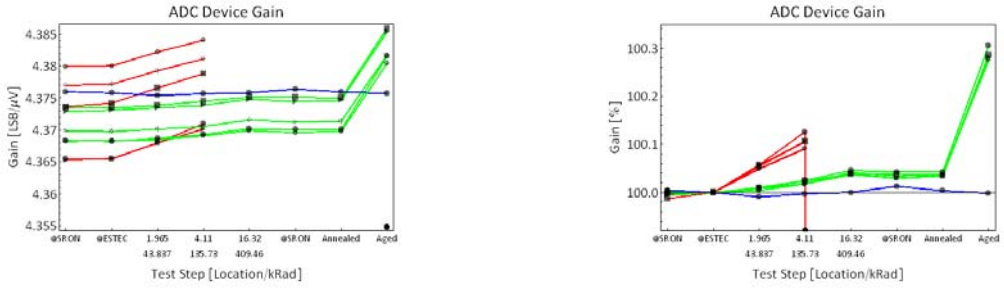

Figure 9: ADC gain based on the sine wave input measurements with 1V amplitude: absolute value right, relative value left (relative to first measurement @ESTEC).

The TID induced gain drift is about 0.03% at 6.2kRad, and 0.04% for the full dose of the low-dose devices. For the high-dose devices, the gain drifts about 0.12% at 135kRad before functional failing (See Figure 9 & Figure 10).
During accelerated ageing a gain drift is visible of almost 0.3%. Whether this drift is due to natural ageing or annealing of radiation effects is not possible to distinguish. A second reference device which is annealed and aged could give us the answer as mentioned before.
The gain error specification is 1% (SHAMROC-0430 [AD1]). The TID gain drift is well below this specification.
Possible causes for this gain drift are HIPO resistor drift, or reference buffer offset drift. If it is HIPO resistor drift then the drift should be visible in the analog power, since the current source values are set by a HIPO resistor. The analog power does not seem to change for the low-dose devices (See Figure 19) while the ADC gain does change for the low-dose devices, thus the HIPO resistors do not seem to be a candidate to explain this effect. The prime candidate is thus the offset drift of the reference buffer. Further analysis needs to be done to determine the definite cause of the gain drift.

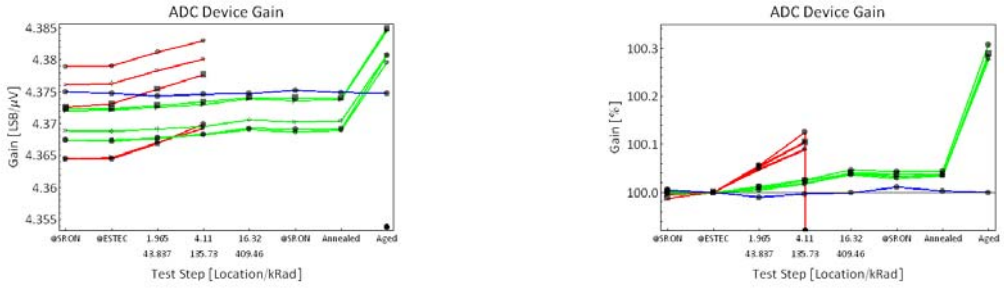

Figure 10: ADC gain based on the sine wave input measurements with 1.25V amplitude: absolute value right, relative value left (relative to first measurement @ESTEC).

3.3 ADC Noise

The ADC noise does not seem to have a TID radiation effect. To illustrate this conclusion Figure 11 shows the noise spectrum of a typical device before radiation on the left, and after a TID of 136kRad on the right. No visible increase in the noise spectrum is visible. During this test the VI-chopper operated at 2kHz and the CM-chopper at 5kHz.

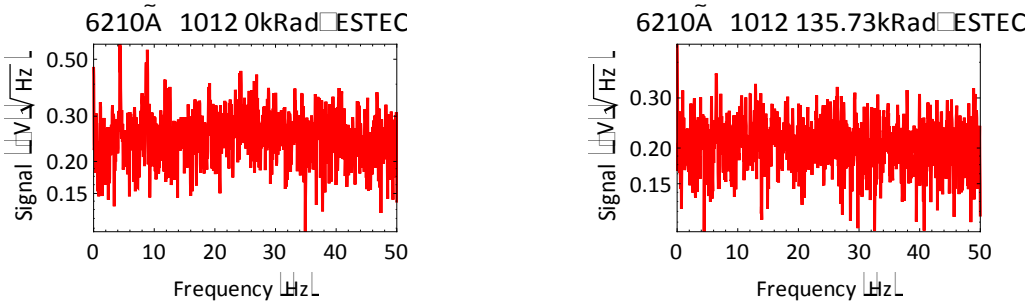

Figure 11: Noise spectrum of a typical device with a shorted input before irradiation (left) and after a TID of 136kRad (right). The VI-chopper operated at 2kHz, while the CM-chopper operated at 5kHz. The x-axes are in Hz, the y-axes are in μV/√(Hz).

During this test the VI-chopper operated at 2kHz, so the 1/f-noise TID effect of the 1/f-noise is not visible in this picture. Figure 12 shows the noise spectrum of the same device under the same circumstances except for the VI-chopper which is now turned off. Even the 1/f-noise does not show a visible increase before (left) and after (right) a 136kRad TID.

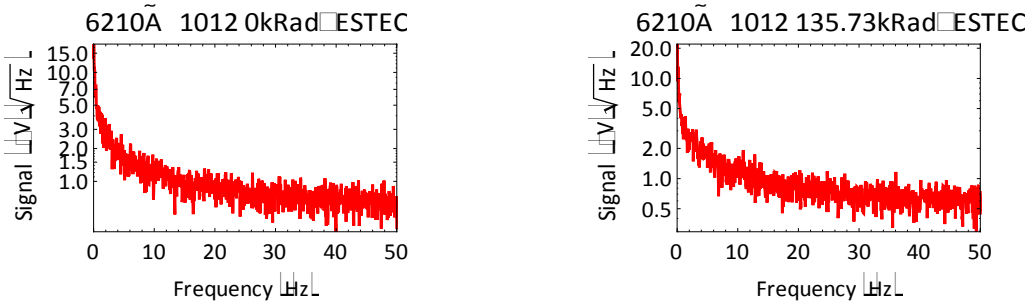

Figure 12: Noise spectrum of a typical device with a shorted input before irradiation (left) and after

a TID of 136kRad (right). The VI-chopper was switched off, while the CM-chopper operated at 5kHz. The x-axes are in Hz, the y-axes are in µV/√(Hz).

3.4 Harmonic Distortion

No TID radiation effects were seen on the HD3 measurements except when the devices were failing. Figure 13 & Figure 14 show the HD3 distortion for a 1V & 1.25V sine wave input respectively. On the left of the figures the general view shows that the HD3 is drastically increased due to the functional failure of the devices at 409kRad TID. The right side of the figures shows a zoomed view, where the conclusion can be drawn that when the devices are still functional the HD3 distortion is not effected by radiation. Although there seems to be a systematic effect of the annealing and ageing increasing the HD3 distortion, this must be explained by variations in the test setup since the reference device (blue) also shows the same effect.

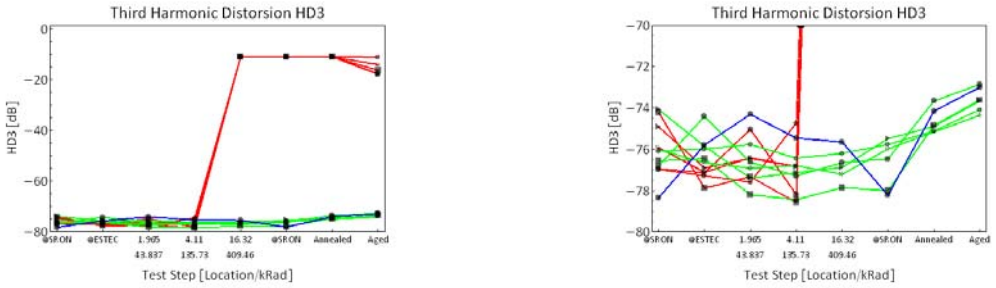

Figure 13: HD3 or third order harmonic distortion measured with a 1V amplitude sine wave on the input (general on the left, zoomed on the right).

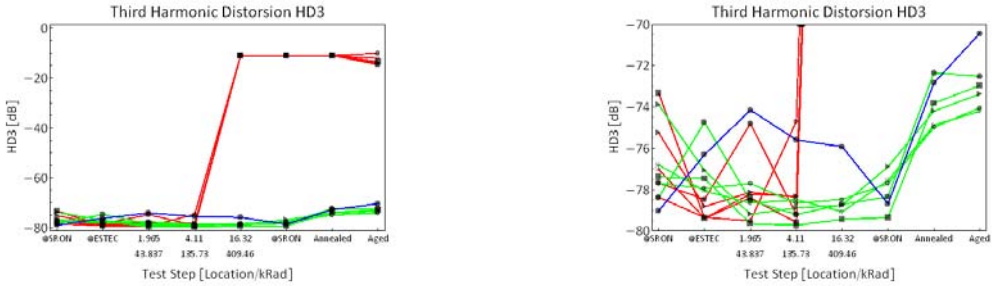

Figure 14: HD3 or third order harmonic distortion measured with a 1.25V amplitude sine wave on the input (general on the left, zoomed on the right).

3.5 ADC Failure

Somewhere between a TID of 136kRad and 409kRad the devices will stop functioning, but what does that mean? Two possible failure modes are shown in Figure 15 & Figure 16: bitstream stuck at 1, or bitstream stuck at 0. Figure 15 shows the 1.25V input sine wave (grey) on the left with a functional ADC output in red. In the middle part of the figure the ADC output in red shows the stuck at 1 output. After annealing and ageing the function of the ADC restores somewhat (right), however, not to a useful level.

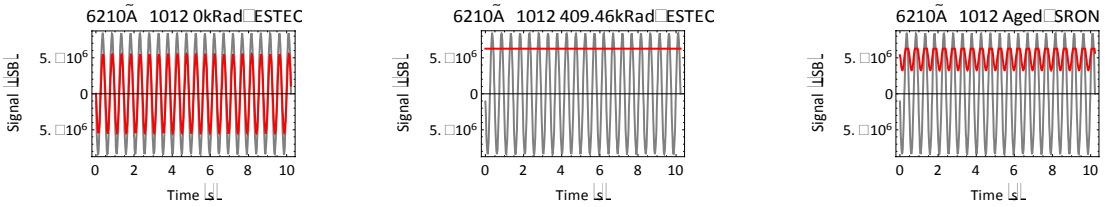

Figure 15: Functional Failure of device 1012 illustrated with a 1.25V input sine wave (grey) before irradiation (left), when failing at 409kRad TID (middle), and after annealing and accelerated ageing (right).

In Figure 16 a similar picture is shown, but now with a stuck at 0 error in the middle picture.

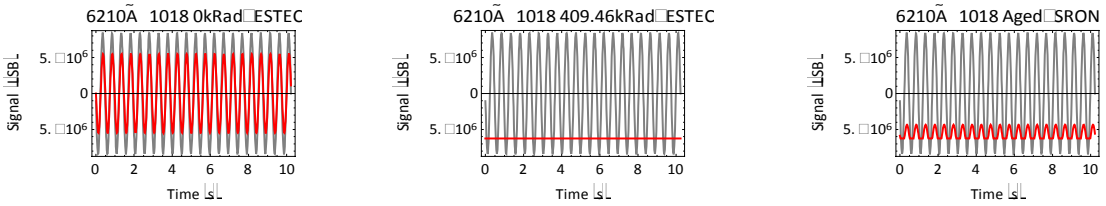

Figure 16: Functional Failure of device 1018 illustrated with a 1.25V input sine wave (grey) before irradiation (left), when failing at 409kRad TID (middle), and after annealing and accelerated ageing (right).

A possible explanation can best be sought by V_t drift. Where in the ADC the dominant V_t shift is located is pure guesswork. More detailed modeling of the transistors over radiation is necessary in order to predict this accurately. We can conclude that the ADC stop functioning due to a stuck at 0 or 1 by the bitstream.

3.6 Power Supply Measurements

3.6.1 Total Power

Figure 17 left shows the total power of the devices during the TID testing. For the reference and the low-dose devices there is no visible total power change during the test. The high-dose devices, however, show a slight power increase of about 0.2mW at 136kRad, and a huge power increase of about 2.4mW at 409kRad. This huge power increase corresponds to the complete functional failure of the device, as can be seen in section 2.1.2 of [RD1]. After annealing the ADC function restores a little bit, but not enough for functioning within specifications.
The power increase of 0.2mW corresponds to an increase of 3.3%, which is well below the specification of 10% (SHAMROC-0110 [AD1]). When the device is functionally failing at 409kRad then the power has increased by 39%, which is also outside the specifications. The total power stays within specification up-to at least 136kRad.

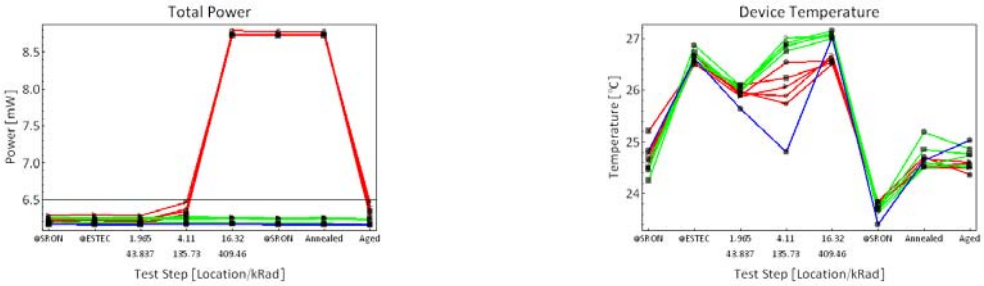

Figure 17: Total power (left) and temperature (right) of the ADC chip during TID testing.

The device temperature (Figure 17 right) shows a rough average of about 26.5˚ C when measured at ESA/ESTEC, and an average of about 24.5˚ C when measured at SRON. This seems to be true for all devices. If differences between the measurements at SRON or ESTEC are found this could be a possible explanation for them.

3.6.2 Power of the Analog Circuits

The power of the analog circuits is influenced by radiation only for the high-dose devices (See Figure 18 left & Figure 19). When these devices have been irradiated up to 136kRad the average power is increased notably by maximum 0.2mW. At 409kRad of radiation, the power has increased over 2mW, and the devices are no longer functional. The increase of the total power is thus caused by the increase in analog power.

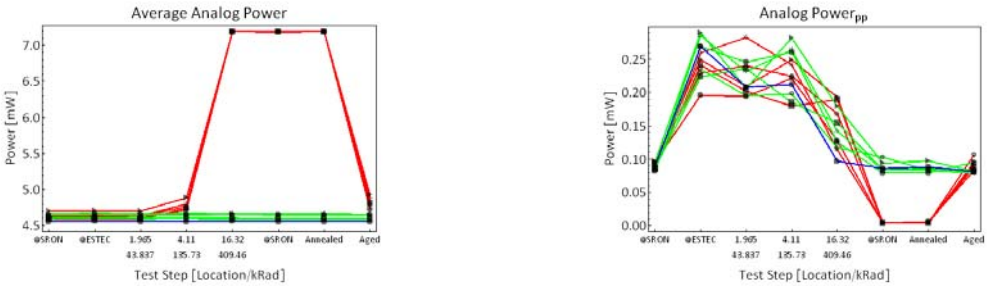

Figure 18: Average power (left) & peak-to-peak power noise (right) of the ADC chip's analog circuits during TID testing.

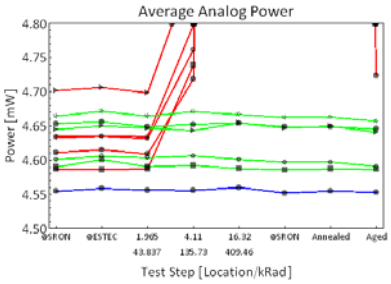

Figure 19: Average power of the ADC chip's analog circuits during TID testing (Zoomed).

The peak-to-peak noise of the analog power shows about 2.5 times increase when measured at ESA/ESTEC (Figure 18 right). On the last day of measurements at ESA/ESTEC the power supply noise is slightly less. The same effect is seen with the standard deviation of the analog voltage (Figure 20 right) and current (Figure 21 right), the digital power

(Figure 22 right), voltage (Figure 23 right) and current (Figure 24 right), the IO power (Figure 25 right), and current (Figure 26 right), the reference voltage (Figure 2 right). This effect does not correlate with the ADC's temperature (Figure 3) or the reference temperature (Figure 4), and the measurement setup has been identical in all places. This effect could explain the increased standard deviation on the DUT temperature measurements (Figure 3 right).
A possible explanation can be the noise of the power grid, which differs in time and place. This has not been measured, so there is no way to prove this. A measurement of the grid voltage stability, combined with grid supply filtering or a battery operated measurement setup could prevent this problems. This could possibly reduce the spread on the measurement data, which could strengthen the conclusions regarding the ADC.

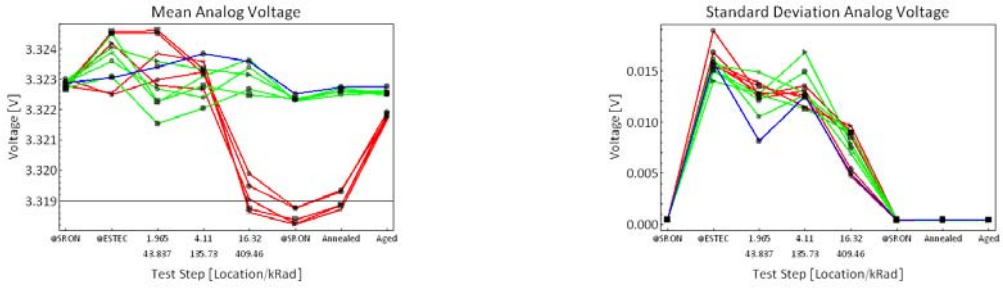

Figure 20: Mean (left) & standard deviation (right) of the ADC chip's analog voltage during TID testing.

For the low-dose devices, no significant voltage change can be correlated with the radiation dose. The high dose device, however, show a slight decrease in analog voltage (Figure 20 left), and a major increase in analog current consumption (Figure 21 left), when the devices are failing at 409kRad. The decrease in analog voltage is explained by the power supply impedance which steals some of the voltage due to the high current when the device is functionally failing. Accelerated ageing seems to repair some of the damage, since the voltage and current go back to the 136kRad levels.

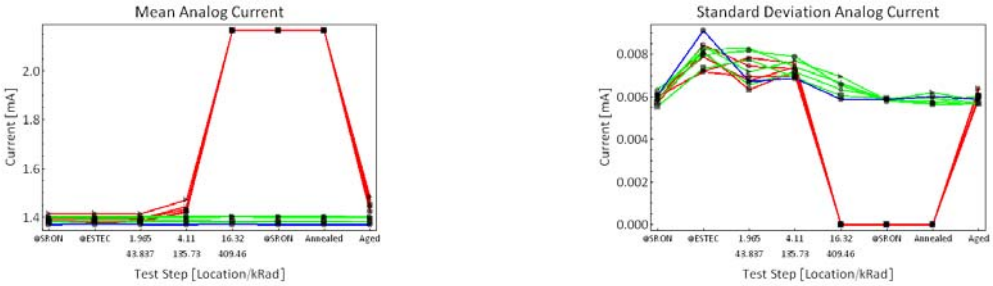

Figure 21: Mean (left) & standard deviation (right) of the ADC chip's analog current during TID testing.

3.6.3 Power of the Digital Circuits

When the focus is turned to the digital power consumption and its peak-to-peak variation (Figure 22), then four out of five high-dose devices dissipate 50µW less than before failing. The only device that does not show a digital power decrease is device 6210A-1002, however, its digital power still decreases after accelerated ageing. There seems to be an effect on the digital power, however, its effect is small and not consistent. Since the digital power supply and analog power supply are completely separate, the extra analog power drawn when the high-dose devices are failing cannot influence the digital power through the supply. A common ground line does not seem to be the cause either, since the reduced analog current after accelerated ageing does not restore the digital power. The most likely cause of this power reduction is the clipping of the analog bitstream signal which is either V_{dd}(4 devices, See section 2.1.2 of [RD1]) or V_{ss}(1 device) when the analog circuits are failing. This introduces a simplified state in the digital circuits, which can lead to

lower power consumption in the digital circuits. The conclusion is that there is a small digital power decrease at the highest radiation level of 409kRad most likely due to the failing of the analog circuits.
The difference in power, voltage and current noise between locations is also visible for the digital circuits (See Figure 22 right, Figure 23 right & Figure 24 right). This effect was already discussed in the previous section.

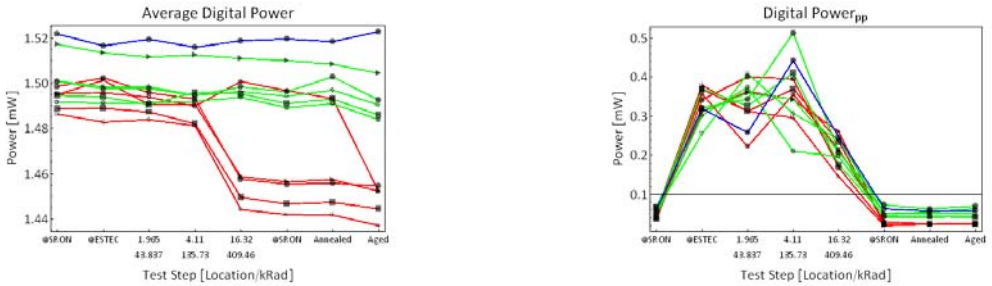

Figure 22: Average power (left) & peak-to-peak power noise (right) of the ADC chip's digital circuits during TID testing.

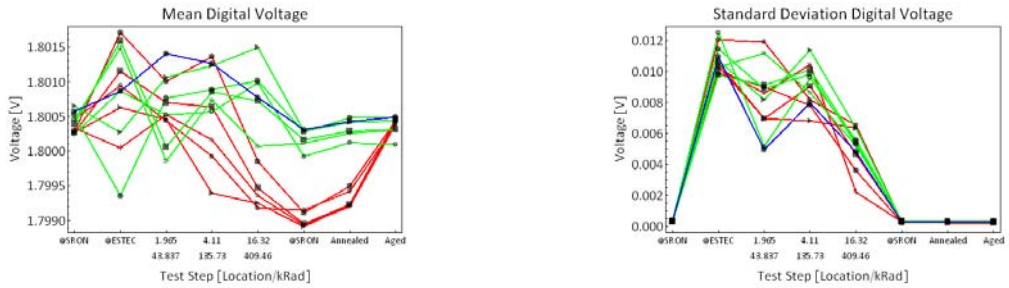

Figure 23: Mean (left) & standard deviation (right) of the ADC chip's digital voltage during TID testing.

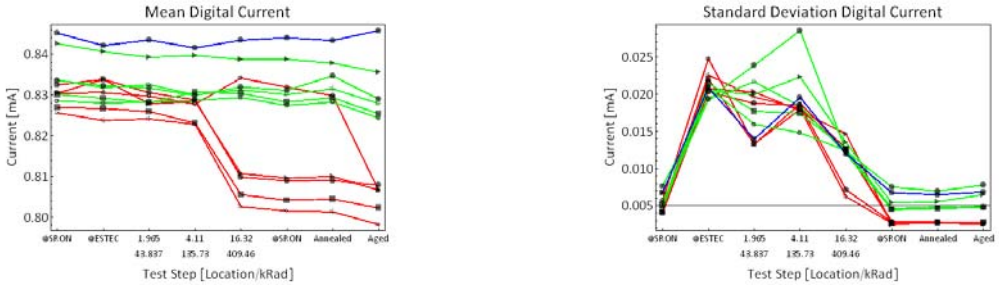

Figure 24: Mean (left) & standard deviation (right) of the ADC chip's digital current during TID testing.

3.6.4 Power of the IO Circuits

The power of the IO circuits does not seem to be influenced by the radiation, since no effect is visible (See Figure 25 left). The difference in power and current noise between locations is again visible (See Figure 25 right & Figure 26 right). There does not seem to be a radiation effect on the IO power.

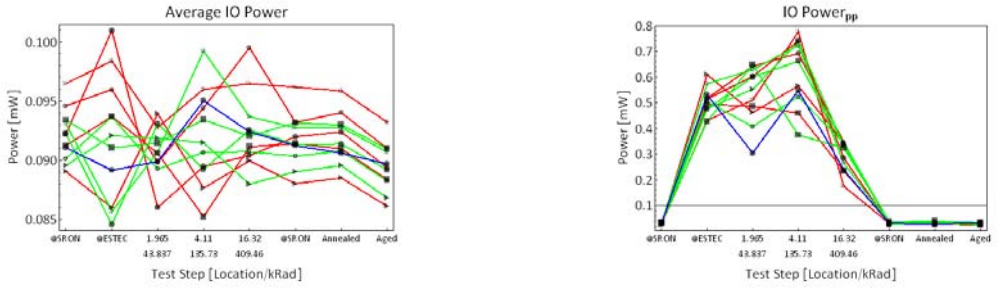

Figure 25: Average power (left) & peak-to-peak power noise (right) of the ADC chip's IO circuits during TID testing.

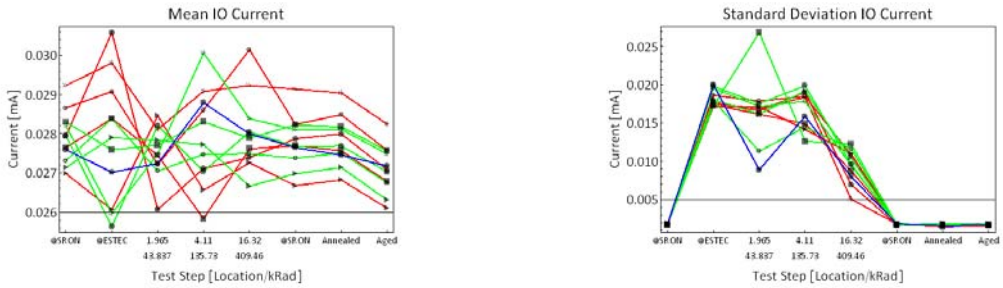

Figure 26: Mean (left) & standard deviation (right) of the ADC chip's IO current during TID testing.

4 Requirement Overview

Table 3 shows the radiation effects on the ADC requirements at 6.2kRad and when it fails for as far as the information has been measured.

Table 3: Radiation effect requirement matrix for the ADC sub-block.

Requirement	Description	@6.2kRad	Fails @ (kRad)
SHAMROC-0110	Increase of power consumption when TID is reached (10%)	Negligible	Somewhere between 136 and 409 kRad.
SHAMROC-0290	Differential Input voltage range	at least ±1.25V, but not tested.	Not tested.
SHAMROC-0300	Common mode input voltage	Not influenced by radiation	
SHAMROC-0310	Input referred noise level above 0.1Hz(1LSB)	10 LSB	Does not seem to be influenced by radiation.
SHAMROC-0320	Input referred noise level at 1mHz	Not tested!	
SHAMROC-0330	Input referred noise level at 10uHz	Not tested!	
SHAMROC-0340	Differential input resistance	Not tested!	
SHAMROC-0350	Differential input capacitance	Not tested!	
SHAMROC-0360	Common mode input resistance	Not tested!	
SHAMROC-0370	Power supply rejection ratio	Not tested!	
SHAMROC-0380	Common mode rejection ratio	Not tested!	
SHAMROC-0390	Pass-band input signal	Not tested!	
SHAMROC-0400	Settling time	Not tested!	
SHAMROC-0410	Dynamic Range	Not tested!	
SHAMROC-0420	Linearity error	Not tested!	
SHAMROC-0430	Gain error (1% Max)	0.03%	Between 136-409kRad
SHAMROC-0440	Offset (500 LSB Max)	10LSB	Between 136-409kRad
SHAMROC-0450	Temperature stability offset	Not tested!	
SHAMROC-0451	Temperature stability gain	Not tested!	
SHAMROC-0460	Reference voltage(1V)	1V	No upper or lower limit defined!
SHAMROC-0470	Power consumption analog part (5mW)	4.2mW	Between 136-409kRad
SHAMROC-0480	Jitter tolerance	Not tested!	
SHAMROC-0490	Power consumption in power down	Not tested!	
SHAMROC-0500	Startup time	Not tested!	

A lot of the requirements are have the label 'Not tested!'. This is because the tests performed here on the total ADC, have been limited due to limited test time. I would like to recommend another strategy so that there is still a way to evaluate these other specifications. In the next phase of the development, and even in other ASIC projects for space inside SRON, a process control module for radiation could be developed and added to the processed designs. In regular IC processing a process control module (PCM) is added several times to every wafer which is processed. This module consists of several test structures which when measured shows the systematic deviation of the structures for this particular wafer. Structures could be resistor, capacitors, transistors etc. A similar module could be added to each wafer, and not only measured after processing, but also during radiation testing. Such a module could provide information about the radiation effect on the basic building blocks of the design. This information can then be used to predict the influence of radiation on a variety of design requirements. When this module becomes a standard module for future designs in future IC processes, then a figure of merit can be generated for the radiation hardness of IC processes, and the IC processes can be compared. Once such a module is developed together with a measurement setup for the module, it will be relatively simple to add this to each future design without much additional costs.

5 Conclusion & Recommendations

5.1 Conclusion

General conclusion:
There is no indication that TID radiation will be a problem for the functioning within specifications of the ADC on the SHAMROC ASIC with the specified radiation level of 6.2kRad.
For the measured requirements, the ADC meets the requirements at least up-to 136kRad.

This conclusion is based on the following sub-conclusions:
ADC functional conclusions:

- The radiation effect on the offset is limited to 10LSB drift for the low-dose devices, which is well inside the 500 LSB requirement.
- For high-dose devices the radiation effect is limited to 30LSB up-to 136kRad, still well inside the 500LSB requirement.
- Somewhere between 136 and 409kRad the device offset fails the 500 LSB requirement.
- Without the offset reducing choppers the ADC offset drift due to radiation is as large as 1500LSB, while the offset itself is as high as up-to 10000LSB. Choppers thus need to be switched on for both the offset reduction as well as offset drift reduction.
- Annealing and accelerated ageing effects the ADC offset with the choppers off by up-to 280LSB for the low-dose devices.
- Activation of the VI chopper reduced the TID induces ADC offset drift from 1500LSB to approximately 250LSB.
- Activation of the common-mode choppers reduce some offsets and worsens others. The radiation induced offset drift is in the same order as without choppers activated.
- The ADC gain increased approximately 0.03% at 6.2kRad of Total Ionizing Dose. At 135kRad the ADC gain increase is about 0.12%. Both increases fall well inside the gain error requirement of 1%.
- Accelerated ageing induces an increase in gain of about 0.3%. Also this gain drift is within the 1% gain error requirement. It can however not be concluded whether this increase is caused by the combination with irradiation or only ageing effects.
- No TID radiation effects were observed on the ADC white noise measurements. Also the 1/f-noise measure with the VI chopper off shows no increase after irradiation.
- No TID radiation effects were observed on the harmonic distortion measurements, other than when device is no longer functioning at 409kRad irradiation.
- At 409kRad the devices are no longer functioning, so somewhere between 136 and 409kRad the device will fail the requirements.
- When the devices fail the bitstream output of the analog electronics is either stuck to 0 or stuck to 1.

ADC power consumption and temperature conclusions:

- The low-dose devices are not showing any radiation effect on the total power consumption.
- The total power consumption of the high-dose devices show no significant change up to 44kRad, and stay within specification (10% increase) up-to at least 136kRad.
- The high-dose devices are showing a slight power increase of about 0.2mW (3.3%) at 136kRad, and a huge power increase of about 2.4mW (39%) at 409kRad when the devices are not longer functional.
- The total power increase at the high-dose devices is due to an analog power increase.
- Accelerated ageing seems to anneal the high-dose devices somewhat, since analog power is restored to the 136kRad level.
- Accelerated ageing restores some functionality of the high-dose devices, but the performance is still generously out of specifications.

- There is a small decrease in digital power of 0.04mW in four out of five high dose devices at 409kRad. The most likely cause of this digital power decrease is the bitstream of the analog circuits which clips to V_{dd} for the four devices with decreased power. The fifth high-dose device, which does not show a decreased digital power, fails with an analog bitstream output at V_{ss}.
- There is no TID radiation effect on the IO power and IO current.
- The reference voltage drops up-to 2mV for the high-dose devices at 409kRad. Annealing and accelerated ageing repairs this effect.
- There does not seem to be a correlation between temperature and radiation level.

5.2 Recommendations

The current setup uses one reference device to separate effects seen in the measurements from changes of the measurement setup or its environment. A second reference device which is not irradiated, but is annealed and acceleratedly aged, could separate the effect of annealing radiation damage from natural ageing effects related to the technology.

The noise on the power readings is higher for measurements at ESTEC compared to the measurements at SRON. Measure the grid power supply noise during the measurements so that the noise on the measurements can be explained. If the power grid is providing extra noise to the measurements then stabilizing the grid power or using battery operated measurement setup could reduce the noise in the measurements. This will improve the confidence of the conclusions during the more extensive TID test during space qualifications.

I would like to recommend a process control module for radiation to be added to the processed designs. This module would consist of several test structures such as resistors, capacitors, and transistors etc. It would not only be measured after processing, but also during radiation testing. Such a module could provide information about the radiation effect on the basic building blocks of the design. This information can then be used to predict the influence of radiation on a variety of design requirements. As a standard module for future designs in future IC processes, it will provide a figure of merit for the radiation hardness of IC processes, and the IC processes can be compared.

Acknowledgements

SRON and Xensor would like to acknowledge Bob Nickson at ESA/ESTEC for his help and input for this TID setup.