Test Report:

Total Ionisation Dose (TID - Co-60) Test with the First Magnetometer Front-end ASIC (MFA-1)

Revision List

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Related Documents

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Test procedure: IWF-MFA-TP-TID-002
Test report: IWF-MFA-TR-001_I1R2_TID1

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1 Abstract

A first version of a Magnetometer Front-end ASIC (MFA), which is used as near-sensor electronics with direct digital output for a fluxgate sensor, has been jointly developed by the Institut für Weltraumforschung (IWF) of the Austrian Academy of Sciences in Graz and the Fraunhofer Institute of Integrated Circuits (Fraunhofer IIS) in Erlangen, Germany under the ESA/ESTEC contract no. 18391/04/NL/HB.
The development is based on a combination of the conventional fluxgate magnetometer readout electronics with the control loop of a sigma-delta (SD) modulator in order to achieve a further miniaturized, robust (especially in terms of radiation hardness) and highly sensitive triaxial magnetometer electronics that provides direct digital output without the use of a separate analog-to-digital converter chip. It is aimed for a reduction of the power consumption of the readout electronics part from 500 mW to 50 mW and to achieve radiation hardness (total ionizing dose) of more than 100 krad. The chip contains altogether four sigma-delta analog-to-digital converter channels. Three of which are modified for reading out the magnetic field information from the fluxgate sensor and the fourth one is used in combination with a multiplexer for digitising up to eight housekeeping channels.
The radiation sensitivity to Total Ionization Dose (TID) of the MFA chip, which was produced on an Austriamicrosystems (AMS) 0.35 µm CMOS multi-project wafer process, was evaluated by using the radiation test facility of ESA's European Space and Technology Centre (ESTEC) in Noordwijk, Netherlands in November 2005.
Altogether four MFA chips of the same lot were tested during three consecutive total dose irradiation cycles. One chip (MFA104) was tested up to 261.5 krad at a dose rate of about 93 rad/min and the second one (MFA112) up to 225.3 krad at a lower dose rate of about 56 rad/min. The third one (MFA102) as well as the fourth one (MFA109) were tested up to 129.4 krad and 88.6 krad, respectively.
All chips showed full functionality in terms of command ability, data transmission as well as modulator and test bus operation throughout the entire test run as well as after the irradiation. The check-out of the MFA102 and MFA112 chips was adversely affected during the first test cycle because some of the chip surrounding digital driver ICs failed due to the remaining irradiation behind the shielding blocks.
An increase of the supply current on the 3.3 V digital supply as well as a decrease of the Signal-to-Noise and Distortion Ratio (SNDR) was measured for all four devices under test.

2 System Design Overview

The system design, see the block diagram in Figure 1, can be divided into the analog (design responsibility by Fraunhofer IIS) and the digital part (design responsibility by IWF). The combined parts were finally placed and routed by Fraunhofer IIS.
The analog part consists of three 2-2 cascaded sigma-delta fluxgate modulators plus one standard 2-2 cascaded modulator which is connected to the output of an eight-to-one multiplexer for housekeeping measurements. The fluxgate modulators are normally connected to the external fluxgate sensor via the input amplifiers and the feedback circuits of the first of altogether two internal second-order delta-sigma modulators per fluxgate channel. The two single-bit outputs of the second-order modulators are again connected to the error cancellation (EC) logic for generating a fourth-order noise shaped and digitized output signal with 6-bit data width and a sampling rate of 6144 Hz.
The chip is supplied by two separate analog and digital 3.3 V supply voltages.

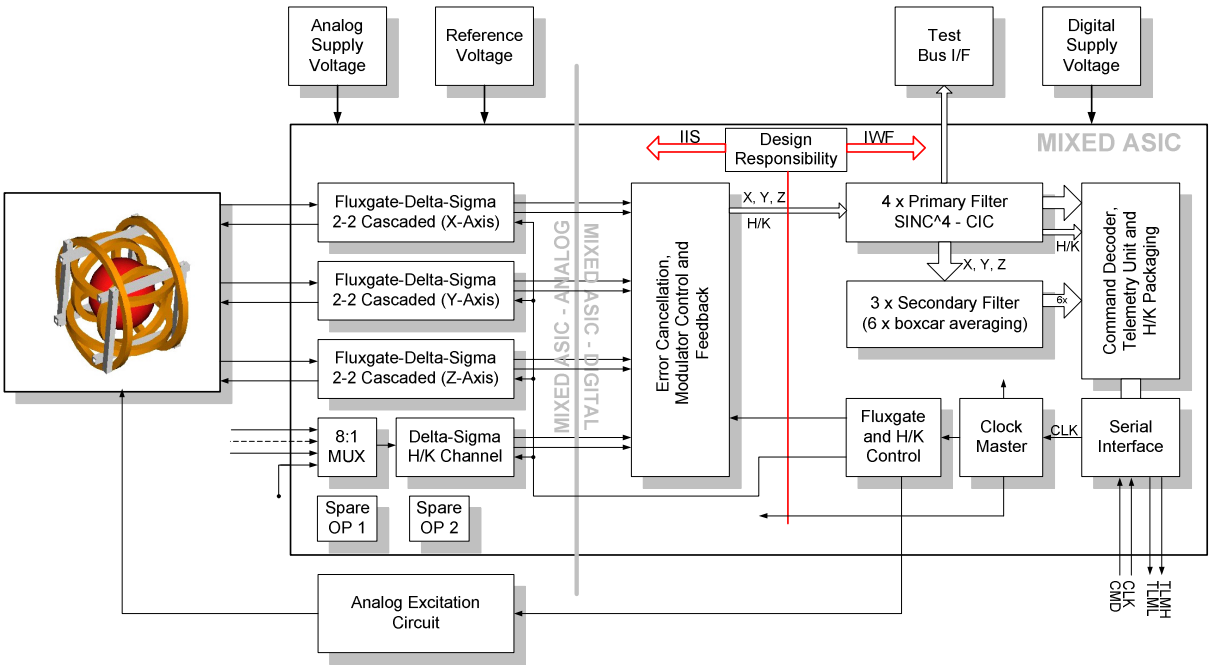

Figure 1: Top level block diagram of the MFA

The digital part includes data processing in the primary and secondary decimation filter blocks, a serial synchronous interface as well as the generation of all necessary control signals for the fluxgate part of the modulators and the digital part itself. The magnetic field and housekeeping data from the sensor and the chip are primarily transmitted with 24-bit data width via the serial synchronous interface. An additional 8-bit test bus provides a separate check-out functionality of the single-bit outputs of the two cascaded second-order modulators as well as the 6-bit output of the error cancellation logic (i.e. the raw data of the sigma-delta modulation) which is also fed to the primary decimation filter within the chip. The test bus therefore provides a good failure separation between the digital and analog part of the chip. Since the MFA has two telemetry lines (TLM-High and TLM-Low) the EC data are decimated by 64 (primary filter) down to 96 Hz in 6 steps for the TLML output.
Apart from the fluxgate mode described above, the fluxgate channels of the MFA can also be operated like standard Analog-to-Digital Converter (ADC) channels with 96 Hz output data rate, ±2.5 V analog input range and 24-bit width of the digital output (which is not the accuracy of the conversion). In this case no fluxgate sensor is used and the feedback lines are connected to the pre-amplifier.

3 Device Information

The basic device information is summarised in the table below:

SCC Component No.	N/A
Component Designation	Readout electronics of a fluxgate sensor based on a 2-2 cascaded sigma-delta converter
Specification	N/A
Acceptance	N/A
Sample Size	Core: 3 x 4.5 mm; total: 3.7 x 5.2 mm
Number of samples	20
Project	Technical assistance in the development of an application-specific integrated circuit (ASIC) for a planetary magnetometer ESTEC/Contract No. 18391/04/NL/HB
Family	Fluxgate magnetometer / analog-to-digital converter
Group	sigma-delta
Package	CQFP100 (Ceramic Quad Flat Package)
Manufacturer Name	Austriamicrosystems (AMS)
Manufacturer Address	Austriamicrosystems AG Schloss Premstätten 8141 Premstätten AUSTRIA
Test House Name	Radiation Effects and Component Analysis Techniques Section, European Space and Technology Centre (ESTEC)
Test House Address	ESA/ESTEC Noordwijk Netherlands
Originator Name	Institut für Weltraumforschung (OeAW) Fraunhofer Institut für Integrierte Schaltungen (Fraunhofer IIS)
Originator Telephone	+43 316 4120 566
Facility	TID Facility
Source	Co-60 (Energy 1.173 & 1.332 MeV photons)
Irradiation	Three cycles
Dose rate	93 and 56 rad/min
Level of Interest	> 100 krad
Irradiation Conditions	see Table 4 to Table 7

Table 1: Device information

4 Test Configuration

Two test boards were used during the test campaign. One of which was set up in the so-called voltage board mode (see also Chapter 3). The other one was run in a very limited set-up (housekeeping board) so that only the differential housekeeping channel could be read-out and checked via the test bus. The test configuration is shown in the block diagram of Figure 2 and in the picture of Figure 3.

4.1 Voltage Board

The upper part of Figure 2 shows the voltage board carrying the device under test (MFA chip) including some digital line drivers for the control and data transfer between the 1-2 meter long distance between the MFA and the Electrical Ground Support Equipment (EGSE).
The MFA as Device Under Test (DUT) is located more or less in the middle of the Printed Circuit Board (PCB). The additionally needed electronics is placed in a safe distance around the MFA to allow sufficient shielding by graphite blocks (size of one block: 20x10x5 cm).
The EGSE itself generates the master clock (CLK) of 3.145728 MHz, all power supply voltages, it handles the data communication with the MFA via the serial synchronous interface and it also measures the supply currents of all supply voltages at a rate of one Hz (without a strict anti-aliasing strategy). It is powered with a 12 V supply voltage. A complete list of the connection lines between MFA and EGSE is given in Table 2 here below.

Signal	Description
CLK	Clock to MFA
CMD	Command to MFA
TLMH	Telemetry high from MFA
TLML	Telemetry low from MFA
+3V3A	VDDA supply voltage of the MFA
+3V3D	VDDD supply voltage of the MFA
+5VD	Line drivers and other circuits
+8VA	External pre-amplifier and other circuits
-8VA	External pre-amplifier and other circuits
AGND	Analog ground
DGND	Digital ground

Table 2: Signals between EGSE and MFA test board

The EGSE again is connected to a host PC, which is located outside of the radiation chamber, via an RS-232 interface where the measured data could be graphically displayed and recorded. With the MFA software and a graphical input mask all possible instrument commands could be transmitted to the MFA. With this connection the correct commanding and data transmission of the MFA as well as of all housekeeping parameter was tested during the irradiation test.
The MFA on the voltage board was additionally checked by a second monitoring system built by the data converter (Data Aqu.) and the second host PC connected to the test bus in the block diagram. It allows the monitoring and storing of the 8-bit test bus containing the single-bit outputs of each of the two second-order modulators as well as the 6-bit error cancellation output. But only one of the four channels could be tested at the same time, which is the reason why only the housekeeping channel was read-out via this test channel by measuring the SNDR with the help of a permanently applied sine wave during the radiation test.

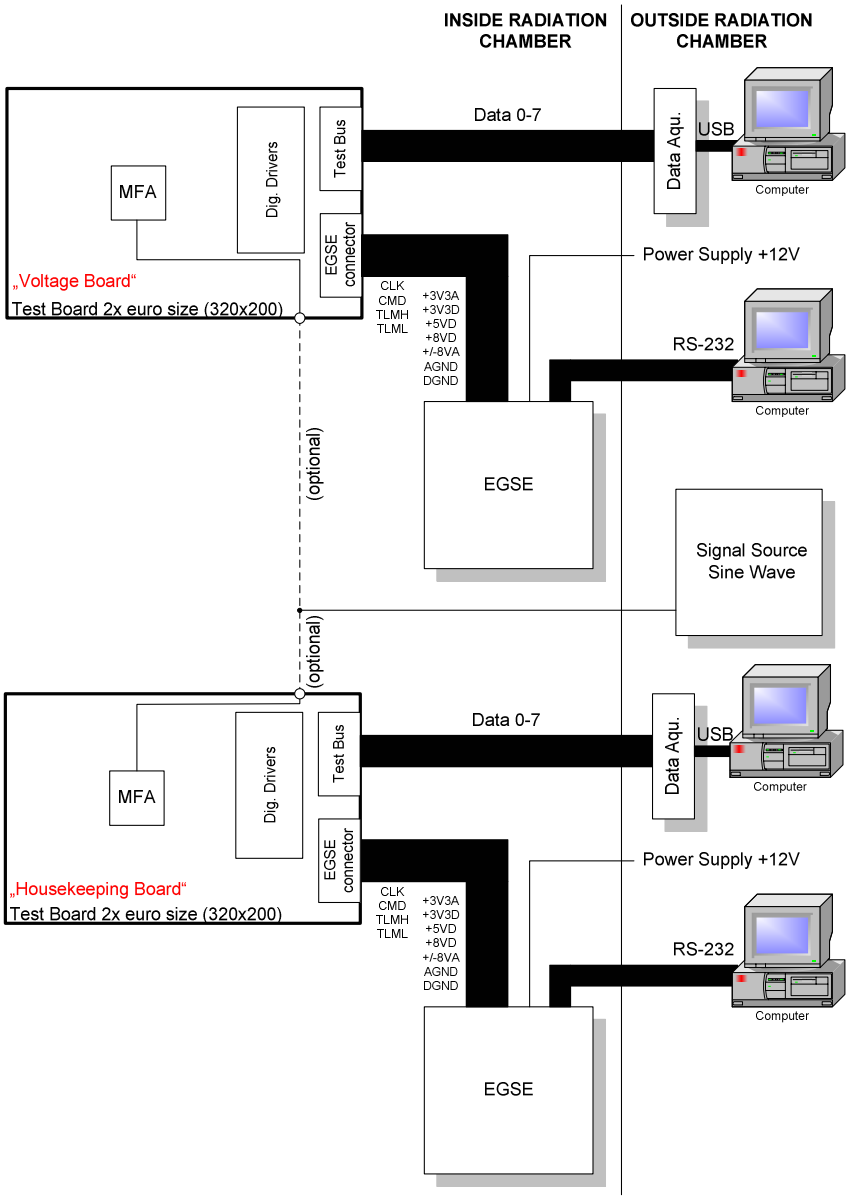

Figure 2: Test configuration

A maximum SNDR of 92 dB had been measured under laboratory conditions on the housekeeping channel and with the MFA on the housekeeping board before the test campaign. Due to several reasons – several meters of power and signal supply cables, the neighbouring placement of the two test boards, grounding issues etc. – the maximum SNDR measured during the irradiation campaign was 76 dB.

4.2 Housekeeping Board

The housekeeping and the voltage board are based on the same Printed Circuit Board (PCB). The difference between the two boards lies in the fact that the housekeeping board has been equipped with only a limited number of additional components, so that only the differential channel of the housekeeping modulator was fully operated.
The housekeeping board is also connected to a second EGSE. During the first test cycle the EGSE was only used for the power supply and the measurement of the supply currents. In

this configuration a precise on-board oscillator with 3.145728 MHz was used as clock generator.
During cycle 2 and 3 the set-up was changed by using the clock signal from the EGSE, so that also the synchronous interface was in operation which allowed the commanding of the chip and the check and storage of the transmitted data.
The way of checking the SNDR of the housekeeping channel was the same as for the voltage board.

4.3 Measurement Set-up and Procedure

A photo of the general measurement set-up is shown in Figure 3. On the right hand side one can see the aperture of the Co-60 radiation source. The two test boards, voltage and housekeeping board, are placed in front of the opening window in an approx. 44 cm and 52 cm distance. With the source activity of 1179.95 Ci (43.7 TBq), the two dosimeters probes carried by the aluminium clamps registered between 90 (cycle 3) and 107 $rad_{(Si)}$/min (cycle 1) for the “closer” board and between 56 and 65 $rad_{(Si)}$/min for the board being located in the further distant position. The grey graphite blocks are very important for the shielding of the chip surrounding electronics. As will be shown in the test results, the insufficient shielding of drivers and oscillators caused some troubles especially during the first irradiation cycle.
All cables which connected either the test boards or the EGSE with the test equipment outside of the radiation chamber were necessarily at least 7 m long.
All currents of the voltage supplies for the test boards were monitored by the EGSEs and stored by the measurement PCs. The EGSEs themselves were connected to the test boards by a 1 m long cable and heavily shielded with graphite blocks. It was deposited outside the irradiation direction below the test boards.

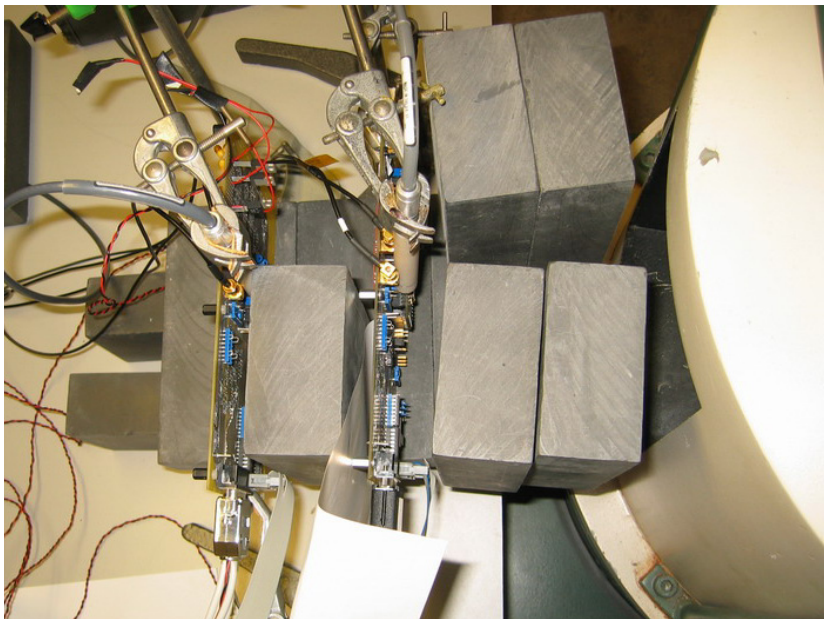

Figure 3: Set-up of the test boards during the first test cycle

The MFA dosimeter position of the closer test board with the therefore higher dose rate is depicted in Figure 4.

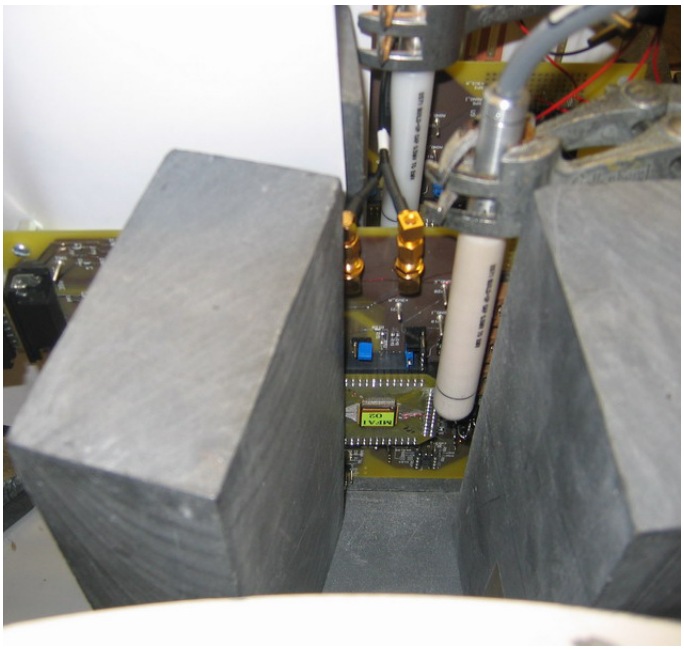

Figure 4: Adapter board of the MFA with the dosimeter above it

The MFA chip contains altogether four ADC channels (three fluxgate channels and one pure ADC channel with an 8-1 multiplexer in front), whereas the pure ADC channel was used for the SNDR performance evaluation with sine wave input during irradiation and the fluxgate channels, wired as standard sigma-delta ADC channels, were short circuited.
Altogether four MFA chips of the same lot were tested during three consecutive total dose irradiation cycles. A brief overview of the test cycles and the maximum radiation levels is given in the table below. All details about test conditions and results are outlined in the following chapter.

Device Name	Test Cycle	Test Board	Type of Operation	Max. Radiation Level	Comment
MFA102	1	voltage	biased	129.4 $krad_{(Si)}$	driver problems
MFA104	2	voltage	biased	261.5 $krad_{(Si)}$	higher dose rate
MFA112	1	housekeeping	biased	81.0 $krad_{(Si)}$	lower dose rate
	2	housekeeping	biased	144.2 $krad_{(Si)}$	lower dose rate
MFA109	3	housekeeping	biased	88.6 $krad_{(Si)}$	spec. SNDR test

Table 3: Overview of the test cycles

5 Test Results

5.1 MFA104

The MFA104 chip was irradiated up to a maximum TID level of 261.5 krad during cycle 2 (more than 46 hours of irradiation). All test details are summarised in the table below.

Type of test board	Voltage board
Device name	MFA104
Operating condition	biased
Chip parameters checked	Supply currents of +3V3A and +3V3D; Chip command ability, data transmission and status bits; Functionality of test bus; Continuous meas. of short circuited Y-axis; SNDR of H/K channel 0;
Board parameters checked	Supply currents of +5VD, +/-8VA and +8VD
Total ionization dose	261,5 $krad_{(Si)}$ (cycle 2)
Dose rate	93.5 $rad_{(Si)}$/min
Duration of irradiation	~46.6 hours (cycle 2)
Distance to source	~44 cm
Sample temp.	20°C (+/-1°C)
MFA condition	CLK and power supply provided by EGSE; X- and Z-axes not operational; Y-axis short circuited at ext. fully diff. preamp (THM4131); Sine wave applied to HK-channel 0 for SNDR measurements: 10 Hz/2Vpp differential;

Table 4: Summary of TID test with MFA104

Analog and Digital Power Consumption of the MFA104

The analog supply current of approximately 10 mA (see Figure 5) and thus also the analog power consumption of the MFA104 remained constant over the 261 krad.
The digital power consumption increased by 61 % what was expected for the CMOS process. The mean supply current measured in Figure 6 increased from 2.55 mA at the beginning to 4.13 mA at the end of test cycle 2 .

Digital Power Consumption of the Test Board

Figure 7 shows the supply current of the digital drivers used between the MFA and the "outside world". It is an important indicator for the health status of the components around the chip. The current curve progression in general is typical for CMOS devices but there hasn't been any explanation found for the very low frequency ripple (period 1.25 h) which decreases over the measurement. A significant jump occurred at 260 krad which had no influence on the data transmission from the MFA to the EGSE and the PC, respectively, which sampled the test bus output data.

Short Circuited Y-Axis

Figure 8 shows the 1.5 Hz low telemetry output of the short circuited Y-axis. The plot confirms – apart from the spike at about 20 krad – that the MFA104 chip (including 2-2 cascaded modulator, error cancellation, primary and secondary filter as well as low telemetry data transmission) nominal functionality during the complete test cycle.
The standard deviation calculated over approx. 1.1 minutes of data (100 data points) is in the order of 60 μV_{rms} (see also Figure 9) which corresponds to a theoretical maximum SNDR of 83.4 dB for the bandwidth from 0.015 to 0.75 Hz which is lower than under normal laboratory conditions. The offset of about 17 mV is as expected. No explanation was found for the 2.2 mV drift between 180 and 210 krad.

The standard deviation in Figure 9 shows a jump from 49 µV to 57 µV at about 10 krad. During the rest of the test cycle it slightly increases up 64 µV.

SNDR of the Differential Housekeeping (H/K) Channel

The Signal-to-Noise and Distortion Ratio (SNDR) calculation was done directly from the H/K sigma-delta modulator data gained via the test bus (Figure 10). It shows a linear decrease of about 10 dB from 72 dB down to about 62 dB (0.038 dB/krad; see also Chapter 4.1). A data gap which occurred during the first test night due to a crash of the data acquisition software on the host PC was linearly interpolated.

The increase of the noise floor in the signal band-width by a factor 3-4 is also depicted in Figure 11. The red curve shows the power spectral density of the error cancellation output at the beginning of the MFA104 irradiation and the blue curve at the end: the noise floor between 20 and 80 Hz increases from about 15 to about 65 µV/√Hz (FS in the plot corresponds with 0.884 Vrms), the fundamental sine of 10 Hz as well as its third harmonic at 30 Hz stay unchanged and all the other disturbing harmonics become larger with a similar ration as the noise floor described before.

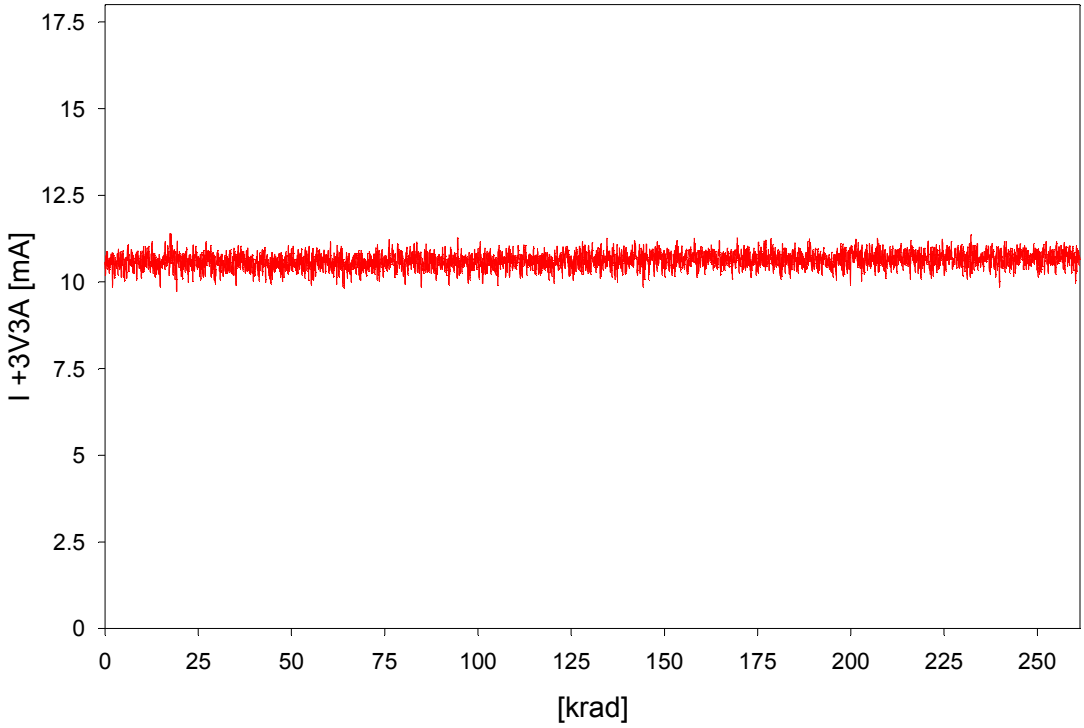

Figure 5: Analog supply current of the MFA104 (3.3 V analog)

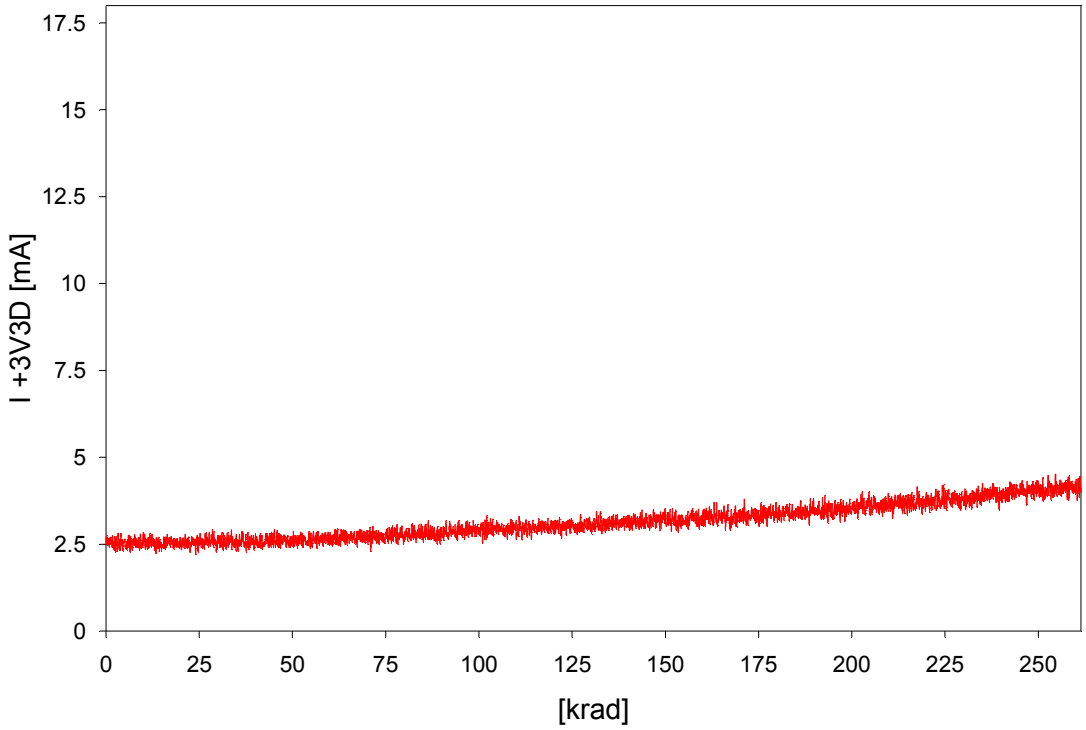

Figure 6: Digital supply current of the MFA104 (3.3 V digital)

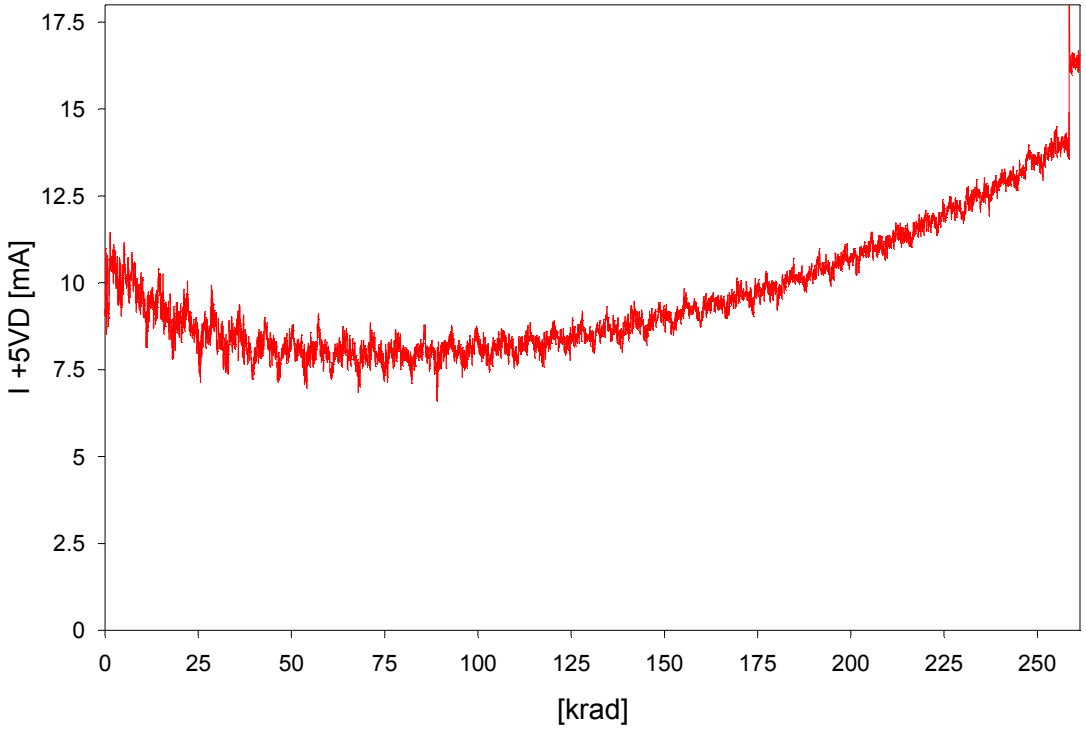

Figure 7: Digital supply current of the test board (5 V digital)

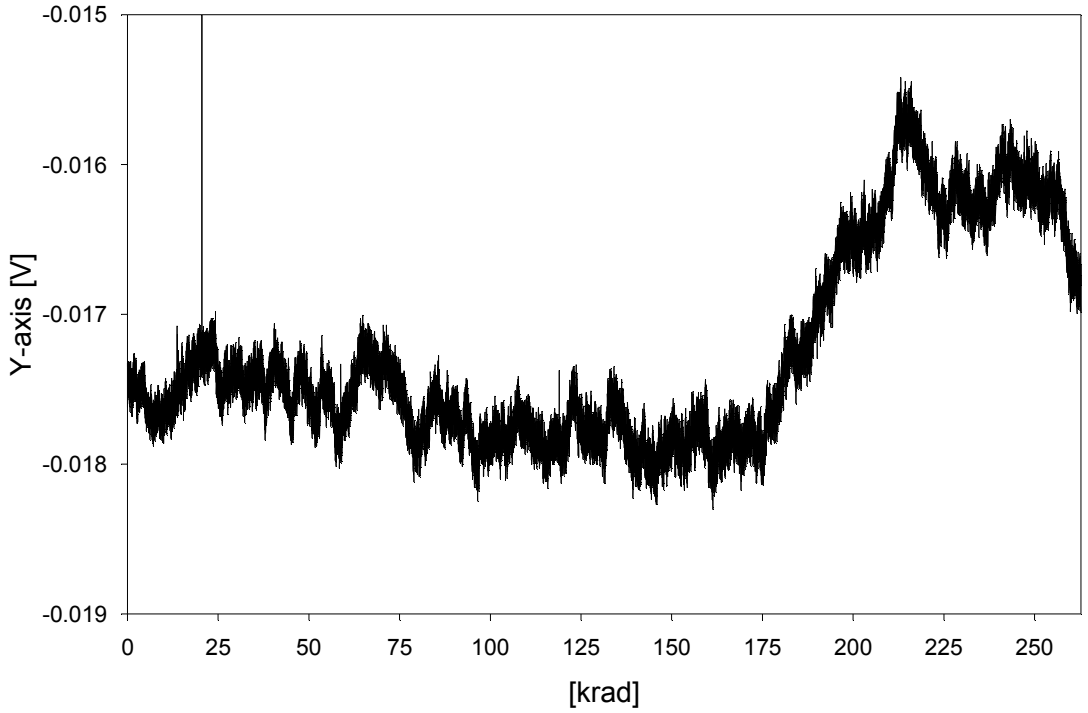

Figure 8: Low telemetry (1.5 Hz) output of the short circuited Y-axis

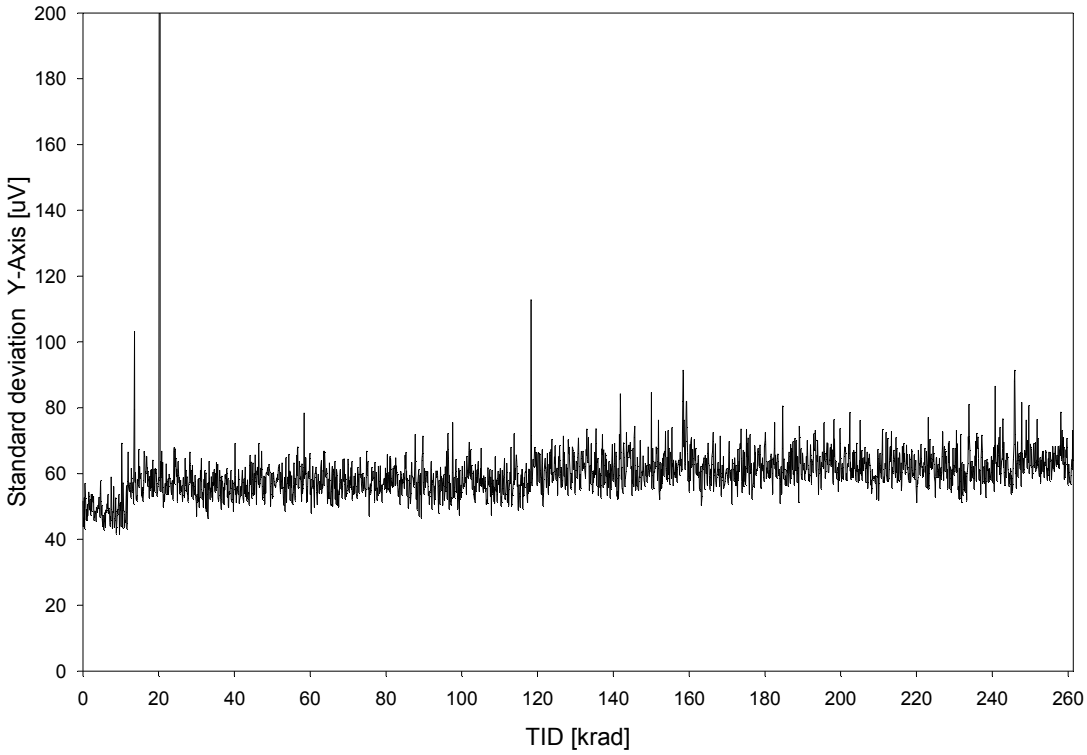

Figure 9: Standard deviation (100 data points) of the Y-axis output in the figure above

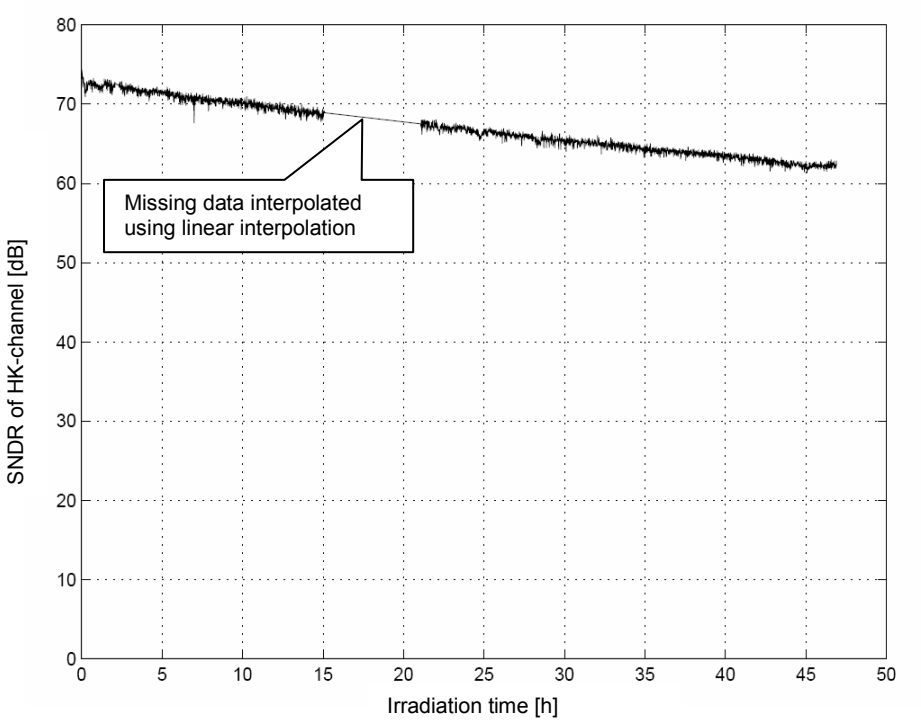

Figure 10: SNDR of the differential housekeeping channel

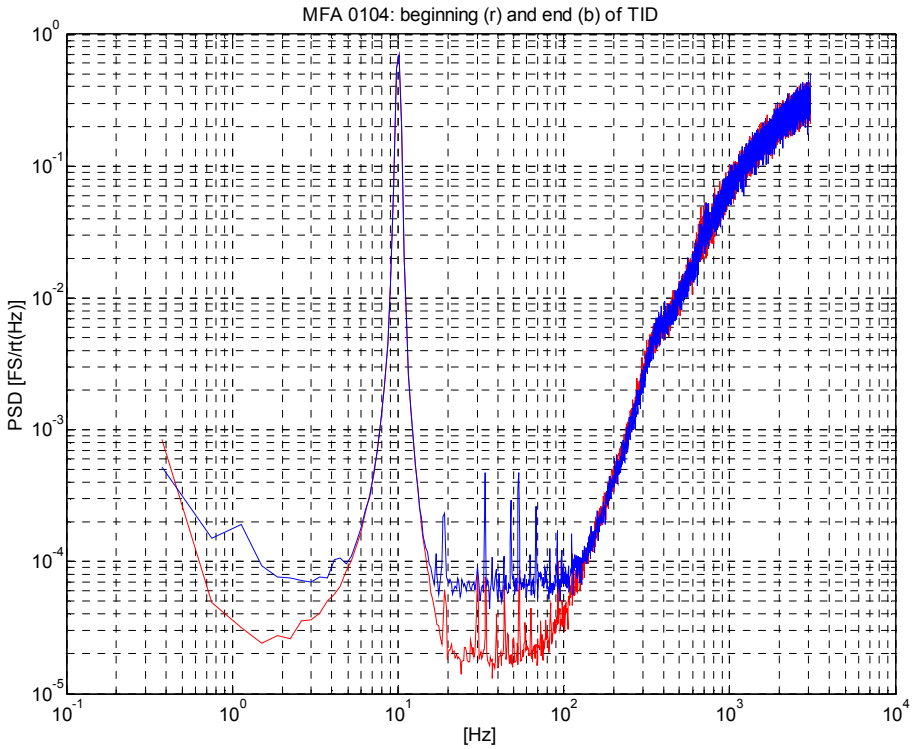

Figure 11 Power spectral density of the diff. H/K channel: beginning (red) and end (blue) of 261.5 krad test

5.2 MFA112

During cycle 1 testing of the MFA112 several problems were caused by on-board circuits (not on-chip!) like oscillator and line drivers, which failed due to the remaining radiation behind the shielding blocks, as well as by a not properly plugged connector at the differential housekeeping channel (supply of the 10 Hz sine). A summary of the test conditions is given in the table below.

Type of test board	Housekeeping board
Device name	MFA112
Operating condition	biased
Chip parameters checked	Cycle 1: Supply currents of +3V3A and +3V3D; Functionality of test bus; SNDR of H/K channel 0; Cycle 2: Like cycle 1 plus chip command ability, data transmission and status bits;
Board parameters checked	Supply currents of +5VD, +/-8VA and +8VD
Total ionization dose	Cycle 1: 81.1 $krad_{(Si)}$ Cycle 2: 144.2 $krad_{(Si)}$ (irradiation pause of about 3 h before) Total: 225.3 $krad_{(Si)}$
Dose rate	Cycle 1: ~65 $rad_{(Si)}$/min Cycle 2: ~56 $rad_{(Si)}$/min
Duration of irradiation	Cycle 1: ~20.2 hours Cycle 2: ~46.6 hours Total: ~66,8 hours
Distance to source	~54 cm
Sample Temp.	20°C (+/-1°C)
MFA condition	Cycle 1: CLK provided by on-board oscillator; Power supply provided by EGSE; X-, Y- and Z-axes not operational; Sine wave applied to HK-channel 0 for SNDR measurements: 10 Hz/2Vpp differential; Cycle 2: CLK and power supply provided by EGSE; Rest as for cycle 1;

Table 5 Summary of TID test with MFA112

Analog and Digital Power Consumption of the MFA

The analog supply current (upper plot of Figure 12) stayed constant during the test cycles. The non-operational fluxgate modulators were switched-on during cycle 1 and switched off during cycle 2 (with the CLK coming from the EGSE it was possible to command the chip), which is the reason for the jump from 9 to 5 mA in the supply current.
The digital supply current of the chip (lower plot of Figure 12) was also constant up to the failure of the on-board oscillator at approx. 65 krad. From that time until the end of test cycle 1, the digital supply current cannot easily be interpreted. During cycle 2, it is stable at about 2.5 mA (much less than in cycle one because no power consumption of the on-board oscillator; CLK comes from the EGSE).

Digital Power Consumption of the Test Board

Figure 13 presents the supply current of the digital drivers used between the MFA and the “outside world”. It clearly shows the failure of the on-board oscillator at 65 krad. The rest of

cycle 1 is again not meaningful. The low-frequency ripple (period of about 1.25 h) of the supply current is much bigger than it was measured with the voltage board of the MFA104 as well as the overall characteristics only shows a decrease of the current.

SNDR of the Differential Housekeeping (H/K) Channel

The SNDR measurement – directly from the H/K sigma-delta modulator – shows in general a linear decrease from 70 to 57 dB (0.058 dB/krad). It is even worse as for the MFA104 in Figure 10. Shortly after the start of cycle 1 a mechanical problem at the supply connector caused a drop of the SNDR to 10 dB. The problem was solved before the start of cycle 2 and the missing data can almost linearly be interpolated as during the SNDR measurement gap of MFA104 above.

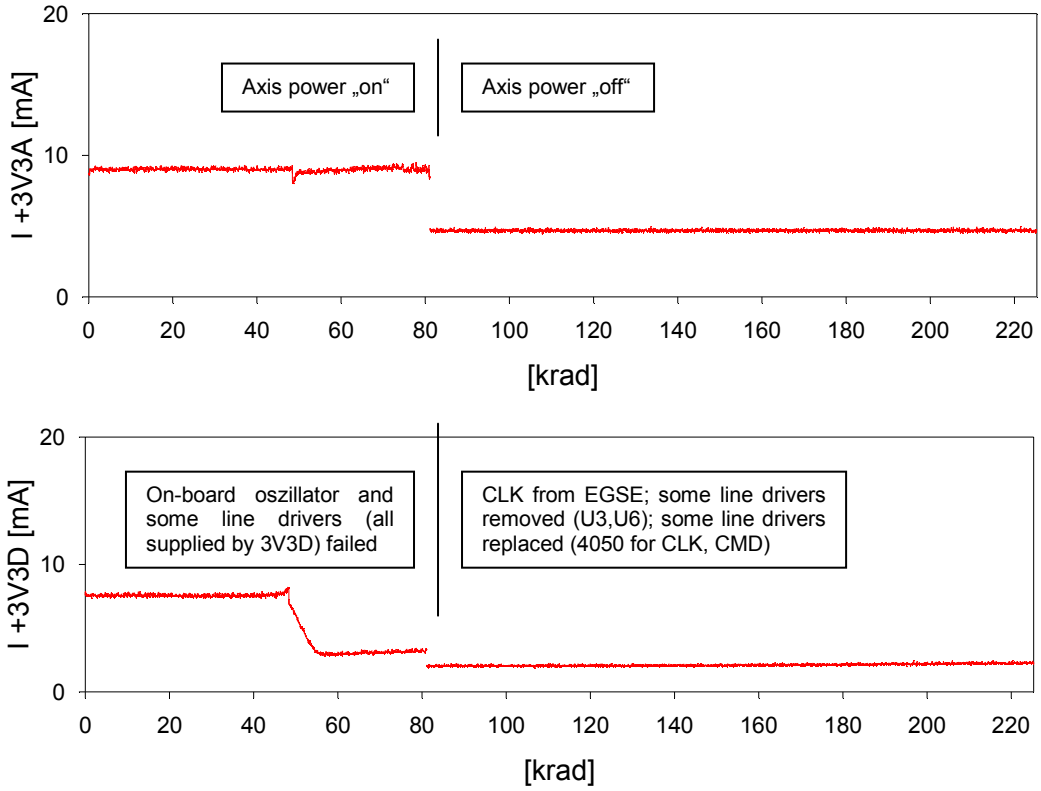

Figure 12: Digital (lower) and analog (lower) supply current of the MFA112

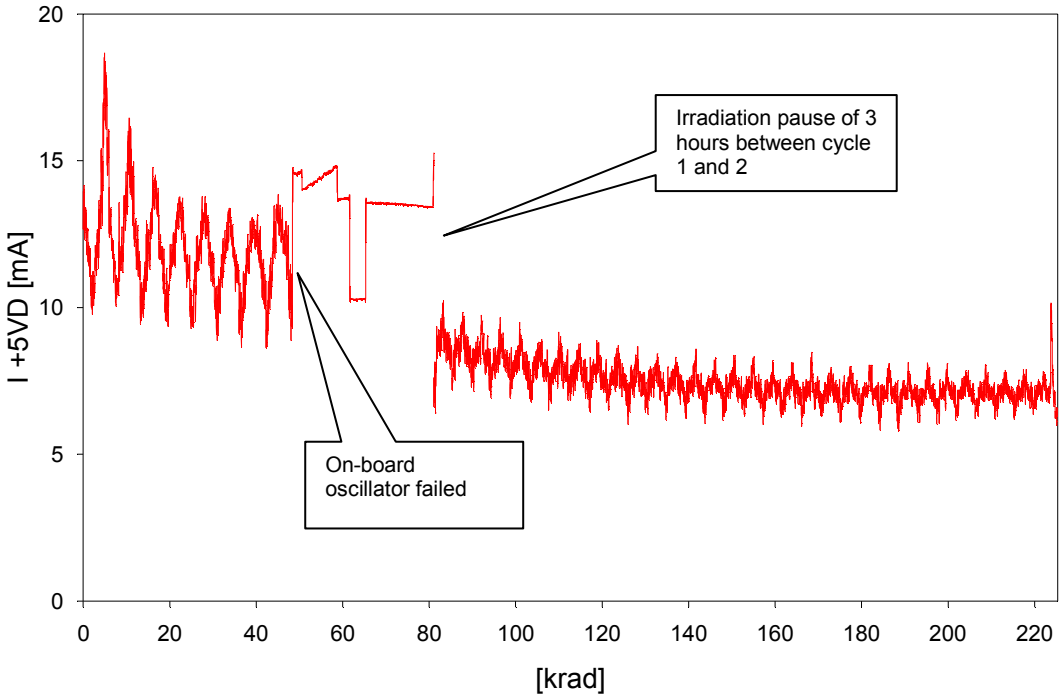

Figure 13: Digital supply current of the test board (5 V digital)

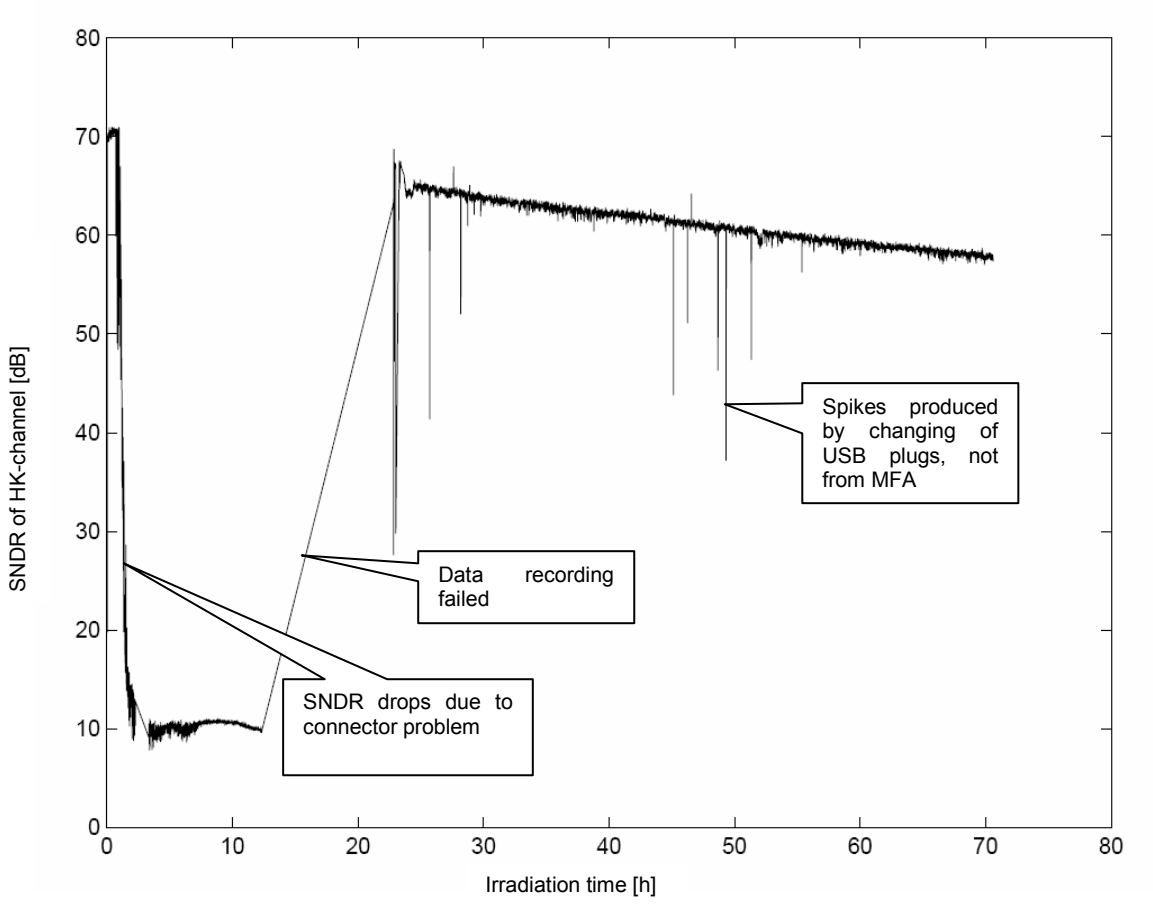

Figure 14: SNDR of the differential housekeeping channel

5.3 MFA109

Type of test board	Field board
Device name	MFA109
Operating condition	biased
Chip parameters checked	Supply currents of +3V3A and +3V3D; Chip command ability, data transmission and status bits; Functionality of test bus; SNDR of H/K channel 0;
Board parameters checked	Supply currents of +5VD, +/-8VA and +8VD
Total ionization dose	88.6 $krad_{(Si)}$ (cycle 3)
Dose rate	~90 $rad_{(Si)}$/min
Duration of irradiation	~16.2 hours
Distance to source	~45 cm
Sample Temp.	20°C (+/-1°C)
MFA condition	CLK and power supply provided by EGSE; X-, Y- and Z-axes not operational; Sine wave applied to HK-channel 0 for SNDR measurements: 10 Hz/2Vpp differential;

Table 6 Summary of TID test with MFA109

The test measurements during cycle 1 and 2 showed that the functionality of the MFA is not affected by a TID up to 261 krad in parallel with a moderate increase of the digital supply current and a significant decrease of the SNDR.
The aim of test cycle 3 was to find a set-up with a better start level of the SNDR by installing only one test board, changing the grounding of the test equipment etc.

Analog and Digital Power Consumption of the MFA109

The analog and digital supply currents are depicted in Figure 15 and Figure 16. The results basically reflect what had already been measured during cycle 1 and 2 with MFA104 and MFA112: analog supply current is not affected by the radiation and the digital supply current increases (0.2 %/krad).

SNDR of the Differential Housekeeping (H/K) Channel

The SNDR plot in Figure 17 again starts with a quite low level of 72 dB and a decreasing trend. After a while, the grounding of the test equipment was changed which increased the SNDR to 76 dB where it remained stable for about 3 hours and 16 krad of radiation. Then unfortunately the acquisition crashed again during night with a loss of the SNDR measurements for 11.5 hours. After a restart of the test equipment a drop of 2.5 dB was measured which is a 0.038 dB/krad linear decrease.

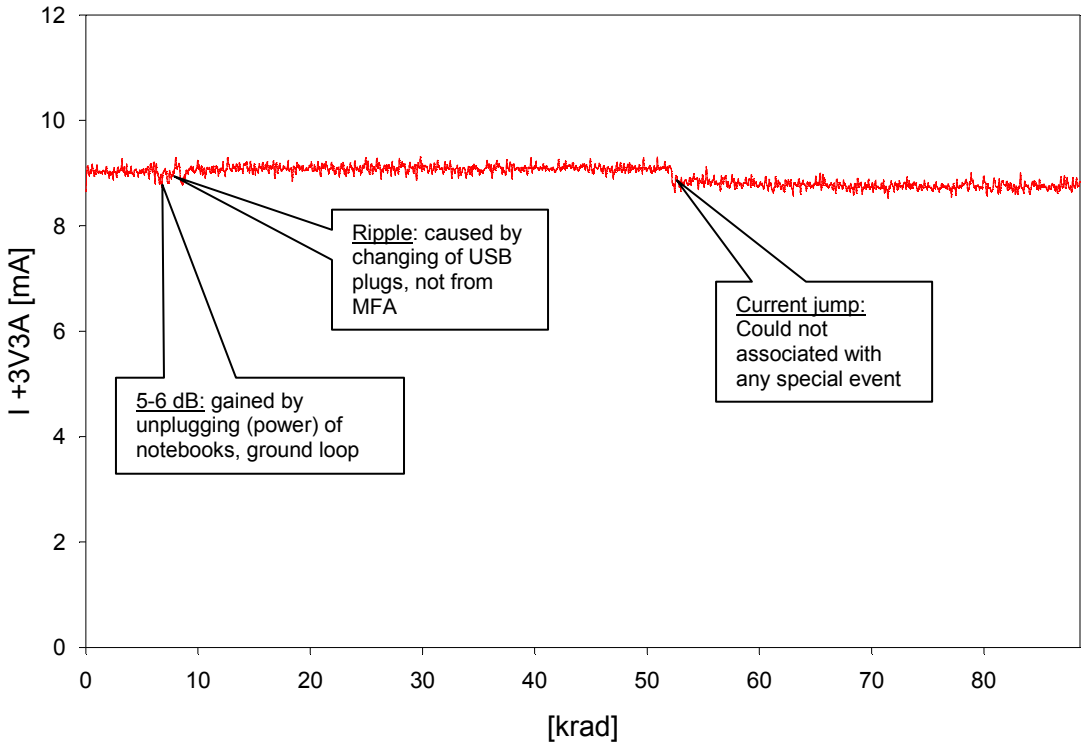

Figure 15 Analog supply current of the MFA109 (3.3 V analog)

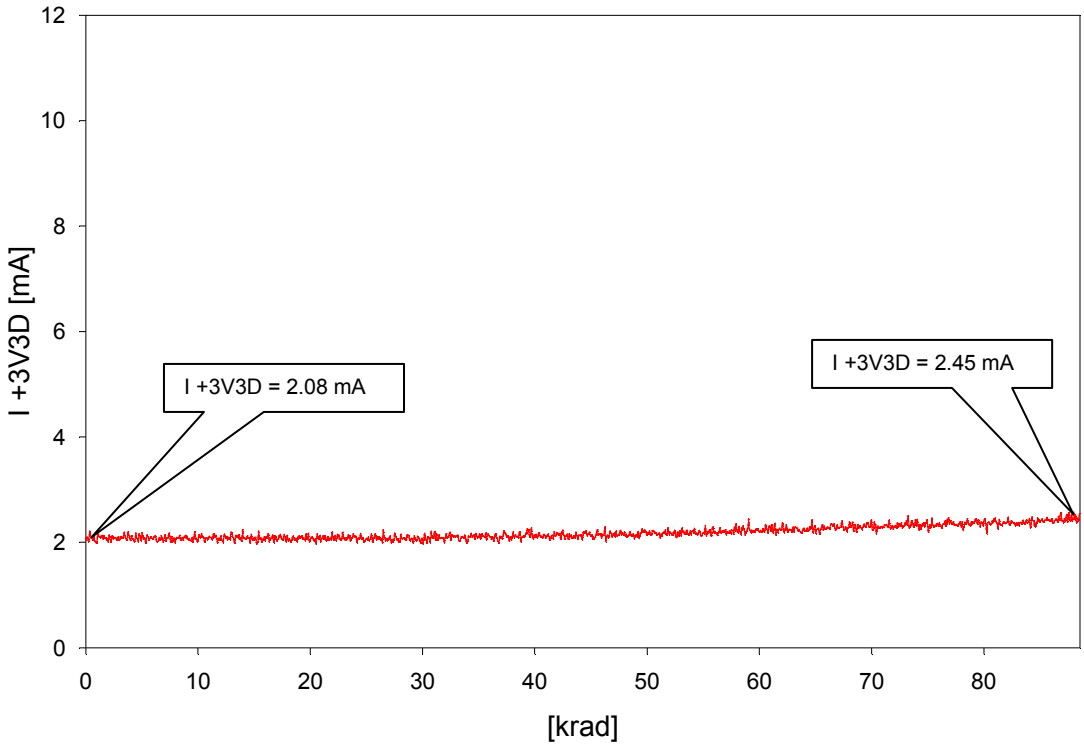

Figure 16 Digital supply current of the MFA109 (3.3 V digital)

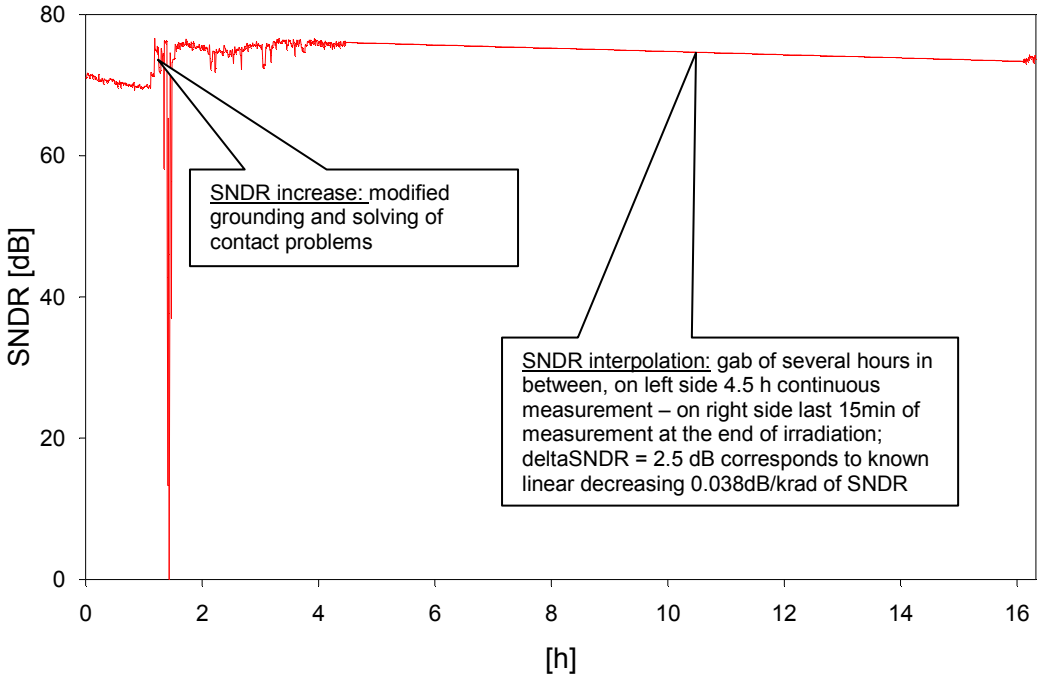

Figure 17 SNDR of the differential housekeeping channel

5.4 MFA102

The MFA102 chip was irradiated for more than 46 hours during cycle 2 up to a maximum TID level of 261.5 krad. All test details are summarised in the table below

Type of test board	Voltage board
Device name	MFA102
Operating condition	biased
Chip parameters checked	Supply currents of +3V3A and +3V3D; Chip command ability, data transmission and status bits; Functionality of test bus; Continuous meas. of short circuited Y- and Z-axis; SNDR of H/K channel 0;
Board parameters checked	Supply currents of +5VD, +/-8VA and +8VD
Total ionization dose	261,5 $krad_{(Si)}$ (cycle 2)
Dose rate	93.5 $rad_{(Si)}$/min
Duration of irradiation	~46.6 hours (cycle 2)
Distance to source	~44 cm
Sample Temp.	20°C (+/-1°C)
MFA condition	CLK and power supply provided by EGSE; X-axis not operational; Y-axis short circuited at ext. fully div. preamp (THM4131); Z-axis short circuited at ext. fully div. preamp (THM4131); Sine wave applied to HK-channel 0 for SNDR measurements: 10 Hz/2Vpp differential;

Table 7 Summary of TID test with MFA104

6 Conclusion

Altogether four MFA chips of the same lot were tested during three consecutive total dose irradiation cycles. The MFA104 was tested up to 261.5 krad at a dose rate of about 93 rad/min. The MFA112 was tested up to 225.3 krad at a lower dose rate of about 56 rad/min. The third one (MFA102) as well as the fourth one (MFA109) were tested up to 129.4 krad and 88.6 krad, respectively.

The complete test campaign aimed for finding the total ionization dose for which the MFA completely fails by either a dramatic increase of the power consumption or a failure in the basic functionality like data transmission, test bus operation, command ability etc. With this set-up it was not possible to do detailed performance tests which will have to be carried out later.

Device Name	Test Cycle	ΔSNDR [dB/krad]	ΔI_d [%/krad]	Max. Radiation Level
MFA104	2	-0.038	0.24	261.5 $krad_{(Si)}$
MFA112	1 / 2	-0.058	< 0.1	225.3 $krad_{(Si)}$
MFA109	3	-0.038	0.20	88.6 $krad_{(Si)}$

Table 8: Summary of SNDR drop-off and digital supply current increase

In general, it was not possible to destroy the chip with the Co-60 source. All chips showed full functionality in terms of command ability, data transmission as well as modulator and test bus operation during the complete test run as well as after the irradiation. The check-out of the MFA102 and the MFA112 chips was adversely affected during the first test cycle because some of the chip surrounding digital driver ICs failed due to the remaining irradiation behind the shielding blocks.

An increase of the supply current on the 3.3V digital supply as well as a decrease of the Signal-to-Noise and Distortion Ratio (SNDR) was in principle measured for all devices under test (see a summary in Table 8). The digital supply currents increases by about 0.2 %/krad and the SNDR drops by 4-5 dB per 100 krad. No significant variation of the analog supply current was detected.