Title : Evaluation of the TID Radiation Test Results of SHAMROC Phase 1 DACs

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Abbreviations and acronyms

Item	Meaning
ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuit
DAC	Digital to Analog Converter
DUT	Device Under Test
ESPAX	Exomars asic SPAce qualification of miXed signal asics
FPGA	Field Programmable Gate Array
ppm	Parts Per Million
SHAMROC	SEIS High Accuracy Mixed-signal Read-out Chip
TID	Total Ionizing Dose
^{60}Co	Cobalt-60, Radioactive Isotope of cobalt

Applicable Documents

[AD#]	Doc. Reference	Issue	Title
[AD1]	SRON-SHAMROC-RS-2007-001	3.0	SHAMROC Design Specification
[AD2]	SRO001	D1g	Measurement report functional subblock tapeout
[AD3]	SRON-SHAMROC-PL-2007-015	2.0	Radiation testplan
[AD4]			
[AD5]			
[AD6]			

Reference Documents

[RD#]	Doc. Reference	Issue	Title
[RD1]	XENSOR-SHAMROC-TR-2009-001	1.0	ADC TID Test Report
[RD2]	SRON-SHAMROC-TR-2009-010	0.1	On-chip T-sensor TID Test Report
[RD3]	SRON-ESPAX-PL-2008-001	1.0	ESPAX project plan
[RD4]			
[RD5]			
[RD6]			

1 Introduction

During the lifetime of the SHAMROC ASIC, it will be subjected to ionizing radiation on its mission to mars. To verify hardness against ionizing radiation, the SHAMROC ASIC will be subjected to a Total-Ionization-Dose (TID) test, as part of the space qualification process. Within the frame of the ESPAX project [RD3], the phase 1 sub-blocks of the SHAMROC ASIC are individually TID tested to investigate whether major TID induced problems can be expected. This document only reports the TID measurements performed on the DAC. The results of the ADC are described separately in [RD1] and the on-chip Temperature-sensor subblock results are described in [RD2].

During the EXOMARS mission the electronics of the SHAMROC ASIC will endure a maximum TID of 6.2kRad (SHAMROC-0080 in [AD1]) which is received for the largest part during it's travel to Mars. In order to investigate the influence of this TID radiation on the performance of the DAC 5 devices have been subjected to a low dose of up to 16krad. The radiation source to do a TID test is a ^{60}Co source which is located at the radiation test facilities of ESA/ESTEC.
To further assess the radiation tolerance *limits* of the DAC, 5 devices have been subjected to a high dose of up to 409krad. For this purpose, two setups have been created. In order to separate systematic influence of the measurement setup from the radiation effects, 1 reference device is added to the test. This device has not been irradiated. Table 1 will show which device belongs to which category.

The evaluation results are an essential input for the SHAMROC design team and - if deemed necessary – may lead to design optimization measures that improve the radiation hardness of the integrated chip at a later stage of the project.

Device	Category	Dose Measurements (kRad)		
		TID_1	TID_2	TID_3
6210D-1007	High Dose	43.8	135.7	409.5
6210D-1011	High Dose	43.8	135.7	409.5
6210D-1013	High Dose	43.8	135.7	409.5
6210D-1015	High Dose	43.8	135.7	409.5
6210D-1017	High Dose	43.8	135.7	409.5
6210D-1002	Low Dose	1.97	4.11	16.32
6210D-1004	Low Dose	1.97	4.11	16.32
6210D-1006	Low Dose	1.97	4.11	16.32
6210D-1010	Low Dose	1.97	4.11	16.32
6210D-1014	Low Dose	1.97	4.11	16.32
6210D-1019	Reference	No Irradiation		

Table 1: Device categorization for TID test.

Measuring only five devices per dose implies that the amount of measurements is not enough to draw statistically proven conclusions. Later in the space qualification process, a TID test will be performed where the sample size is in-line with the requirements of ESCC22900; that is 10 samples + 1 reference sample. The goal of this test is to investigate if there are major TID induces issues to be solved.

All the devices were tested between each phase in the TID test. In total the devices are tested for eight times (see test plan for more details [AD3]):

- Once at SRON before irradiation (@SRON, T00),
- Once at ESTEC before irradiation (@ESTEC, T10),
- Once after 1 day of irradiation (TID_1, T20),
- Once after 3 days of irradiation (TID_2, T30),
- Once after 9 days of irradiation (TID_3, T40),
- Once back at SRON (@SRON, T50),
- Once after annealing (anneal, T60), and
- Once after accelerated ageing (ageing, T70).

There has been a small change in test setup between T00 and T10. This change involves the circuit connected to the output of the DAC. Due to this change the offset is slightly increased, however the noise measurement at the DAC output is improved. Measurement T10 @ESTEC can therefore be seen as the starting test step of the TID test sequence. The change was performed deliberately due to the improvement of the noise measurement.
During the different phases within a TID test the devices are biased. Biasing means that all power supplies are applied to the device and that the master clock is active. Real communication with the chip is not obligated, as long as the operation during those test phases is as close to the normal operation as possible.
The annealing process lasts for one day at 20°C. The accelerated ageing process takes seven days at 100°C.
The reference device is not irradiated, annealed or aged in any way and is therefore only used to verify if the test board operates constant over each measurement step.

6210D-1002 Low-dose
6210D-1004 Low-dose
6210D-1006 Low-dose
6210D-1010 Low-dose
6210D-1014 Low-dose
6210D-1007 High-dose
6210D-1011 High-dose
6210D-1013 High-dose
6210D-1015 High-dose
6210D-1017 High-dose
6210D-1019 Reference

Figure 1: Common legend for all plots inside the document.

Figure 1 shows the common legend for all figures in this document. In order to save space this legend is not included on every page. Generally speaking, all the high-dose devices are drawn in red, the low-dose devices are drawn in green, and the reference device is drawn in blue.

The output of the DAC is measured via an ADC on the test board. The sample frequency of this ADC is 14.29Hz and is used with two input circuits. The first input circuit uses a high gain and in used to measure low amplitude signals. The second input circuit is used to measure full range signals. Therefore this gain is much lower. The conversion between ADC_{LSB} and Volt is for high DAC values: $3/2^{24}$ V/LSB and for low DAC values this gain value is: $3/(64*2^{24})$ V/LSB.

In order to determine the influence of ionising radiation several parameters of the chip are measured. The parameters measured are offset, noise, gain and power consumption. These parameters are most likely to drift as function the radiation level and are quite easy to measure. To determine these parameters the output of the DAC is measured for 1320 samples while the digital output setting of the DAC was set to zero. With this set of data the offset (chapter 2) and the noise (chapter 3) are calculated. Secondly, the DAC generated a signal of approximately 0.5V and -0.5V. Each of these amplitudes were measured over 80 samples and used for a gain calculation (chapter 4). A housekeeping ADC measured the power consumption (chapter 5) of the DAC and the temperature (chapter 6) of the environment near the device. The conclusions can be found in chapter 7. The raw data samples are plotted in Appendix A.

2 Offset

The output of the DAC is measured with the value 'zero' in the output register. Each test step (T00, T10, ...) the device is measured over 1320 ADC samples (raw data is plotted in Appendix A, Figure 24 and Figure 25). The mean value is calculated for each period and plotted in Figure 2. In the plot it can be seen that the offset is constant up to the high dose measurement at TID_2 (red lines, high dose: 136 kRad). For the low dose devices (green lines) only a small change in offset can be seen, but this is also the case for the reference device (blue line). Therefore, we can conclude that this effect is due to the test board and not related to radiation.
In the first measurement 'T00, @SRON' the output of the DAC is measured just before the analog filter/buffer on the testboard. In the other measurements the offset is measured after the analog filter/buffer. That's why the offset is slightly different with respect to the other measurements. The reason for this change is that the noise at this point is less than after the filter (@SRON measurement). This was realized only after the first measurements T00 were already performed.
At 409 kRad an absolute maximum drift can be calculated of 300 µV. From the plot it can be seen that the drift can be positive as well as negative.

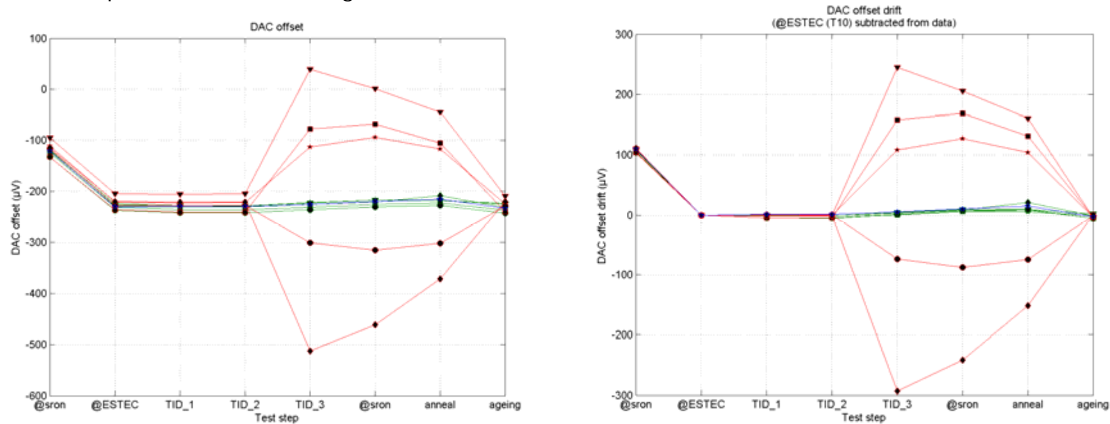


Figure 2: DAC offset in µV with zero output. Mean calculation of Figure 24 and Figure 25.

The annealing step, samples biased for 24 hours at room temperature, seems to reduce the effect caused by radiation. After the ageing step the effects caused by radiation is completely gone. Therefore no permanent effect can be seen in the offset value of the DAC.

The requirement on the offset (SHAMROC-0890) is 30ppm (≈69µV). This is not met with the current version of the chip, but this was already known from different functional tests [AD2]. Note though that the amplitude of the measured low dose offset variations are much less than 69 µV (ignoring the first data sample at T00 for reasons described above); The drift caused by TID effects up to ExoMars dose levels is within the specifications.

3 Noise

The noise of the DAC is determined with the same data as used for calculating the offset. The noise is measured as RMS-noise, pp_noise (peak to peak noise) and as function of frequency. The raw data plots can be found in Appendix A, Figure 24 and Figure 25. In these plots the ADC samples, from each individual measurement, are plotted against time.

3.1 Noise spectrum

The single sided output power spectral density of the DAC devices is plotted in Figure 3. The spectrum is calculated for each measurement period individually and plotted against the frequency. The ADC sample frequency is 14.29Hz therefore the calculated spectrum ends at 7.15Hz. In total 1320 samples are used to calculate each spectrum. Each spectrum is calculated with an average factor of 7 and 50% overlap.

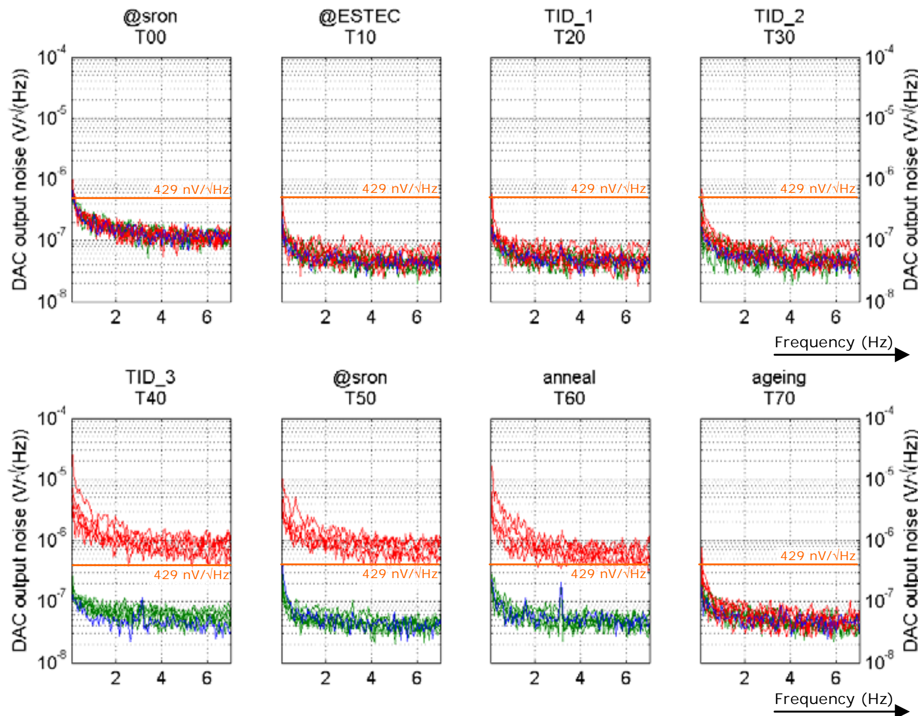


Figure 3: Output noise of the DAC against frequency during the several measurement periods. One line corresponds with one single DAC device.

From the figure several anomalies can be observed. The noise in T00 (@SRON) seems slightly higher with respect to the noise during the other test periods. This difference results not from the DAC but is due to the different measurement path on the test board as explained in section 1. After T00 the test setup was changed to gain this extra margin in the noise. Up to T30 (TID_2: 4.11kRad (green) and 136 kRad (red)) no observable effects can be found due to radiation. At T40 (TID_3: 409kRad) all high dose rate devices (red lines) show an increase in the noise with a factor of 15. This increase does not change after transportation back to SRON or after the annealing period. After ageing the noise is again back to its nominal level.

The requirement (SHAMROC-0840) for the noise above 0.1Hz is 429 nV/√Hz. The low dose rate devices always stay well below this level. During test period T60 (anneal) there is a little distortion around 3Hz. This distortion is due to the test board because it can be seen on the reference sample as well.

3.2 Noise RMS

The noise is also expressed as an RMS value. The results are plotted in Figure 4.

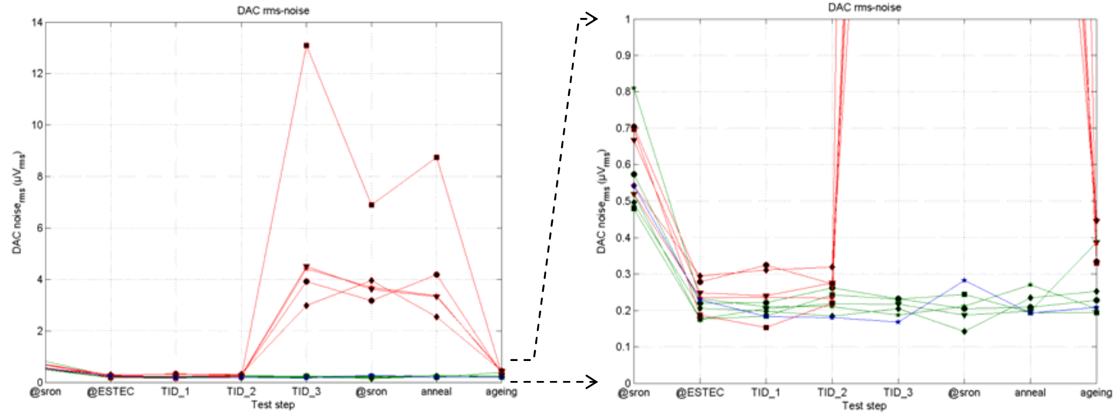


Figure 4: RMS-noise against measurement step. (left: RMS-noise level, right: zoom-plot)

The drift of the RMS noise is calculated by subtracting the T10 (@ESTEC) value from the other measurements. The RMS noise increases at 409kRad which is in line with the trends observed in the spectrum. The average increase is about $5\mu V_{rms}$ with a maximum of $13\mu V_{rms}$. Below 409kRad no observable effects can be seen. The noise of the low dose rate devices also stays for the complete period at the same level. After the ageing step all noise levels are back to the original values.

3.3 Noise PP

The peak to peak noise is also calculated with the output of the DAC set to zero. The results are plotted in Figure 5.

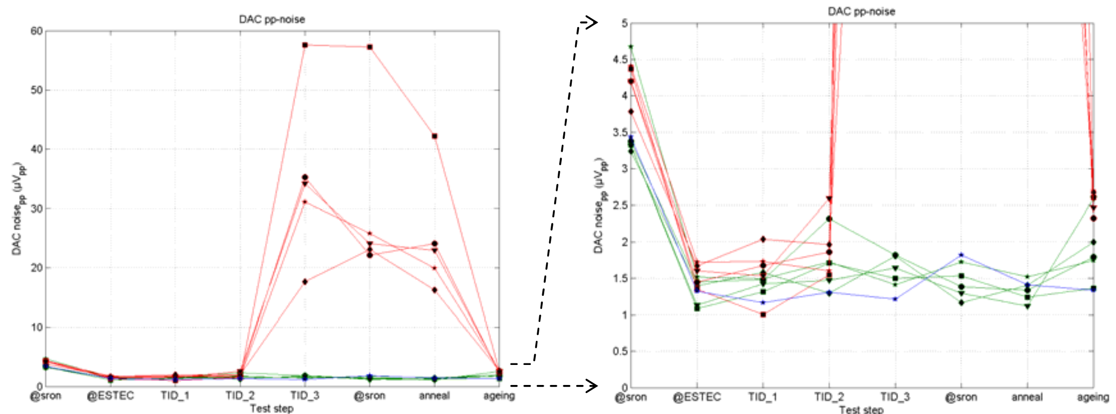


Figure 5: pp-noise against measurement step. (left: pp-noise level, right: zoom-plot)

The effects seen in the figure are corresponding to the effects seen at the other noise plots. There is however also a small difference between the peak to peak noise and the RMS noise. This means that that the noise is not just scaled due to radiation, but also has a different 'shape'. This phenomenon can also be seen in the time plots in Figure 24 and Figure 25.

4 Gain

The gain of the DAC is measured by generating two different DC output levels with the DAC. The levels send out with the DAC correspond to -4125634lsb and 4125634lsb. These two levels were measured 80 times by the ADC. The 'raw'-values are plotted against time in Appendix A, Figure 31 up to Figure 38. The digital ADC value is converted to voltages. The difference of the mean level of both amplitudes is used to determine the output swing of the analog signal. When the value for this swing is divided by the digital swing of the DAC (subtraction of both digital values) a gain value is calculated. The mean calculated gain of the DAC is 0.1288µV/LSB (see Equation 1). These measurements and calculations are done for each individual measurement step. Measurement T10 (@ESTEC) is subtracted to get a gain drift plot (see Figure 6) This point is used due to the change in test setup between T00 and T10.

$$Gain = \frac{\text{analogswing}}{\text{digitalswing}} = \frac{0.5305 - -0.5325}{4125634 - -4125634} = 0.1288 \cdot 10^{-6}\, V/_{LSB}$$

Equation 1: Gain calculation.

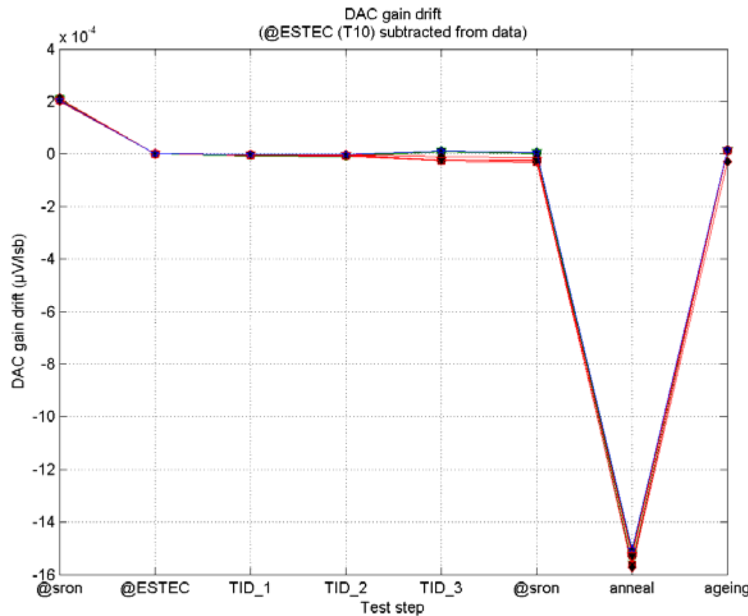


Figure 6: Calculated gain drift as function of measurement step.

The figure shows a large drift after the annealing step. The annealing process is however not performed on the reference sample, but the drift is found on this sample as well. From this result it can be concluded that it means that this measurement (T60-anneal) is not correct. Something disturbed the measurement for all devices, most likely this is the result of a loaded vs. an unloaded test situation. In order to say something about the gain drift as function of radiation the disturbed samples of T60 are excluded from the plot and a new plot is made in Figure 7.

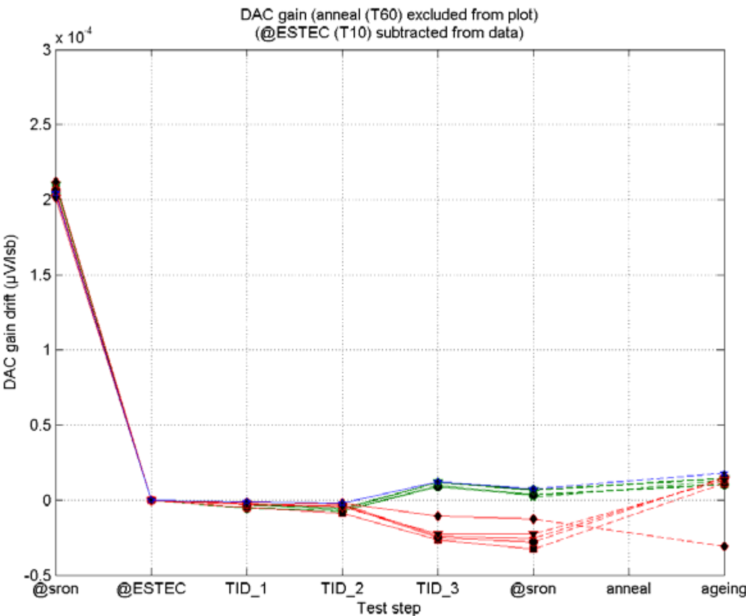


Figure 7: Calculated gain drift as function of measurement step with the annealing measurement excluded.

From this figure it can be seen that the first measurement is again different with respect to the other measurements. This is the result of the change in measurement path between DAC and ADC. At T40 (TID_3) some difference can be found in the gain values between the high and the low dose rate samples. The maximum drift between the reference device and the high dose rate samples is -0.05nV/lsb. This corresponds to a drift of -0.0388%, 388ppm (see Equation 2). Due to the fact that the reference and low dose rate samples also suffer from some drift, in the opposite direction, it is for sure that the test setup/method influences the result as well. The found drift can be seen as a worse case drift.

$$drift = \frac{\text{max. drift}}{\text{nominal gain}} = \frac{-0.5 \cdot 10^{-4} \mu V / lsb}{0.1288 \mu V / lsb} \cdot 100 = -0.0388\%$$

Equation 2: gain drift calculation.

After aging, 4 out of 5 high dose rate devices are again back on there nominal levels. Only 1 device (6210A-1015) still has a drift with respect to the gain measured before the radiation tests (@ESTEC). Please take into account that these values only apply on the high dose samples. The low dose samples follow the reference device, which is not radiated, annealed or aged, very good. No observable drift can be detected at those samples.

5 Power consumption

The power consumption of the DAC is measured during each measurement step. The power is calculated by measuring the voltage and current of the reference, the digital supply and the IO supply. This is done for the 'ON'-state of the DAC as well as the 'OFF'-state. Each voltage and current is measured for 10 samples in the 'ON'-state with a sample period of 2 seconds. After 10 samples the DAC is set to the 'OFF'-state and again 10 samples are measured. The raw data samples are plotted in Appendix A, Figure 15 up to Figure 22. The data is plotted against time for each individual measurement step.

5.1 Reference power consumption

The power consumption of the reference supply is calculated by multiplying the reference voltage with the current. The measured supply voltage is plotted against time in Figure 15. Both 'ON' and the 'OFF' voltage are plotted in the same subplot. There is a difference in measured voltage of <4mV between both states, this is the case for all radiated samples as well as the reference sample and can therefore be explained as a test board effect. The direct cause of this phenomenon is however not known (yet). Unfortunately this is also not an expected effect. The current is also measured and plotted against time in Figure 16. The currents in the upper-row are the measured during the 'ON'-state of the DAC while the bottom-row is measured in the 'OFF'-state. The calculated power is plotted in Figure 17.

Figure 8 shows the averaged value of the ON and OFF power consumption from the reference supply over the different test periods.

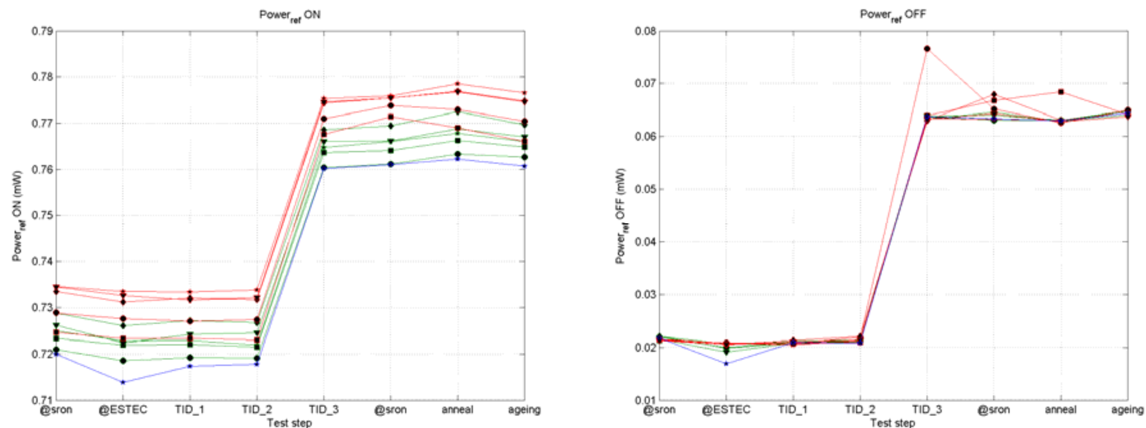


Figure 8: averaged 'ON' (left) and 'OFF' (right) power consumption from the reference supply.

From the figure a large jump can be observed between TID_2 and TID_3. This jump can be seen in all samples. The cause of this jump is not explained (yet). However it is for sure that it has something to do with the test board itself since the jump in 'ON'-state is similar to the jump in the 'OFF'-state and the jump is equal for all samples. In both states the jump is approximately 40µW.

Due to the jump the drift in the currents can not clearly be seen. In order to get a good impression about this drift, as a result of radiation, the drift of the reference is subtracted from all radiated samples. This way the test board effect is removed from the plots. The result can be seen in Figure 9.

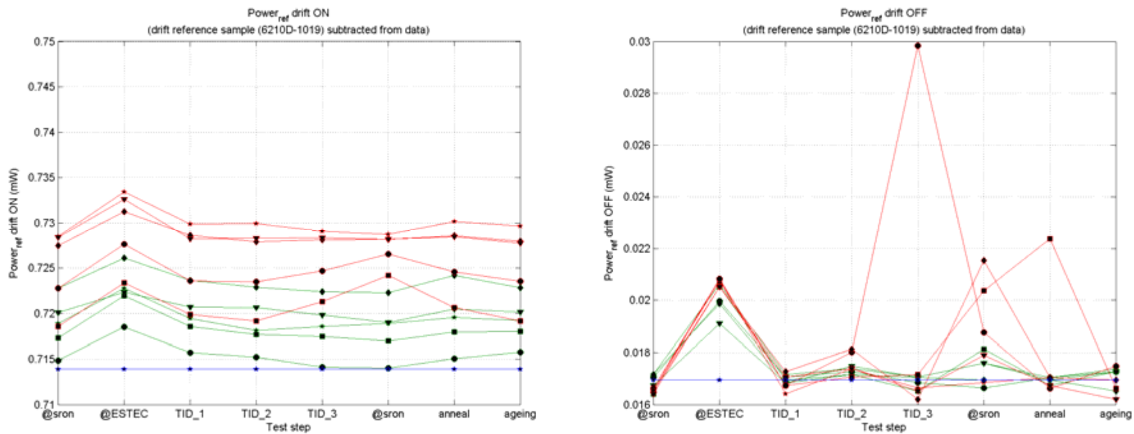


Figure 9: averaged 'ON' (left) and 'OFF' (right) drift of power consumption from the reference supply.

From the figure no clear drift can be observed. There are some measurements different from the rest but these effects can not be correlated with radiation, so these effects can be considered to be noise.

5.2 Digital power consumption

Also the power consumption of the digital part is calculated. The measurement is done in parallel with the measurement of the reference power. First the power is measured for 10 samples in the 'ON'-state, then the device is turned 'OFF' and the power is again measured for 10 samples. The measured voltage can be found in Figure 18, while the current is plotted in Figure 19. From these two plots the power is calculated and plotted in Figure 20.

Figure 10 shows the averaged value of the ON and OFF power consumption from the digital supply over the different test periods.

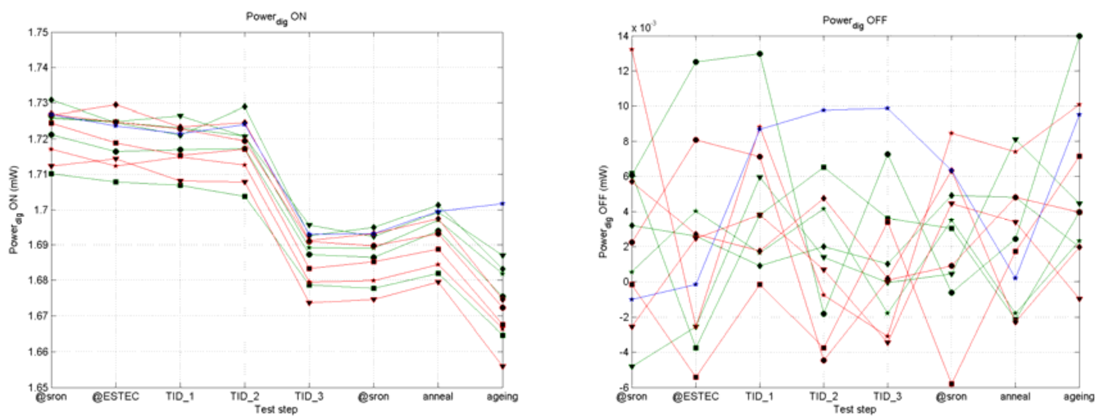


Figure 10: averaged 'ON' (left) and 'OFF' (right) power consumption from the digital supply.

The digital 'ON' consumption shows again a jump between measurement TID_2 and TID_3. This jump is almost the same (≈40μW) to the jump found within the reference measurements, however in opposite direction. The digital part does not show this phenomenon while the device is in the 'OFF'-state.
If the jump is removed from the plot, by subtracting the drift of the reference sample, the influence of radiation can be seen. The drift as function of test step is plotted in Figure 11.

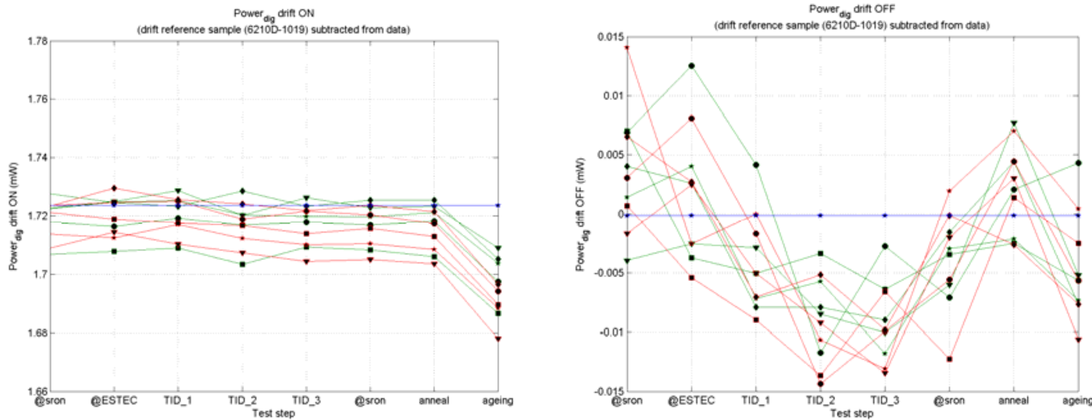


Figure 11: averaged 'ON' (left) and 'OFF' (right) drift of power consumption from the digital supply.

The power consumption in the 'ON'-state can not be correlated to the applied radiation because no drift can be seen. However there is an effect visible after the ageing step. This effect is approximately equal for all high and low dose rate devices.
The pattern seen in the 'OFF' measurement is mostly due to the effects seen on the reference sample (see Figure 10). The measured fluctuations can be seen as noise. The noise of the digital part is, in some points, calculated as a negative power. This is due to the method how the test board is made. Figure 12 gives an illustration about the test setup.

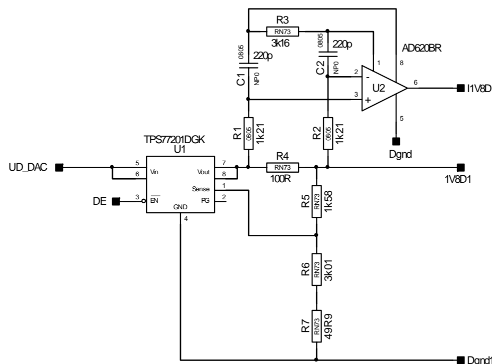


Figure 12: digital supply circuit of the DAC test board.

The digital supply voltage is regulated via a sense path (R5+R6+R7). This path consumes some current. The consumed current is added to the current measurement (voltage drop over R4) as an offset value. The software subtracts this offset value from the measured value. The inaccuracy of this subtraction is however in the same order as the digital current in the 'OFF' state. This is the reason why that calculation of the

power consumed by the DAC seems, sometimes, negative, while in fact the digital offset compensation of the sense path is too high.

5.3 IO power consumption

The IO circuit in the DAC also consumes some power. For the power calculation only the current can be measured. Since the test board is not capable of measuring the 3.3V IO voltage this value is assumed to be stable. The measurement is again done parallel to the digital and reference measurement. The measurement result is plotted in Figure 21. The current measurement is multiplied by 3.3V to calculate the power consumption of the IO section. The result is plotted in Figure 22.
Figure 13 shows the averaged value of the ON and OFF power consumption from the IO supply over the different test periods.

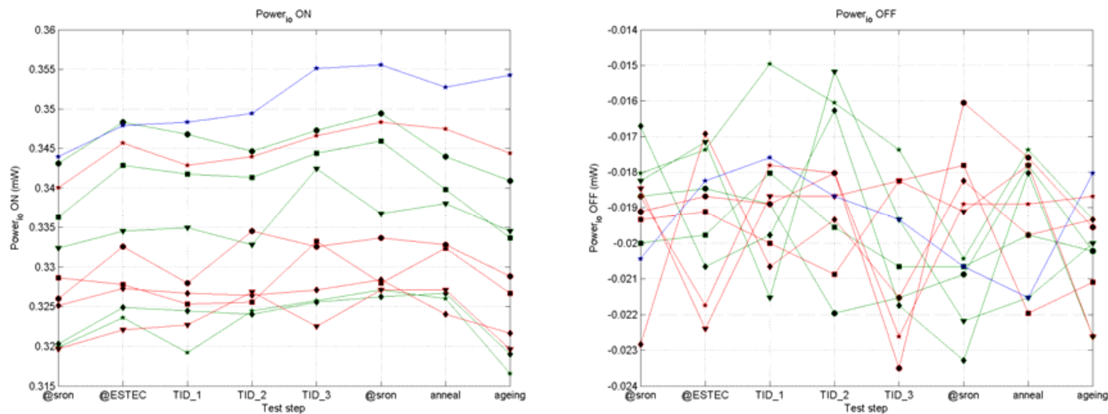


Figure 13: averaged 'ON' (left) and 'OFF' (right) power consumption from the IO supply.

From these plots no jumps can be observed and also no drift can be found. It can therefore be concluded that there is no influence of radiation on the IO supply up to the high dose level of 409kRad.
From the power consumption in the 'OFF'-state it can be seen that again the subtraction is inaccurate. Of course the power consumed by the device is not negative.

5.4 Analog power consumption

The analog power consumption is too small to measure. The current drawn from this supply can not be measured on the test board since it is in the range of 4μA. The voltage towards this point can however be measured and the result is plotted in Figure 23. This voltage is similar to the digital as well as the reference supply voltage.

6 Temperature

During the power measurements also the temperature of the device environment is monitored. The temperature sensor is positioned on the test board in the neighbourhood of the chip. This is done to verify if the external conditions of the test board are similar during all different test steps. This temperature measurement can be found in Figure 14. In this plot the temperature is plotted against time for each individual test step.

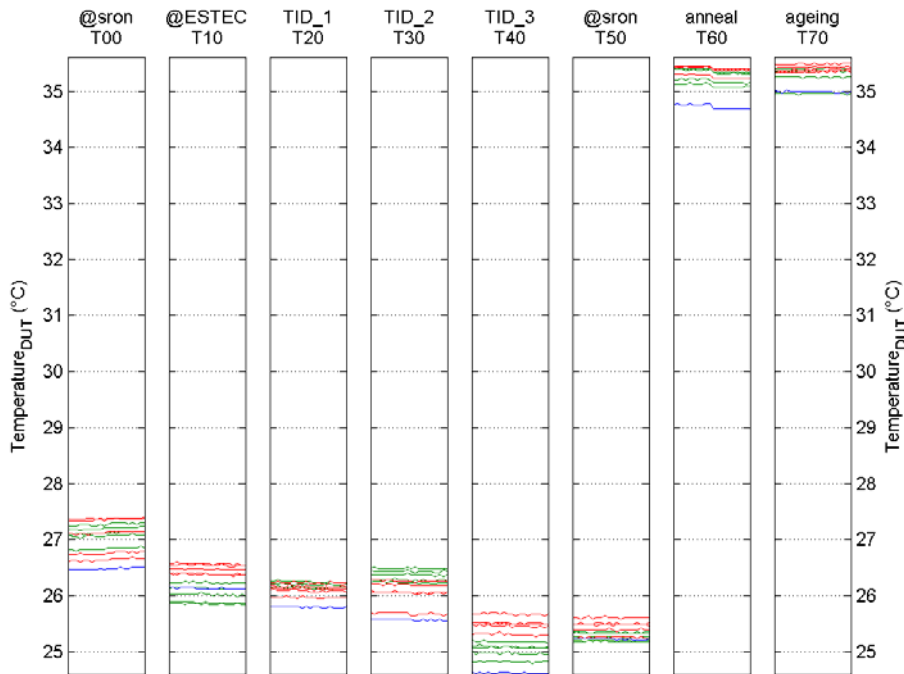
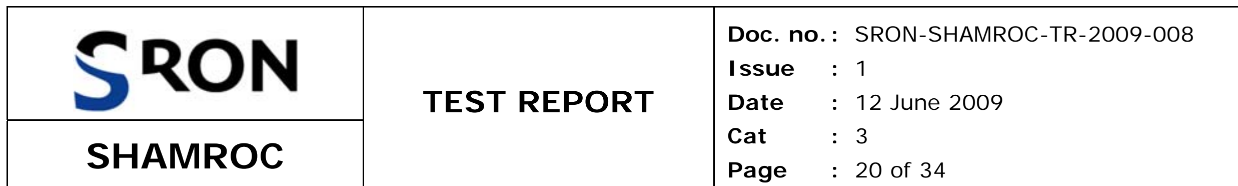


Figure 14: device temperature as function of time over all different test steps (not regulated).

The device temperature is almost the same over all test steps. However the temperature has an increase at the last two measurement steps (T60 and T70). The effect of this increase in temperature can not be correlated to any measurement result. The different temperature is therefore concerned not to be a problem.



7 Conclusion

From the TID measurement several conclusions can be drawn. As an overall conclusion it can be stated that the low-dose rate devices do not show any effect due to radiation. Also the high dose rate samples are measured without any influence up to a radiation level of at least 136kRad. Above this level (409kRad) some influences can be observed but none of the effects are destructive to the device.

- Offset:
  The offset has an increase of 300µV. After the ageing period this influence is completely gone.
- Noise:
  The noise increases to a value just above the requirement. This increase in noise increase is also not a permanent damage in the device, because the noise is back to its nominal level after the ageing period.
- Gain:
  The gain is changed due to the radiation with maximum of -0.0388% (388ppm). This drift must be seen as an worse case drift because the test setup causes a small drift as well. With only 1 out of 5 (high dose rate) devices this drift seems to be of permanent damage while the other 4 are back to their nominal levels.
- Power consumption:
  No effects can be correlated with the applied radiation to the devices. All measured currents are similar to the expected levels. There are a few test board effects, but these can not be the result of radiation.

Appendix A

RAW data files.

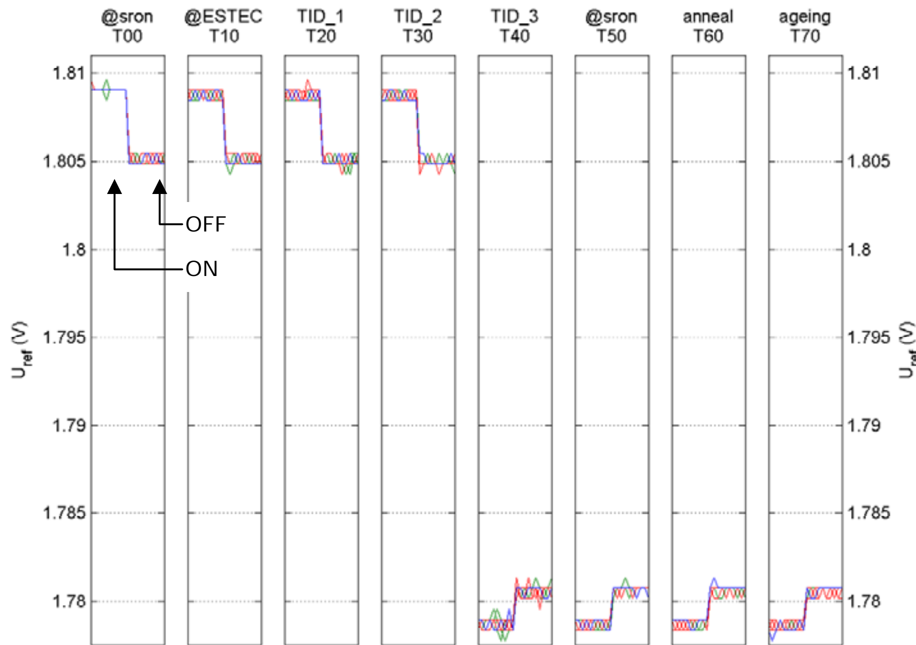


Figure 15: Uref as function of time over all different test steps. (10 values per ON / OFF state)

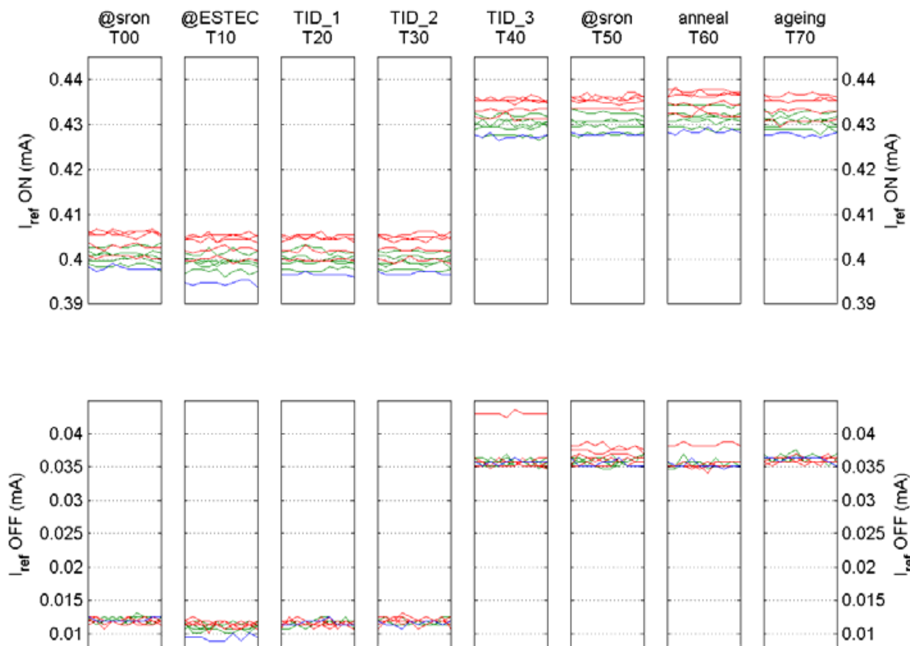


Figure 16: Iref ON and OFF as function of time over all different test steps. (10 values per state)

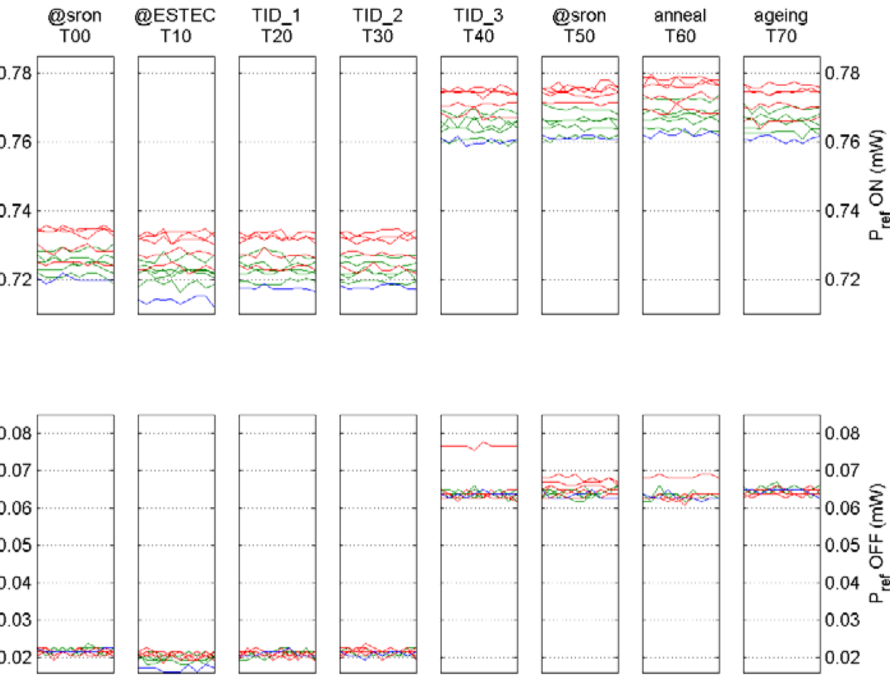


Figure 17: Pref ON and OFF as function of time over all different test steps. (10 values state)

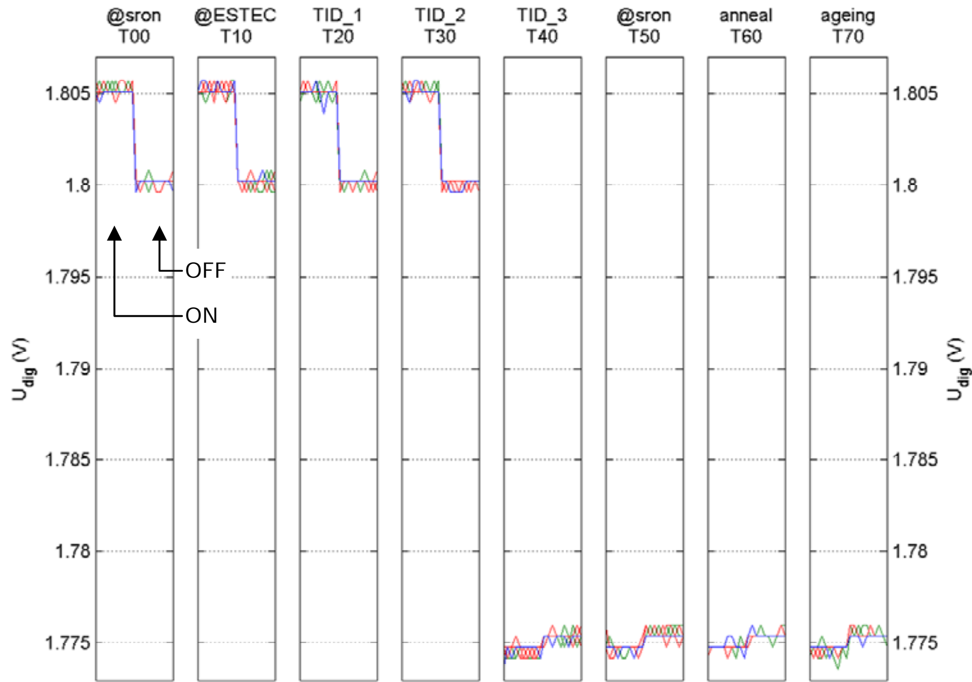


Figure 18: Udig as function of time over all different test steps. (10 values per ON / OFF state)

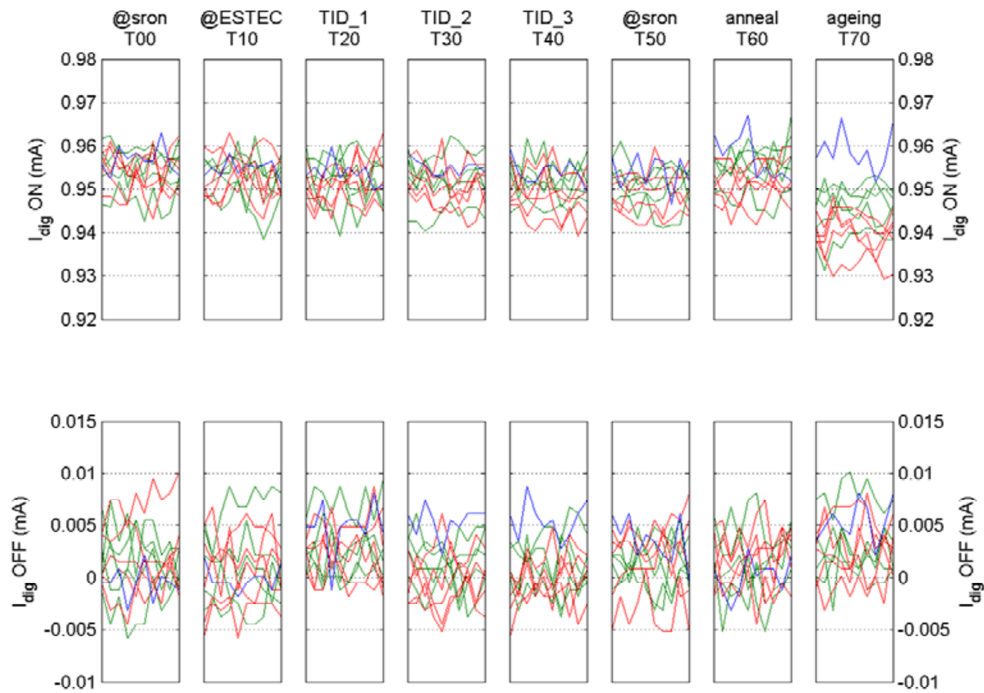


Figure 19: Idig ON and OFF as function of time over all different test steps. (10 values per state)

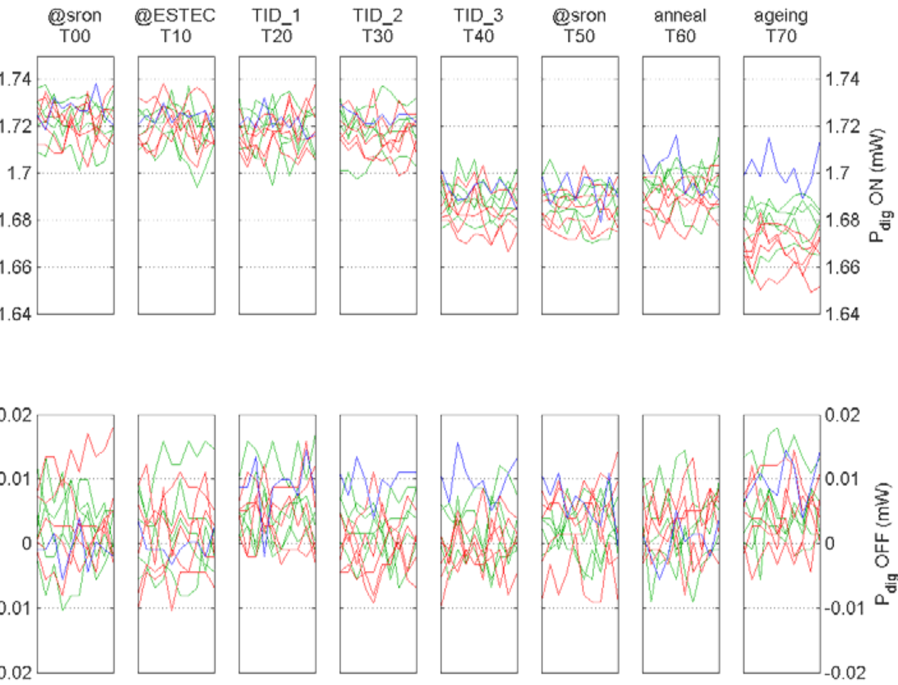


Figure 20: Pref ON and OFF as function of time over all different test steps. (10 values per state)

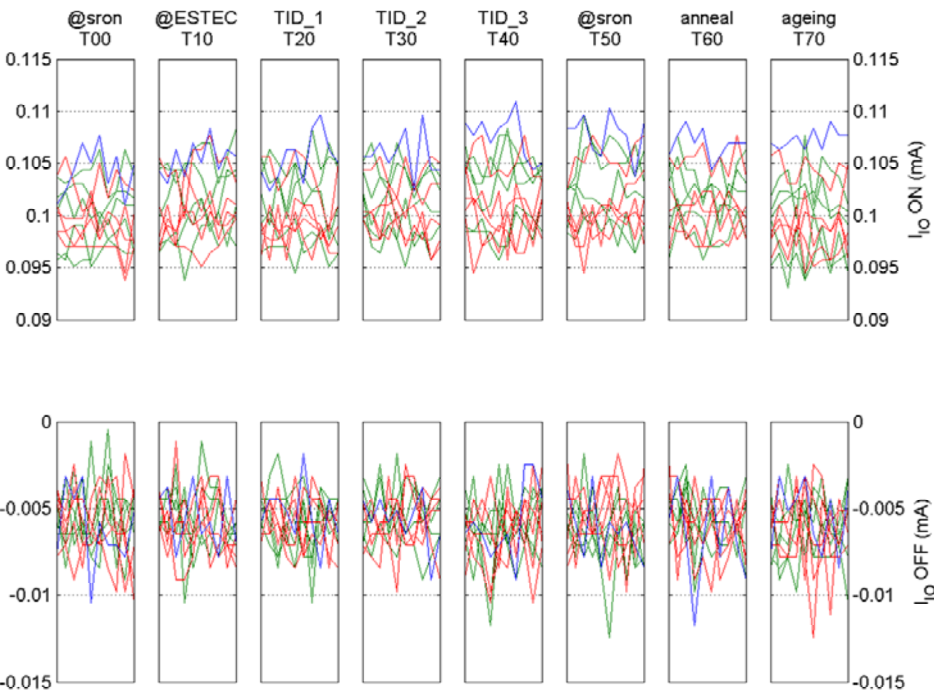


Figure 21: Iio ON and OFF as function of time over all different test steps. (10 values per state)

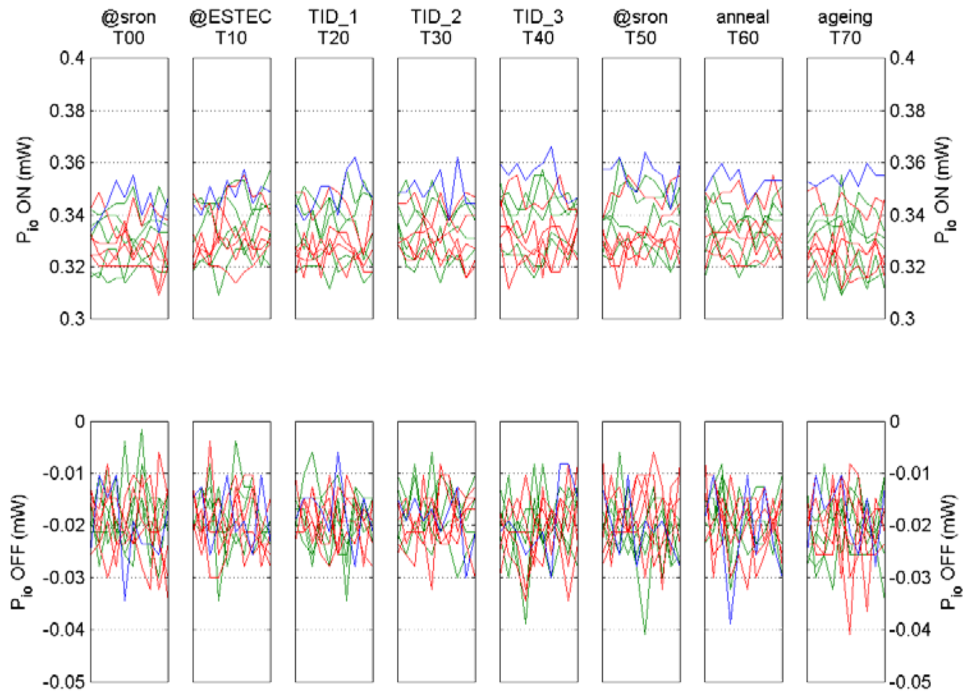


Figure 22: Pio ON and OFF as function of time over all different test steps. (10 values per state)

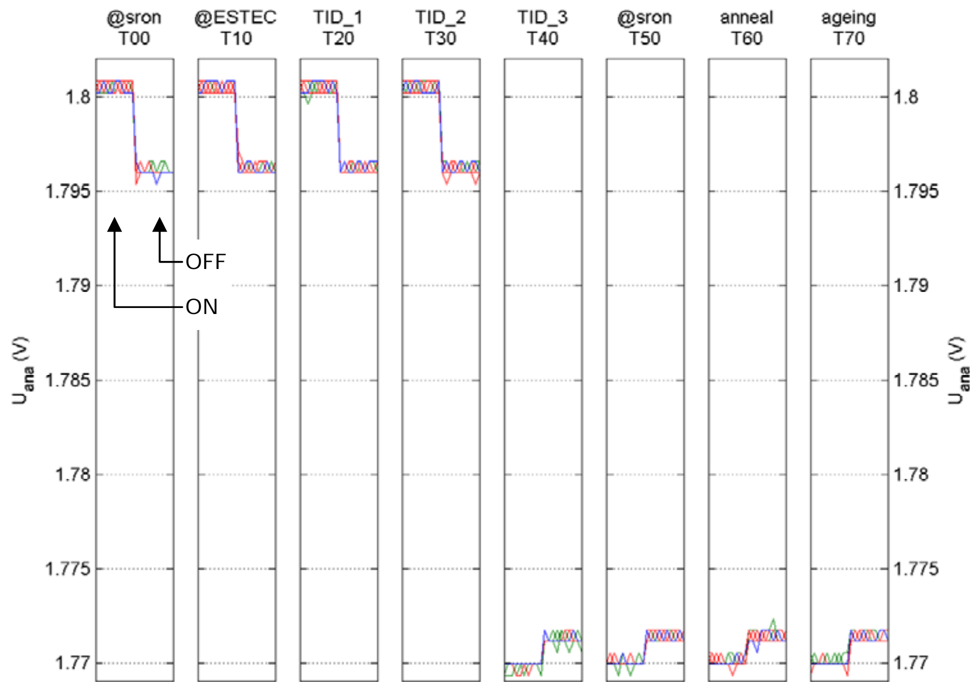


Figure 23: Uana as function of time over all different test steps. (10 values per ON / OFF state)

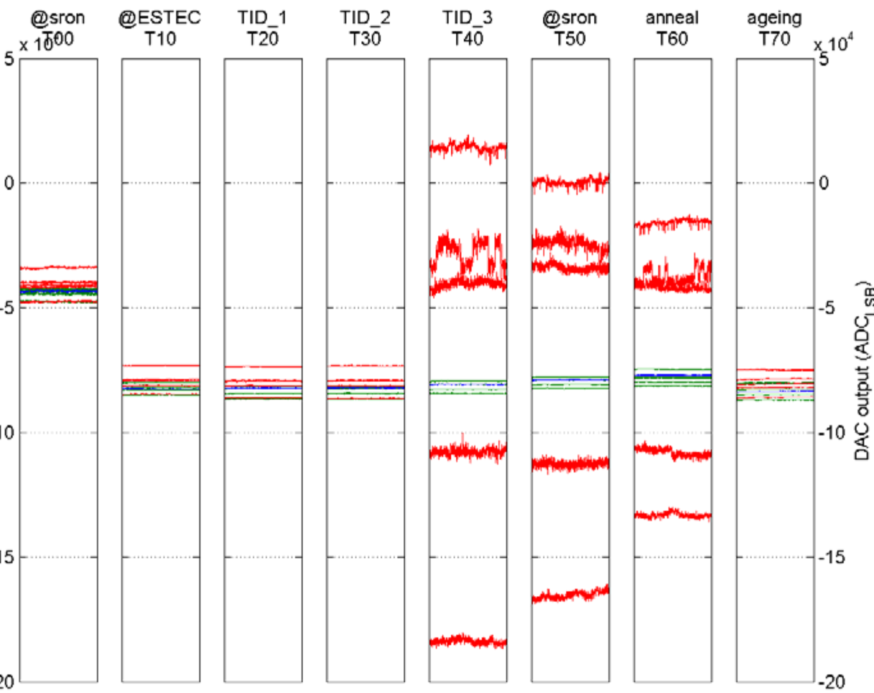


Figure 24: DAC output in ADC_LSB with DAC_out 0x000000. (Fs_ADC: 14.29Hz, 1320 samples)

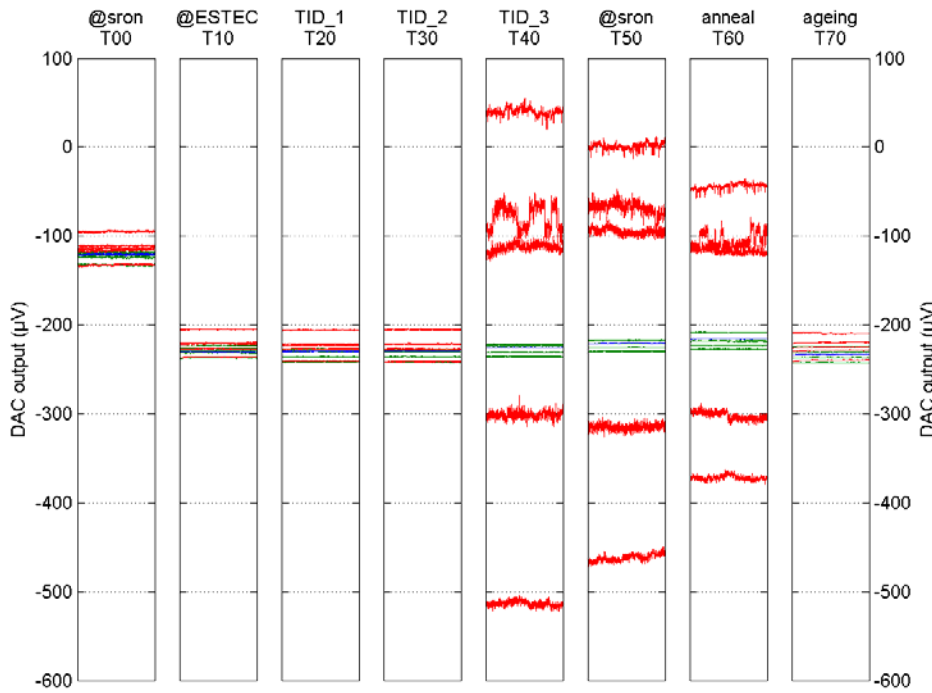


Figure 25: DAC output in µV with DAC_out 0x000000. (Fs_ADC: 14.29Hz, 1320 samples)

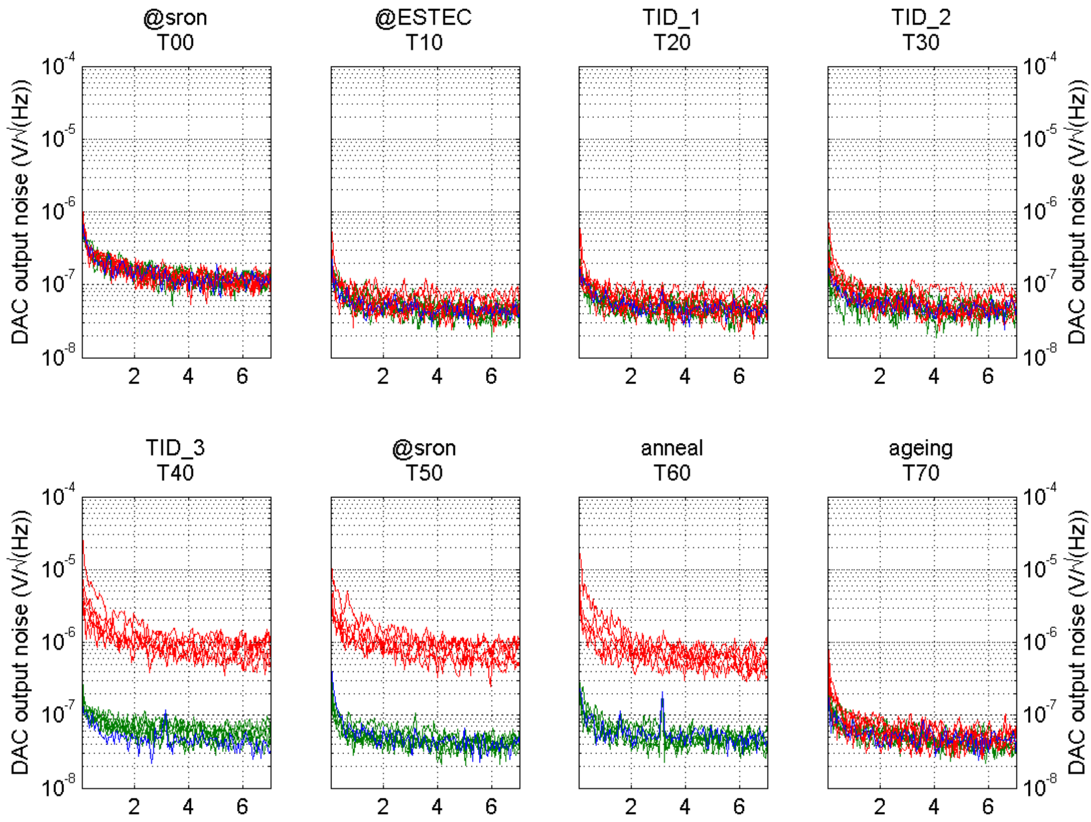


Figure 26: DAC output noise (μV/√(Hz)) against frequency (DAC_out 0x000000, Fs_ADC: 14.29Hz)

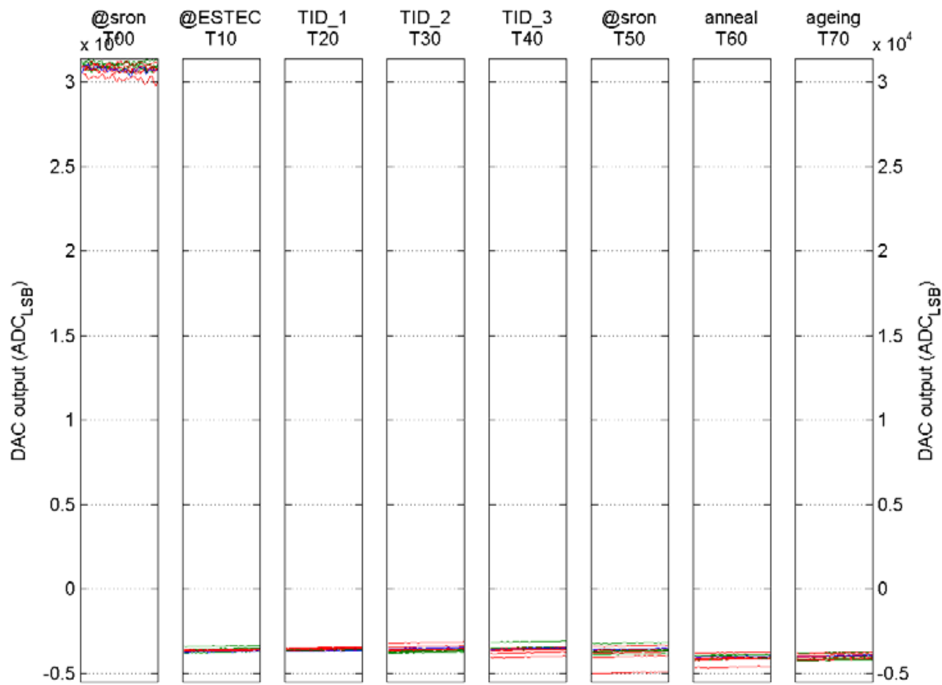


Figure 27: Board offset in ADC_LSB with shorted ADC input. (Fs_ADC: 14.29Hz, 40 samples)

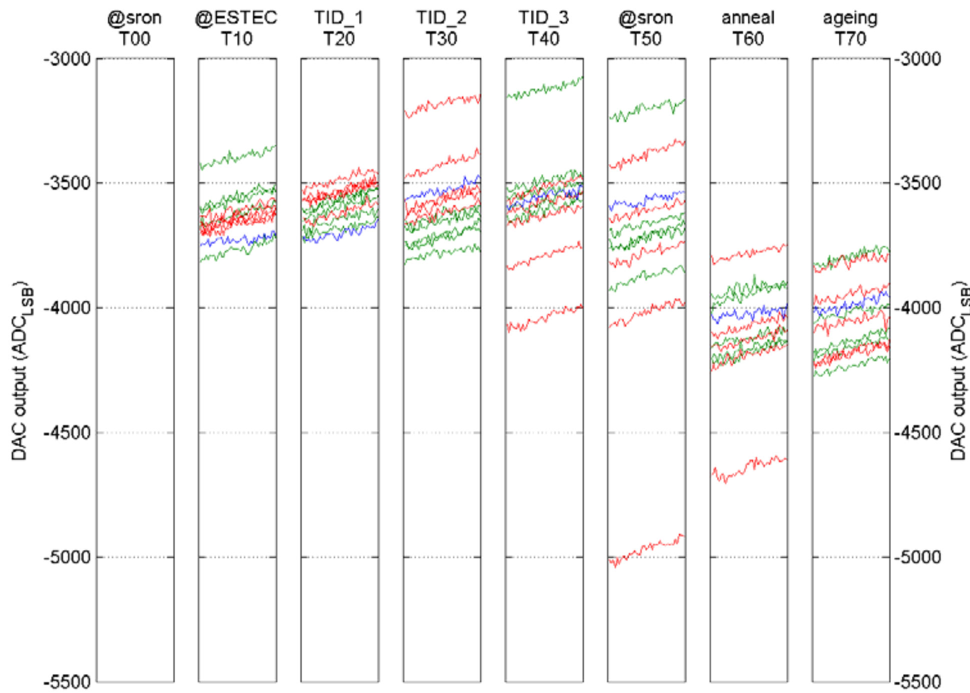


Figure 28: Board offset in ADC_LSB with shorted ADC input (picture scaled without T00).

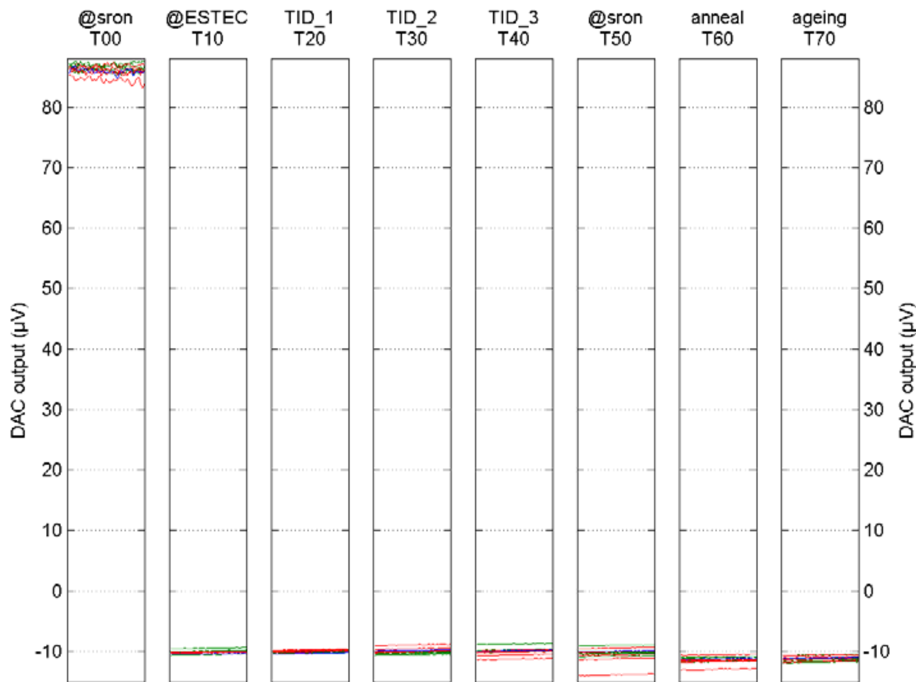


Figure 29: Board offset in µV with shorted ADC input (Fs_ADC: 14.29Hz, 40 samples).

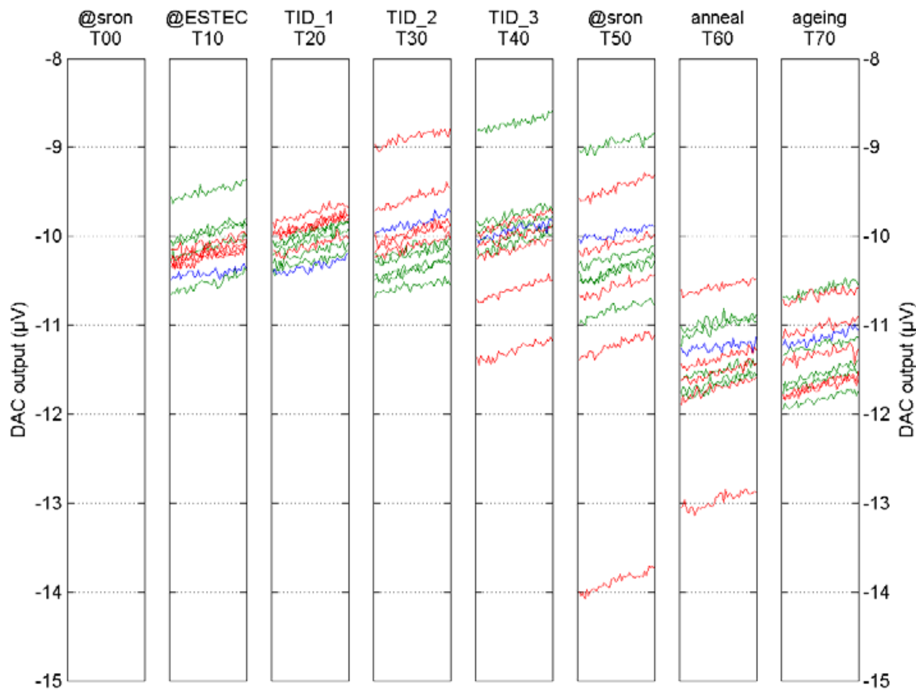


Figure 30: Board offset in µV with shorted ADC input (picture scaled without T00).

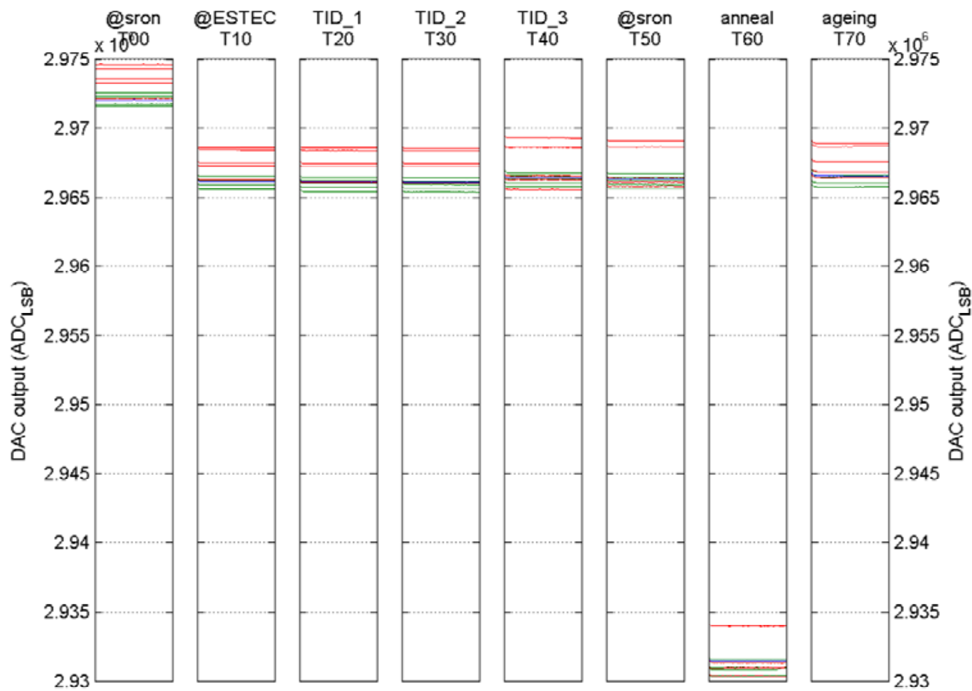


Figure 31: DAC output in ADC_LSB with DAC_out = 4125634 (Fs_ADC: 14.29Hz, 80 samples).

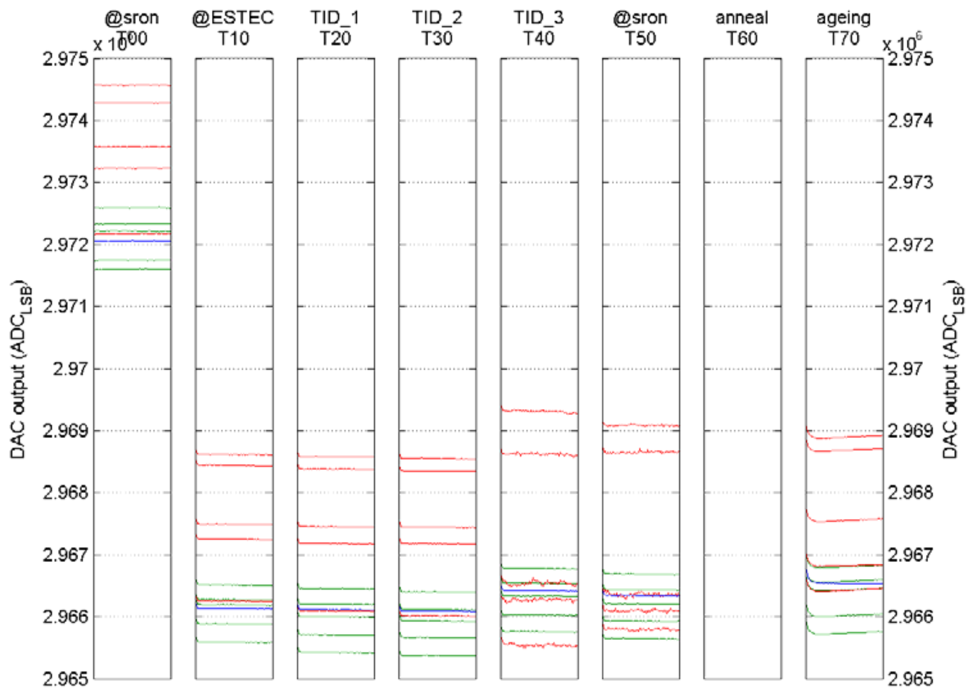


Figure 32: DAC output in ADC_LSB with DAC_out = 4125634 (scaled without T60).

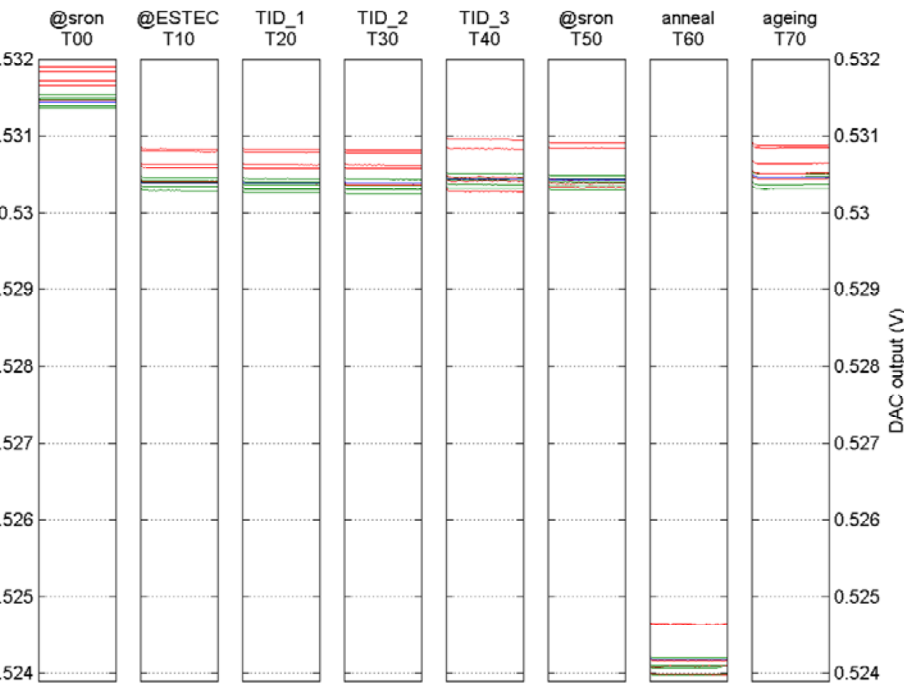


Figure 33: DAC output in V with DAC_out = 4125634 (Fs_ADC: 14.29Hz, 80 samples).

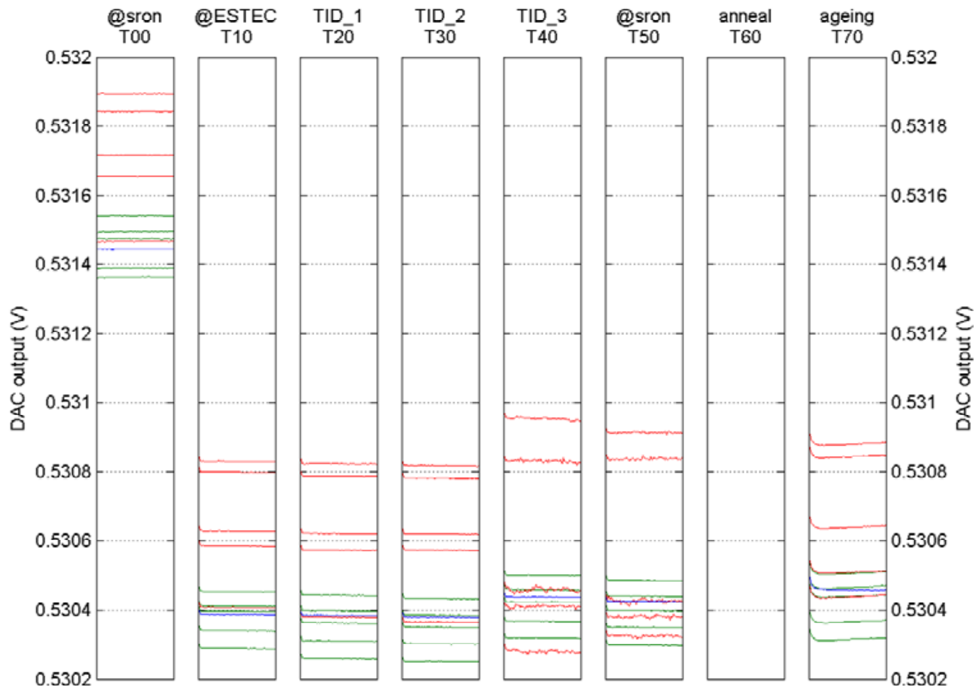


Figure 34: DAC output in V with DAC_out = 4125634 (scaled without T60).

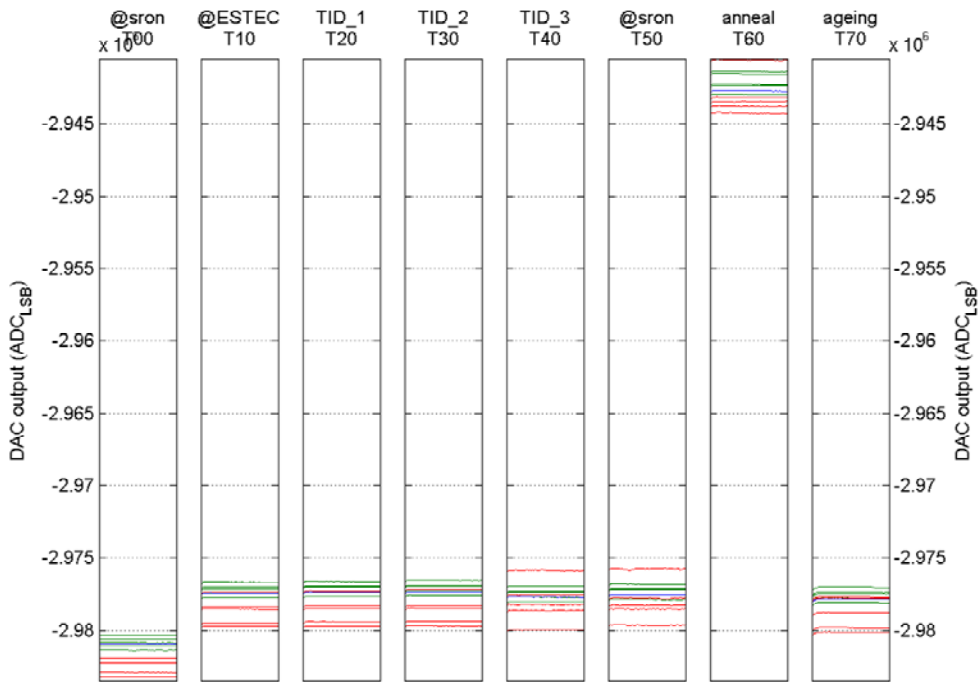


Figure 35: DAC output in ADC_LSB with DAC_out = -4125634 (Fs_ADC: 14.29Hz, 80 samples).

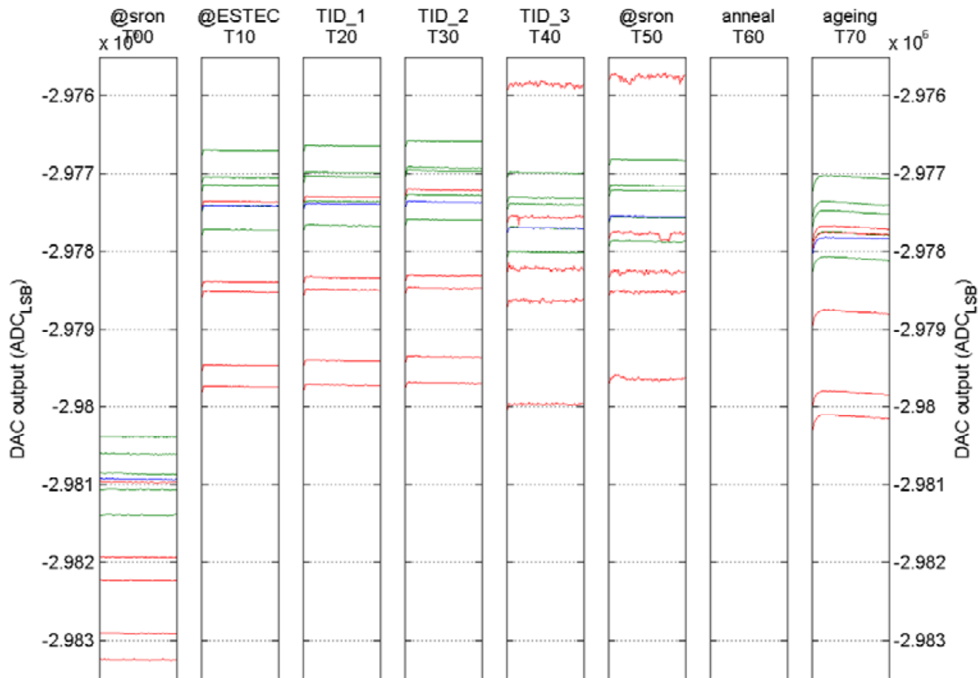


Figure 36: DAC output in ADC_LSB with DAC_out = -4125634 (scaled without T60).

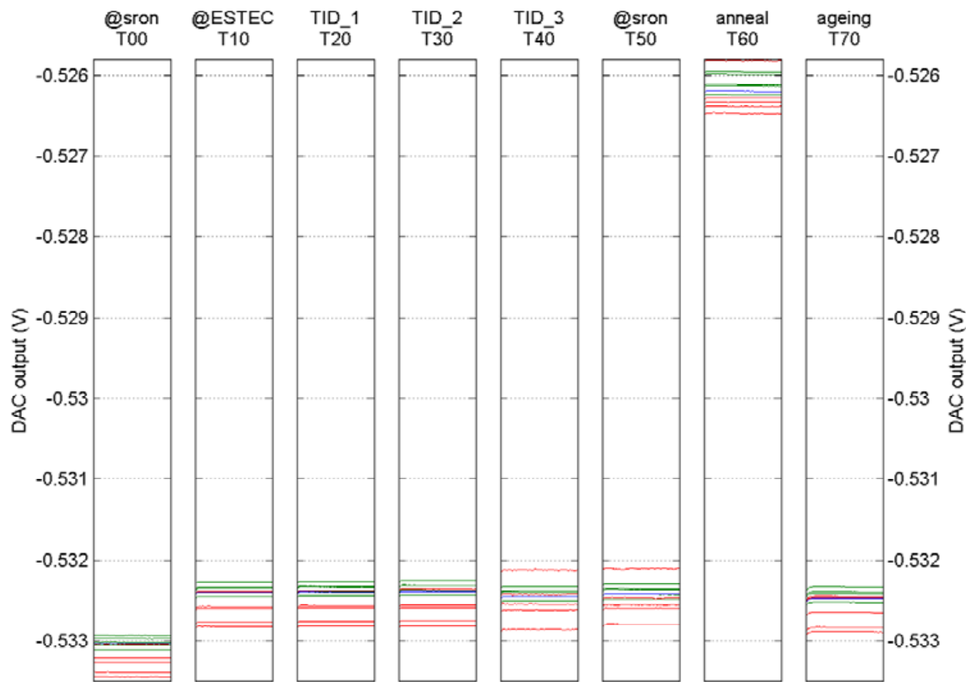


Figure 37: DAC output in V with DAC_out = -4125634 (Fs_ADC: 14.29Hz, 80 samples).

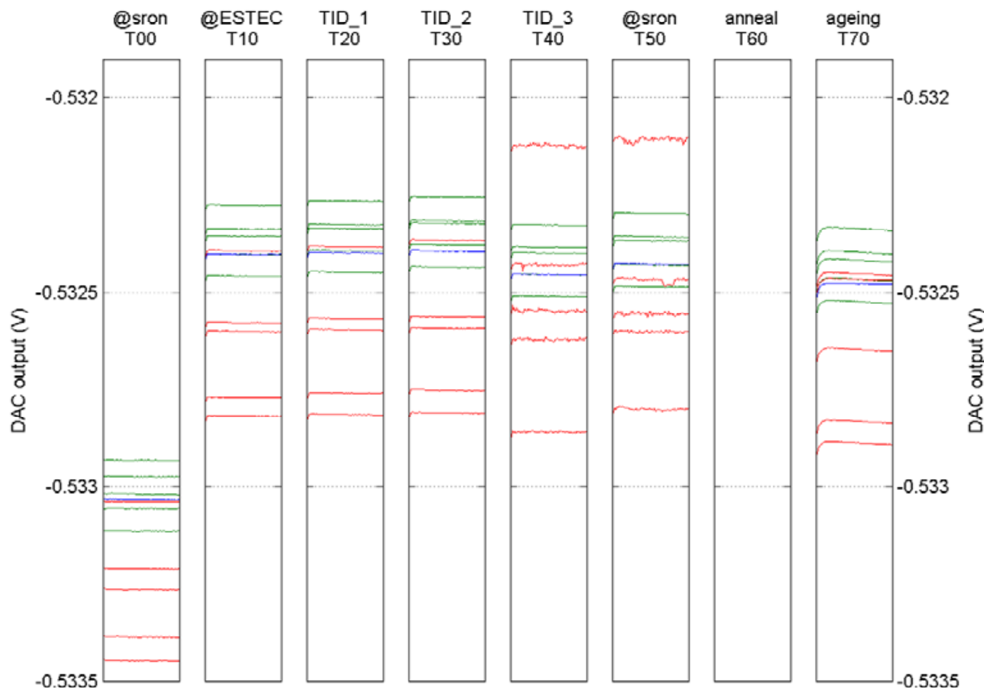


Figure 38: DAC output in V with DAC_out = -4125634 (scaled without T60).