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HAS2 Heavy Ion Test report

HAS2 Heavy Ion Test report

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1.SCOPE AND APPLICABILITY

1.1.Scope

This test report presents the result of the heavy ion irradiation of the HAS2 CMOS image sensor performed in the frame of ESTEC contract N° 4000102571/10/NL/AF “Radiation Characterization of Laplace/Tandem RH optocouplers, sensors and detectors”.

The irradiations were performed at the heavy ion irradiation facility in Louvain-La-Neuve (B) June 22nd 2012.

1.2.Purpose

Low LET range and Non Destructive Readout mode are investigated in order to complete heavy ion data currently available. High LET range is covered by the heavy ion campaign reported in [RD 2].

2.REFERENCES

2.1.Applicable documents

[AD 1] ITT 6429 HAS Irradiation Test Plan, PR__00004584, D

2.2.Reference documents

[RD 1] ON Semiconductor HAS2 Detailed Specification NOIH2SM1000A/D, Rev. 3

[RD 2] HAS2 Heavy ion test report, HAS2-CY-FVD-07-214, Rev. 2.1, D. Van Aken, Cypress, December 11 2007

[RD 3] Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

3. ABBREVIATIONS

AD	Applicable Document
APS	Active Pixel Sensor
CDS	Correlated Double Sampling
CMOS	Complementary Metal-Oxide Semiconductor
DC	DateCode
DDD	Displacement Damage Dose
DR	Destructive Readout
DS	Double Sampling
DSNU	Dark Signal Non Uniformity
ECSS	European Cooperation for Space Standardization
EOL	End Of Life
FPA	Focal Plane Array
FPN	Fixed Pattern Noise
HAS2	High Accuracy STR 2
LET	Linear Energy Transfer
LSB	Least Significant Bit
N/A	Not Applicable
NDR	Non-Destructive Readout
PCB	Printed Circuit Board
RD	Reference Document
SEE	Single Event Effect
SET	Single Event Transient
SEU	Single Event Upset
SEFI	Single Event Failure interrupt
TID	Total Ionizing Dose

4.DEVICE INFORMATION

4.1.HAS2 presentation

The Accuracy STR 2 sensor (HAS2) is a 1024 x 1024 pixel rolling shutter Active Pixel Sensor (APS), featuring a programmable (gain and offset) output amplifier (PGA) and an internal 12 bits ADC.

The CMOS image was sensor designed and manufactured by ON Semiconductor[1] under ESA contract 17235/03/NL/FM for star tracker applications.

The simplified block diagram of HAS2 is presented in Figure 4-1.

Pixel design is based on a photodiode coupled with a three transistor readout circuit. The HAS2 is the descendant from a lineage radiation-hardened by design sensors from ON Semiconductor: the photodiodes includes a doped surface protection layer to prevent the depleted area from reaching the field oxide interface, while the CMOS readout circuitry is designed using enclosed geometry transistor layouts.

The wafers are produced by Plessey Semiconductors[2] on the standard XC035P311 CMOS process (0.35 µm).

In order to reduce the variation in signal offset from pixel to pixel (known as Fixed Pattern Noise, or FPN) typically seen on APS, the HAS2 implements two different noise reduction techniques: Double Sampling (DS) also called Destructive Readout (DR) and Correlated Double Sampling (CDS) also called Non Destructive Readout (NDR). In DR mode, the pixel is reset at the end of the signal integration time in order to sample the pixel reference level. The reference level is subtracted from the signal level in order to cancel the pixel offset. This internal analog operation is performed before digitization. In NDR mode, two images are sampled and digitized: a reference image at the beginning of the integration time, and a signal image at its end. Offset correction must be performed off-chip by subtracting these two images.

A temperature sensor is also integrated on chip, which can be addressed through an internal multiplexer. This MUX can also address analogue inputs to be digitized by the internal ADC.

[1] Formerly Cypress BVBA and Fillfactory.
[2] Formerly X-FAB.

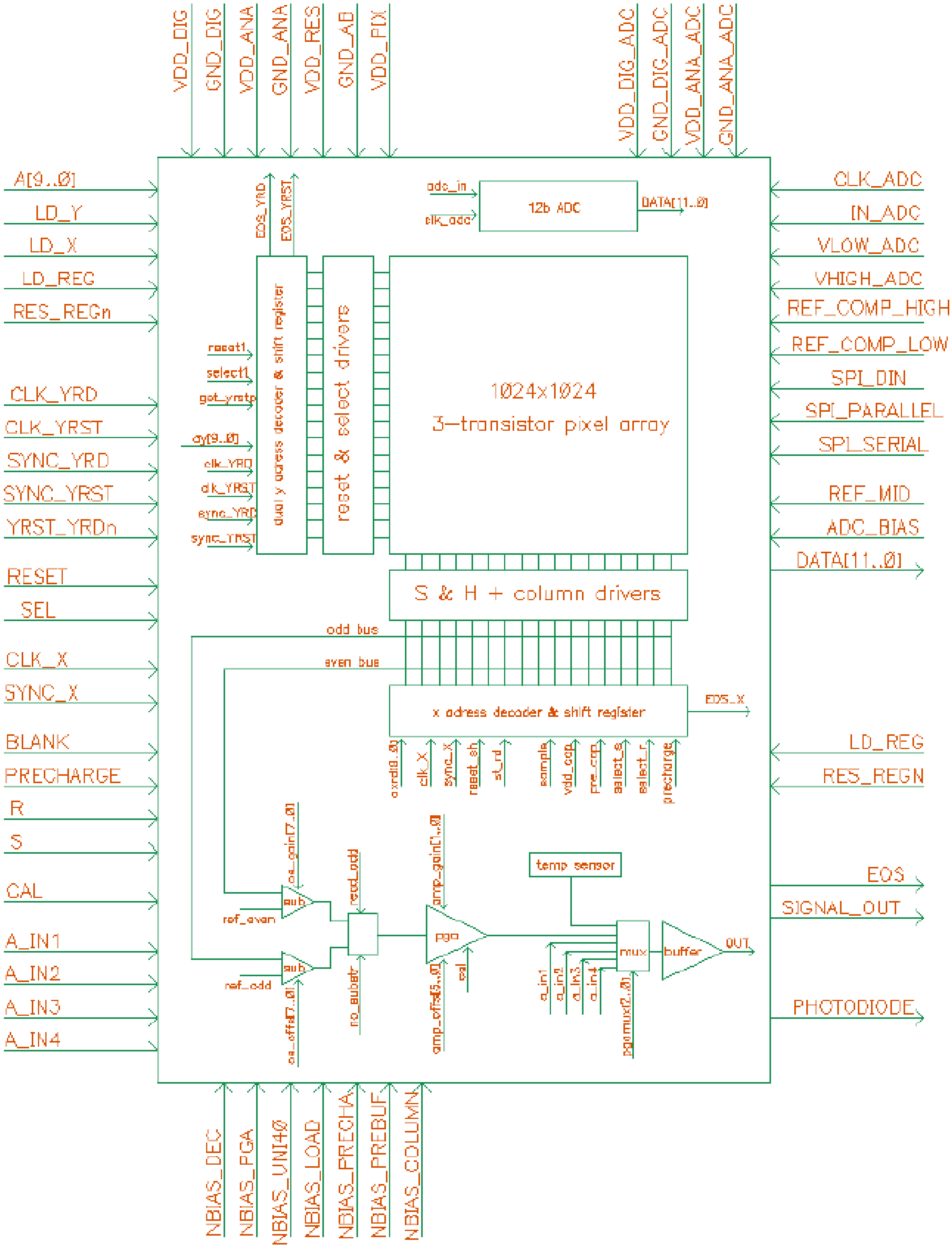

Figure 4-1 : HAS2 block diagram

4.2.Devices description

Part type:	HAS2
Manufacturer:	ON Semiconductor
Package:	JLCC84
Tested Samples:	s/n704, s/n722, s/ n017
Backside marking:	NOIH2SM1000A HHC (Engineering Model)
	NOIH2SM1000S-HWC (Flight Model without glass lid)

For Engineering Model devices, a burn-in 168 hours 125°C has been performed prior to irradiation.

All the devices were irradiated without glass lid.

4.3.Samples identification

Sample s/n704 is an engineering model with date code 110414 (April 14, 2011).

Sample s/n722 is an engineering model with date code 110414 (April 14, 2011) which has been submitted to 3.9E+12 neutrons(1 MeV)cm^2 prior to heavy ion irradiation. Neutron campaign had been performed on December 7th 2011, i.e. 6 months before the heavy ion campaign.

Sample s/n017 is a windowless flight model with date code NAA1148 (week 48, 2011).

2 samples (s/n 679 and s/n741) irradiated up to 55.1 krad prior to heavy ion test campaign were initially included in the test plan. Unfortunately, those parts have been destroyed during the glass de-capsulation process.

All the 3 samples are coming from the same silicon wafer lot P29506.1.

5. IRRADIATION FACILITY

Irradiation has been performed at UCL (Université Catholique de Louvain - Belgium) on the Heavy Ion Facility (HIF) line, using cocktail n°2. Cocktail n°2 provides the following beams:

Ion	*DUT energy [MeV]*	*Range [µm Si]*	*LET [MeV.cm²/mg]*
$^{13}C^{4+}$	131	292	1.1
$^{22}Ne^{7+}$	235	216	3
$^{40}Ar^{12+}$	372	117	10.2
$^{58}Ni^{18+}$	567	100	20.4
$^{83}Kr^{25+}$	756	92	32.6

Table 5-1 : UCL cocktail n°2 characteristics

Cocktail n°1 relevant of high LET range has not been used as this LET range is covered by the heavy ion campaign reported in [RD 2].

Irradiations are performed under vacuum with parts delidded in order to provide adequate penetration of the particles through the device active layers. The vacuum chamber is shown below.

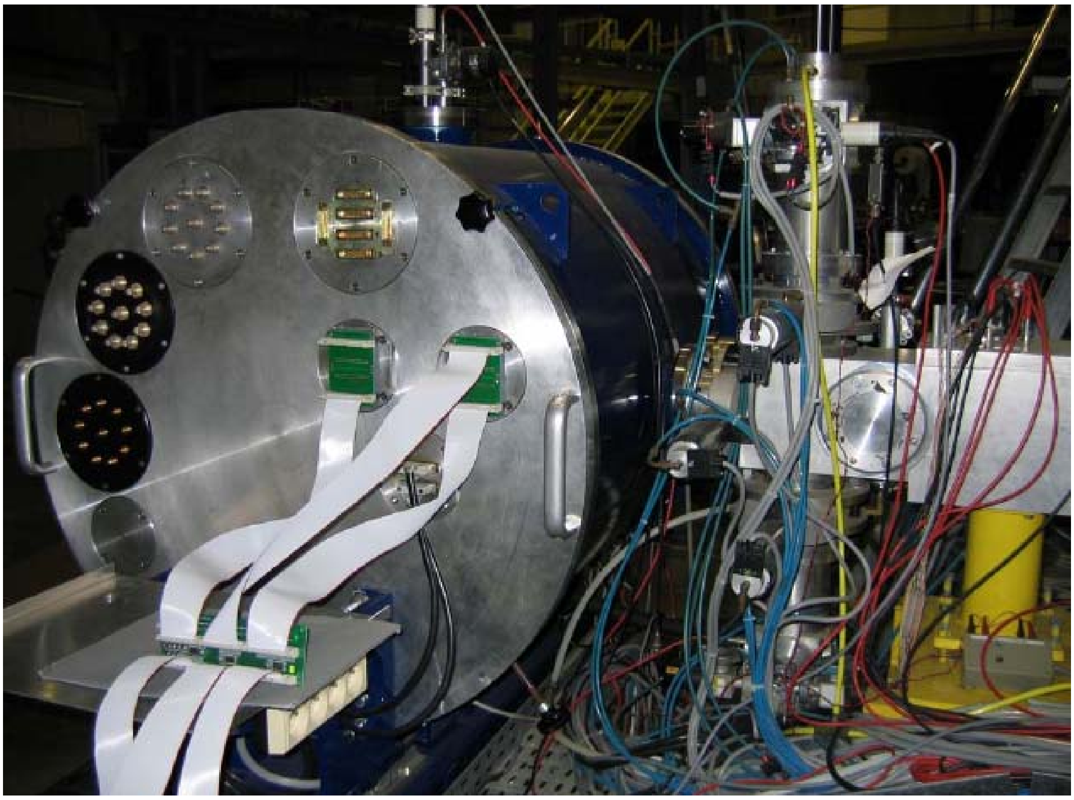

Figure 5-1 : Ion beam vacuum chamber

Depending on vacuum initial conditions, the complete vacuum (1.3E-04 mbar) takes between ten and thirty minutes pumping. Within the same cocktail, it takes only a few minutes to change from one ion to another. The homogeneity of the beam is ± 10 % on a 25 mm diameter. Dosimetry is performed using a Faraday cup, and two parallel plate avalanche counters. A laser pattern calibrated on the beam axis is used to place the DUT in the middle of the beam.

6. TEST SETUP

The irradiations and electrical characterizations have been performed at room temperature. Image acquisition was carried out by ON Semiconductor using dedicated driving boards and acquisition system. The whole setup had the capability to operate the device inside the vacuum chamber under beam flux. The figure hereafter presents the geometry of the irradiation setup. The dimensions of the radiation board and proximity electronics are compatible with the vacuum chamber. The device can be tilted with respect to beam axis by activating the motor implemented inside the chamber.

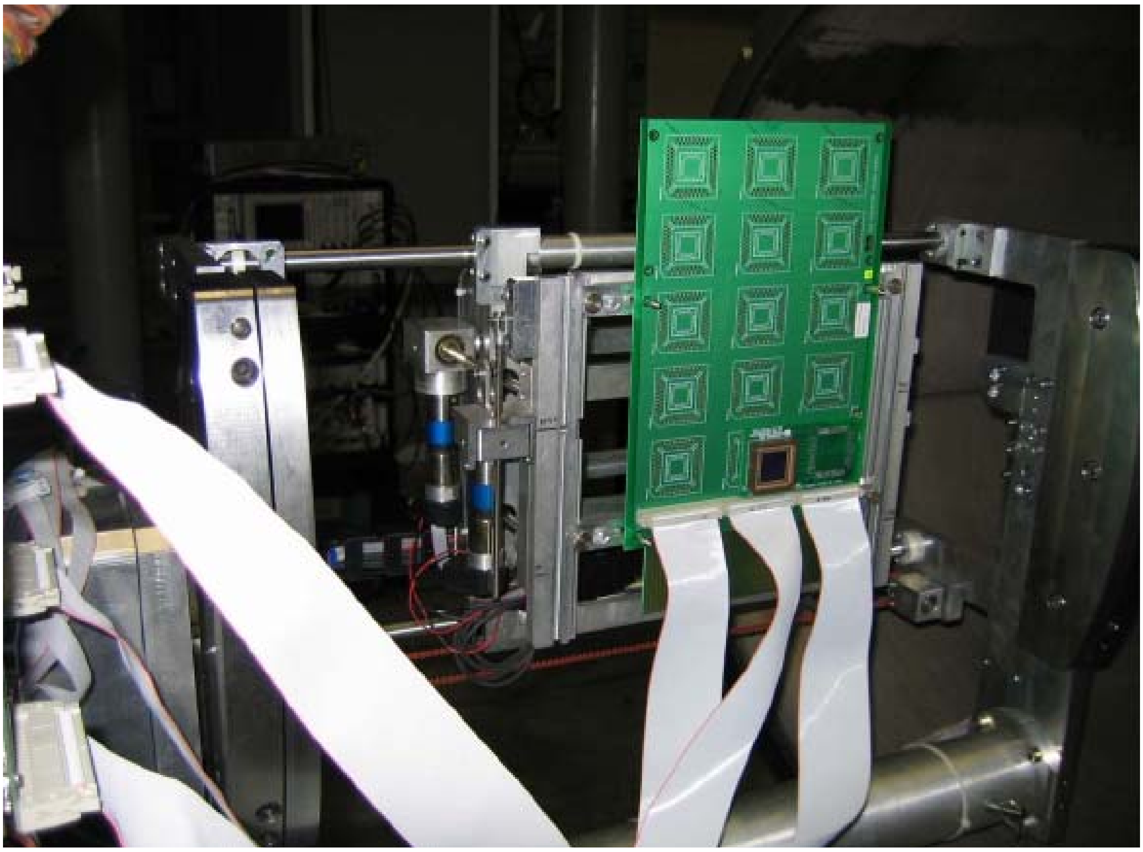

Figure 6-1 : HAS2 PCB in the heavy ion chamber

The purpose of the heavy ion test is to collect particle-induced upset events occurring in the HAS2 pixel array and in his registers. Movies of several images are stored. Each movie contains several images under beam and a few images in darkness (beam OFF) at the beginning and end of the movies.

HAS2 is operated under beam in Hard Reset condition to eliminate lag effects.

During image acquisition under beam flux, the test chamber is placed in darkness to avoid light to be captured by the sensor.

Both DR and NDR mode are investigated (for details on readout modes refer to [RD 1]. In DR mode, full frame images are acquired with a frame rate of 5 image/s (around 150 images per movie). In NDR mode, full frames are grabbed with a frame rate of 2.5 images/s (around 3x150 images per movie including reference, video, and final image).

In DR mode, the integration time is 16 ms. In NDR mode, the integration time is 200 ms (shorter integration time is not possible in this mode on the test setup).

In each movie, mode of operation is refreshed at each frame. The rolling shutter scheme is applied according to 2 addressing modes:

- addressing per line,
- addressing per frame.

The operation of the sensor in these two modes is detailed here after.

The rolling shutter scheme involves two line address pointers called Y-Readout (YRD) and Y-Reset (YRST) pointers. Integration time is based on the time shift between these two pointers (refer to Figure 6-2). For instance, the integration time of 16 ms used in DR mode implies a shift of 80 lines between Reset and Video rolling pointers.

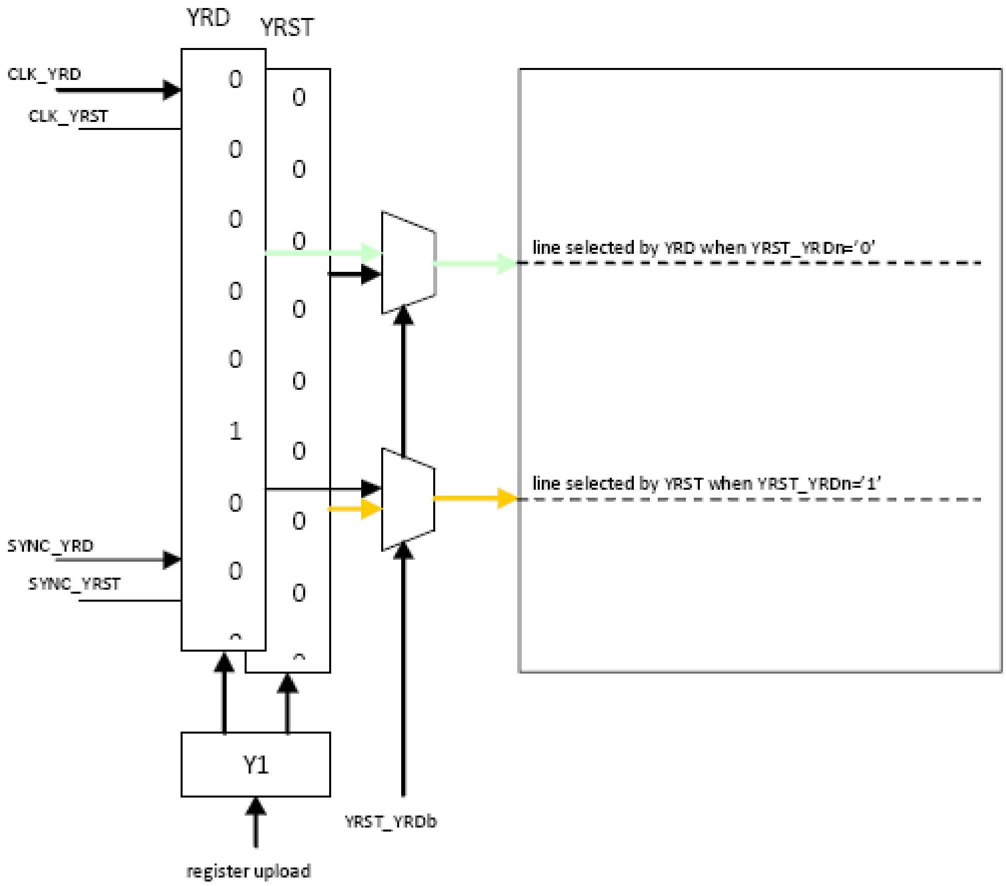

Figure 6-2 : Line Addressing Structures: YRD and YRST shift register pointers

Addressing per line means that the address of each line is uploaded in the Y1 programmable start-of-scan register.

Addressing per frame means that only the address of the 1st line of the frame is uploaded in Y1. The next lines are scanned by clocking the Y-address shift registers (incremental addressing). Previous testing has shown that image corruption can occur under heavy ions flux in this operating mode. A change in the density of particle induced events has been observed related to variation of integration time within a single frame. This behaviour is likely due to Y address pointers errors (whether Reset or Video pointer) inducing modification of the integration time on portion(s) of the image. Corrupted images can be counted and cross section can be extracted. The cross section can be plotted versus the applied heavy ion effective LET (see § 7). NDR mode requires both reference level and video level to be acquired in order to get the final image (after subtraction). The effect of heavy ions on reference image and video image can be observed separately. In DR mode, only the final image is extracted from the sensor. In this case, the effect of heavy ion in readout and reset shift registers cannot be separated (combined effect).

The camera system consists in 4 main components (Figure 6-3). The boards implemented in the system are detailed hereafter:

- A digital controller runs the image sensor controller, the frame grabber and the communication to a PC.
- A cable interface board contains the controllable power supplies, cable line drivers to drive the control signals to the DUT and receivers that receive the video signal from the DUT.
- A cable receiver board receives the driving signals from the controller and also contains buffers to drive the video signal to the 5 meter long cable.
- A radiation/burn-in board contains the DUT. The DUT returns a video signal to the controller.

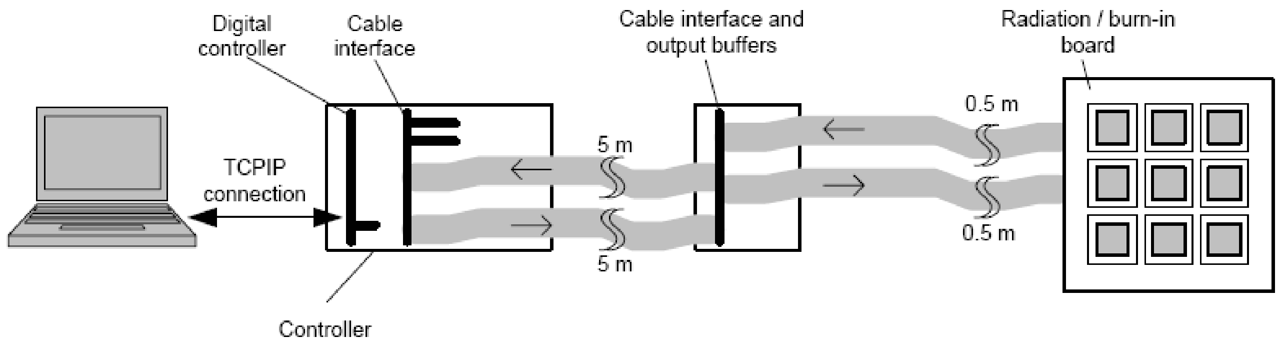

Figure 6-3 : Overview of the HAS2 test setup

The system operates one sample at nominal frequency. Read-back of the images is provided at nominal operating frequency. If a sustained transfer of images is not possible provisions are made to record a sequence of at least 256 images at nominal image sensor speed. A cable of at least 2 m is required between the driving system and the radiation board. The harnessing is compatible with the available feed-troughs of the vacuum chamber.

During irradiation the device supply currents are monitored separately. In case of latch-up or device failure, the following parameters can be logged: power supply where the latch-up condition occurred, time when the condition occurred, and latch-up current. In case of latch-up the current supplied to the device is limited to a safe value in order to prevent damage.

7. EXPERIMENTAL RESULTS

7.1. Run list preparation

The run list was built according to previous data gathered from HAS2 heavy ion testing. Experimental results presented in [RD 2] show that SEE sensitivity can be split in two groups:

- very low sensitivity of configuration registers (DR/NDR mode register, output address MUX register, offset registers),
- moderate sensitivity of FPA line/column address registers.

According to these results, short runs were performed in DR mode for detecting line/column address corruption while longer runs at doubled flux were performed in NDR mode for checking errors in the configuration registers. These long runs were also providing information on the line/column address corruption rate in NDR mode. NDR was preferred as DR mode is the default readout mode of the sensor.

7.2. Detailed run list and error counts

The runs presented in Table 7-1 were performed. 3510 images were stored in DR mode (final images) and 6750 images were stored in NDR mode (including reference, video, and final images). The images are available in TIFF format as full frame image of 2 Mbytes size.

Frame events mean count is presented in Table 7-1.

Register upset count and cross section are presented in Table 7-2.

The upset cross section of the address shift registers is calculated according to the errors counted during the movie divided by the relevant heavy ion fluence. This fluence is obtained considering the heavy ion flux Φ, the number of images under flux N_{Φ}, and the duration necessary to acquire a full frame image. The duration considered herein is 200 ms and corresponds to the time needed to scan all the addresses of a single register (whether reset or readout register). In DR mode, reset register and readout register are used almost simultaneously during 200 ms (only 16 ms time shift due to integration time). In NDR mode, only one register (whether reset or readout register – in the case of ON Semi test set-up only the reset register is selected) is used during 200 ms to scan the whole lines and get the reference image, and then scanned again during another 200 ms to get the video image. For both DR and NDR mode, the relevant duration to get a final image is 200 ms. Address registers upset cross section is calculated using the following formula:

$$\sigma_{address\_register} = Error\_count / \left(N_{\Phi} \times \Phi \times T_{image\_acquisition}\right)$$

The upset cross section of the configuration registers is calculated considering the duration while data corresponding to 1 image are transferred, i.e. 216 ms in the case of DR mode and 400ms in the case of NDR mode. Configuration registers upset cross section is calculated using the following formula:

$$\sigma_{configuration\_register} = Error\_count / \left(N_{\Phi} \times \Phi \times T_{data\_transfer}\right)$$

Table 7-1: Run list for Single Event Effects characterization - Frame events mean count

Test run N°	Sample	Ion	Energy [MeV]	Range [µm Si]	LET [MeV/mg.cm²]	Incidence Angle [deg]	Effective LET [MeV/mg.cm²]	Flux [p/cm²/s]	Irradiation Time [s]	Effective Fluence [p/cm²]	readout mode	addressing mode	integration time [ms]	purpose	Acquisition setup	Frame events mean count [SET/frame]
0	A	$^{83}Kr^{25+}$	756	92	32.6	0	32.6	4000	25	1.00E+05	DR	per line	16	check for address register error check for mode, Offset, MUX error	soft reset 80 lines	218
1	A	$^{83}Kr^{25+}$	756	92	32.6	0	32.6	4000	25	1.00E+05	DR	per line	16	check for address register error check for mode, Offset, MUX error	100 images hard reset 80 lines integration time	218
2	A	$^{83}Kr^{25+}$	756	92	32.6	0	32.6	4000	25	1.00E+05	DR	per frame	16	check for address register error check for mode, Offset, MUX error	120 images hard reset 80 lines integration time	218
3	A	$^{83}Kr^{25+}$	756	92	32.6	0	32.6	8000	200	1.60E+06	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x60 images hard reset 1k lines integration time	5440
4	A	$^{83}Kr^{25+}$	756	92	32.6	45	46.1	4000	25	7.07E+04	DR	per line	16	check for address register error check for mode, Offset, MUX error	120 images hard reset 80 lines integration time	154
5	A	$^{83}Kr^{25+}$	756	92	32.6	45	46.1	4000	25	7.07E+04	DR	per frame	16	check for address register error check for mode, Offset, MUX error	120 images hard reset 80 lines integration time	154
6	A	$^{83}Kr^{25+}$	756	92	32.6	45	46.1	8000	200	1.13E+06	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x60 images hard reset 1k lines integration time	3847
7	A	$^{83}Kr^{25+}$	756	92	32.6	60	65.2	4000	25	5.00E+04	DR	per line	16	check for address register error check for mode, Offset, MUX error	120 images hard reset 80 lines integration time	109
8	A	$^{83}Kr^{25+}$	756	92	32.6	60	65.2	4000	25	5.00E+04	DR	per frame	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	109
9	A	$^{83}Kr^{25+}$	756	92	32.6	60	65.2	8000	200	8.00E+05	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x60 images hard reset 1k lines integration time	2720
10	A	$^{58}Ni^{18+}$	567	100	20.4	0	20.4	4000	25	1.00E+05	DR	per line	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
11	A	$^{58}Ni^{18+}$	567	100	20.4	0	20.4	4000	25	1.00E+05	DR	per frame	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
12	A	$^{58}Ni^{18+}$	567	100	20.4	0	20.4	8000	200	1.60E+06	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x60 images hard reset 1k lines integration time	5440
13	A	$^{40}Ar^{12+}$	372	117	10.2	0	10.2	4000	25	1.00E+05	DR	per line	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
14	A	$^{40}Ar^{12+}$	372	117	10.2	0	10.2	4000	25	1.00E+05	DR	per frame	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
15	A	$^{40}Ar^{12+}$	372	117	10.2	0	10.2	8000	200	1.60E+06	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x60 images hard reset 1k lines integration time	5440
16	A	$^{22}Ne^{7+}$	235	216	3	0	3	4000	25	1.00E+05	DR	per line	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
17	A	$^{22}Ne^{7+}$	235	216	3	0	3	4000	25	1.00E+05	DR	per frame	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
18	A	$^{22}Ne^{7+}$	235	216	3	0	3	8000	200	1.60E+06	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x50 images hard reset 1k lines integration time	5440
19	A	$^{13}C^{4+}$	131	292	1.1	0	1.1	4000	25	1.00E+05	DR	per line	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
20	A	$^{13}C^{4+}$	131	292	1.1	0	1.1	4000	25	1.00E+05	DR	per frame	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
21	A	$^{13}C^{4+}$	131	292	1.1	0	1.1	8000	200	1.60E+06	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x50 images hard reset 1k lines integration time	5440

Table 7-1 (cont'): Run list for Single Event Effects characterization - Frame events mean count

Test run N°	*Sample*	*Ion*	*Energy [MeV]*	*Range [µm Si]*	*LET [MeV/mg.cm²]*	*Incidence Angle [deg]*	*Effective LET [MeV/mg.cm²]*	*Flux [p/cm²/s]*	*Irradiation Time [s]*	*Effective Fluence [p/cm²]*	*readout mode*	*addressing mode*	*integration time [ms]*	*purpose*	*Acquisition setup*	*Frame events mean count [SET/frame]*
22	C	$^{83}Kr^{25+}$	756	92	32.6	0	32.6	4000	25	1.00E+05	DR	per line	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
23	C	$^{83}Kr^{25+}$	756	92	32.6	0	32.6	4000	25	1.00E+05	DR	per frame	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
24	C	$^{83}Kr^{25+}$	756	92	32.6	0	32.6	6000	300	1.80E+06	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x50 images hard reset 1k lines integration time	4080
25	C	$^{58}Ni^{18+}$	567	100	20.4	0	20.4	4000	25	1.00E+05	DR	per line	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
26	C	$^{58}Ni^{18+}$	567	100	20.4	0	20.4	4000	25	1.00E+05	DR	per frame	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
26B	C	$^{58}Ni^{18+}$	567	100	20.4	0	20.4	4000	25	1.00E+05	DR	per frame	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
27	C	$^{58}Ni^{18+}$	567	100	20.4	0	20.4	8000	200	1.60E+06	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x50 images hard reset 1k lines integration time	5440
28	C	$^{40}Ar^{12+}$	372	117	10.2	0	10.2	4000	25	1.00E+05	DR	per line	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
29	C	$^{40}Ar^{12+}$	372	117	10.2	0	10.2	4000	25	1.00E+05	DR	per frame	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
30	C	$^{40}Ar^{12+}$	372	117	10.2	0	10.2	8000	200	1.60E+06	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x50 images hard reset 1k lines integration time	5440
31	C	$^{22}Ne^{7+}$	235	216	3	0	3	4000	25	1.00E+05	DR	per line	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
32	C	$^{22}Ne^{7+}$	235	216	3	0	3	4000	25	1.00E+05	DR	per frame	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
33	C	$^{22}Ne^{7+}$	235	216	3	0	3	8000	200	1.60E+06	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x50 images hard reset 1k lines integration time	5440
34	B	$^{83}Kr^{25+}$	756	92	32.6	0	32.6	3200	25	8.00E+04	DR	per line	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	174
34B	B	$^{83}Kr^{25+}$	756	92	32.6	0	32.6	3200	25	8.00E+04	DR	per frame	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	174
35	B	$^{83}Kr^{25+}$	756	92	32.6	0	32.6	8000	200	1.60E+06	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x50 images hard reset 1k lines integration time	5440
36	B	$^{40}Ar^{12+}$	372	117	10.2	0	10.2	4000	25	1.00E+05	DR	per frame	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
37	B	$^{40}Ar^{12+}$	372	117	10.2	0	10.2	8000	200	1.60E+06	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x50 images hard reset 1k lines integration time	5440
38	B	$^{22}Ne^{7+}$	235	216	3	0	3	4000	25	1.00E+05	DR	per frame	16	check for address register error check for mode, Offset, MUX error	150 images hard reset 80 lines integration time	218
39	B	$^{22}Ne^{7+}$	235	216	3	0	3	8000	200	1.60E+06	NDR	per frame	200	check for address register error check for mode, Offset, MUX error	3x50 images hard reset 1k lines integration time	5440

Table 7-2: Run list with register upset count

Test run N°	*Sample*	*Ion*	*LET [MeV/mg.cm²]*	*Incidence Angle [deg]*	*Effective LET [MeV/mg.cm²]*	*Flux [p/cm²/s]*	*Irradiation Time [s]*	*Effective Fluence [p/cm²]*	*readout mode*	*addressing mode*	*integration time [ms]*	*Y-address register error count*	*configuration registers error count*	*start image*	*final image*	*Y-address register error cross section*	*configuration registers error cross section*	*comments*
0	A	$^{83}Kr^{25+}$	32.6	0	32.6	4000	25	1.00E+05	DR	per line	16							
1	A	$^{83}Kr^{25+}$	32.6	0	32.6	4000	25	1.00E+05	DR	per line	16	1		20	99	1.6E-05		*NO UPSET*
2	A	$^{83}Kr^{25+}$	32.6	0	32.6	4000	25	1.00E+05	DR	per frame	16	11		22	119	1.4E-04		UPSETS
3	A	$^{83}Kr^{25+}$	32.6	0	32.6	8000	200	1.60E+06	NDR	per frame	200	50	1	5	152	2.1E-04	2.1E-06	UPSETS ON ADDRESS REGISTERS *NO UPSET ON CONFIG REGISTERS*
4	A	$^{83}Kr^{25+}$	32.6	45	46.1	4000	25	7.07E+04	DR	per line	16	1		16	119	1.7E-05		*NO UPSET*
5	A	$^{83}Kr^{25+}$	32.6	45	46.1	4000	25	7.07E+04	DR	per frame	16	9		17	119	1.6E-04		UPSETS
6	A	$^{83}Kr^{25+}$	32.6	45	46.1	8000	200	1.13E+06	NDR	per frame	200	67	1	5	180	3.4E-04	2.5E-06	UPSETS ON ADDRESS REGISTERS 1 UPSET ON CONFIG REGISTERS (MUX)
7	A	$^{83}Kr^{25+}$	32.6	60	65.2	4000	25	5.00E+04	DR	per line	16	1	1	17	119	3.3E-05		1 UPSET (single line)
8	A	$^{83}Kr^{25+}$	32.6	60	65.2	4000	25	5.00E+04	DR	per frame	16	11		15	148	2.8E-04		UPSETS
9	A	$^{83}Kr^{25+}$	32.6	60	65.2	8000	200	8.00E+05	NDR	per frame	200	55	1	6	180	4.0E-04	4.8E-06	UPSETS ON ADDRESS REGISTERS *NO UPSET ON CONFIG REGISTERS*
10	A	$^{58}Ni^{18+}$	20.4	0	20.4	4000	25	1.00E+05	DR	per line	16	1		14	142	9.8E-06		NO UPSET
11	A	$^{58}Ni^{18+}$	20.4	0	20.4	4000	25	1.00E+05	DR	per frame	16	3		17	137	3.1E-05		UPSETS
12	A	$^{58}Ni^{18+}$	20.4	0	20.4	8000	200	1.60E+06	NDR	per frame	200	11	1	4	154	4.6E-05	2.1E-06	UPSETS ON ADDRESS REGISTERS *NO UPSET ON CONFIG REGISTERS*
13	A	$^{40}Ar^{12+}$	10.2	0	10.2	4000	25	1.00E+05	DR	per line	16	1		16	136	1.0E-05		*NO UPSET*
14	A	$^{40}Ar^{12+}$	10.2	0	10.2	4000	25	1.00E+05	DR	per frame	16	1		15	135	1.0E-05		*NO UPSET*
15	A	$^{40}Ar^{12+}$	10.2	0	10.2	8000	200	1.60E+06	NDR	per frame	200	1	1	4	145	4.4E-06	2.2E-06	*NO UPSET*
16	A	$^{22}Ne^{7+}$	3	0	3	4000	25	1.00E+05	DR	per line	16	1		17	137	1.0E-05		*NO UPSET*
17	A	$^{22}Ne^{7+}$	3	0	3	4000	25	1.00E+05	DR	per frame	16	1		20	149	9.7E-06		*NO UPSET*
18	A	$^{22}Ne^{7+}$	3	0	3	8000	200	1.60E+06	NDR	per frame	200	1	1	5	147	4.4E-06	2.2E-06	*NO UPSET*
19	A	$^{13}C^{4+}$	1.1	0	1.1	4000	25	1.00E+05	DR	per line	16	1		16	139	1.0E-05		*NO UPSET*
20	A	$^{13}C^{4+}$	1.1	0	1.1	4000	25	1.00E+05	DR	per frame	16	1		17	119	1.2E-05		*NO UPSET*
21	A	$^{13}C^{4+}$	1.1	0	1.1	8000	200	1.60E+06	NDR	per frame	200	1	1	5	146	4.4E-06	2.2E-06	*NO UPSET*

Table 7-2 (cont'): Run list with register upset count

Test run N°	*Sample*	*Ion*	*LET [MeV/mg.cm²]*	*Incidence Angle [deg]*	*Effective LET [MeV/mg.cm²]*	*Flux [p/cm²/s]*	*Irradiation Time [s]*	*Effective Fluence [p/cm²]*	*readout mode*	*addressing mode*	*integration time [ms]*	*Y-address register error count*	*configuration registers error count*	*start image*	*final image*	*Y-address register error cross section*	*configuration registers error cross section*	*comments*
22	C	$^{83}Kr^{25+}$	32.6	0	32.6	4000	25	1.00E+05	DR	per line	16	1		18	142	1.0E-05		*NO UPSET*
23	C	$^{83}Kr^{25+}$	32.6	0	32.6	4000	25	1.00E+05	DR	per frame	16	7		10	135	7.0E-05		UPSETS
24	C	$^{83}Kr^{25+}$	32.6	0	32.6	6000	300	1.80E+06	NDR	per frame	200	33	1	4	150	1.9E-04	2.9E-06	UPSETS ON ADDRESS REGISTERS *NO UPSET ON CONFIG REGISTERS*
25	C	$^{58}Ni^{18+}$	20.4	0	20.4	4000	25	1.00E+05	DR	per line	16	1		17	149	9.5E-06		*NO UPSET*
26	C	$^{58}Ni^{18+}$	20.4	0	20.4	4000	25	1.00E+05	DR	per frame	16							DELETED
26B	C	$^{58}Ni^{18+}$	20.4	0	20.4	4000	25	1.00E+05	DR	per frame	16	3		13	138	3.0E-05		UPSETS
27	C	$^{58}Ni^{18+}$	20.4	0	20.4	8000	200	1.60E+06	NDR	per frame	200	21	1	1	150	8.8E-05	2.1E-06	UPSETS ON ADDRESS REGISTERS *NO UPSET ON CONFIG REGISTERS*
28	C	$^{40}Ar^{12+}$	10.2	0	10.2	4000	25	1.00E+05	DR	per line	16	1		18	137	1.1E-05		*NO UPSET*
29	C	$^{40}Ar^{12+}$	10.2	0	10.2	4000	25	1.00E+05	DR	per frame	16	1		17	136	1.1E-05		*NO UPSET*
30	C	$^{40}Ar^{12+}$	10.2	0	10.2	8000	200	1.60E+06	NDR	per frame	200	1	1	4	150	4.3E-06	2.1E-06	*NO UPSET*
31	C	$^{22}Ne^{7+}$	3	0	3	4000	25	1.00E+05	DR	per line	16	1		19	138	1.1E-05		*NO UPSET*
32	C	$^{22}Ne^{7+}$	3	0	3	4000	25	1.00E+05	DR	per frame	16	1		17	137	1.0E-05		*NO UPSET*
33	C	$^{22}Ne^{7+}$	3	0	3	8000	200	1.60E+06	NDR	per frame	200	1	1	5	150	4.3E-06	2.2E-06	*NO UPSET*
34	B	$^{83}Kr^{25+}$	32.6	0	32.6	3200	25	8.00E+04	DR	per line	16	1		18	149	1.2E-05		*NO UPSET*
34B	B	$^{83}Kr^{25+}$	32.6	0	32.6	3200	25	8.00E+04	DR	per frame	16	6		19	149	7.2E-05		UPSETS
35	B	$^{83}Kr^{25+}$	32.6	0	32.6	8000	200	1.60E+06	NDR	per frame	200	35	1	3	150	1.5E-04	2.1E-06	UPSETS ON ADDRESS REGISTERS 1 UPSET ON CONFIG REGISTERS
36	B	$^{40}Ar^{12+}$	10.2	0	10.2	4000	25	1.00E+05	DR	per frame	16	1		15	144	9.7E-06		*NO UPSET*
37	B	$^{40}Ar^{12+}$	10.2	0	10.2	8000	200	1.60E+06	NDR	per frame	200	1	1	3	150	4.3E-06	2.1E-06	*NO UPSET*
38	B	$^{22}Ne^{7+}$	3	0	3	4000	25	1.00E+05	DR	per frame	16	1		17	146	9.7E-06		*NO UPSET*
39	B	$^{22}Ne^{7+}$	3	0	3	8000	200	1.60E+06	NDR	per frame	200	1	1	4	150	4.3E-06	2.1E-06	*NO UPSET*

7.3. Observations

7.3.1. Pixel array SET

Heavy ions induced transient signals are generated in the pixel array by direct ionization. The SET spot size is illustrated Figure 7-1 and Figure 7-2 with $^{83}Kr^{25+}$ heavy ion at 0° and 60° beam incidence (DR mode 16 ms integration time). In Figure 7-2, though heavy ion beam is tilted wrt normal incidence, extension in spot size is negligible. Indeed, the size of the spot is driven by the carrier diffusion effect in the epitaxial layer of the sensor. Local interaction of heavy ion is negligible compared to diffusion length.

Some of the SET spots are truncated along line axis. This shape is related to the rolling shutter scheme of 80 lines applied in DR mode to achieve 16 ms integration time. Considering a spot size of 6 pixels, the partial reset or partial readout should affect around 12 % (10/85) of the total events. This figure is in line with the observed density of truncated events (refer to Figure 7-3).

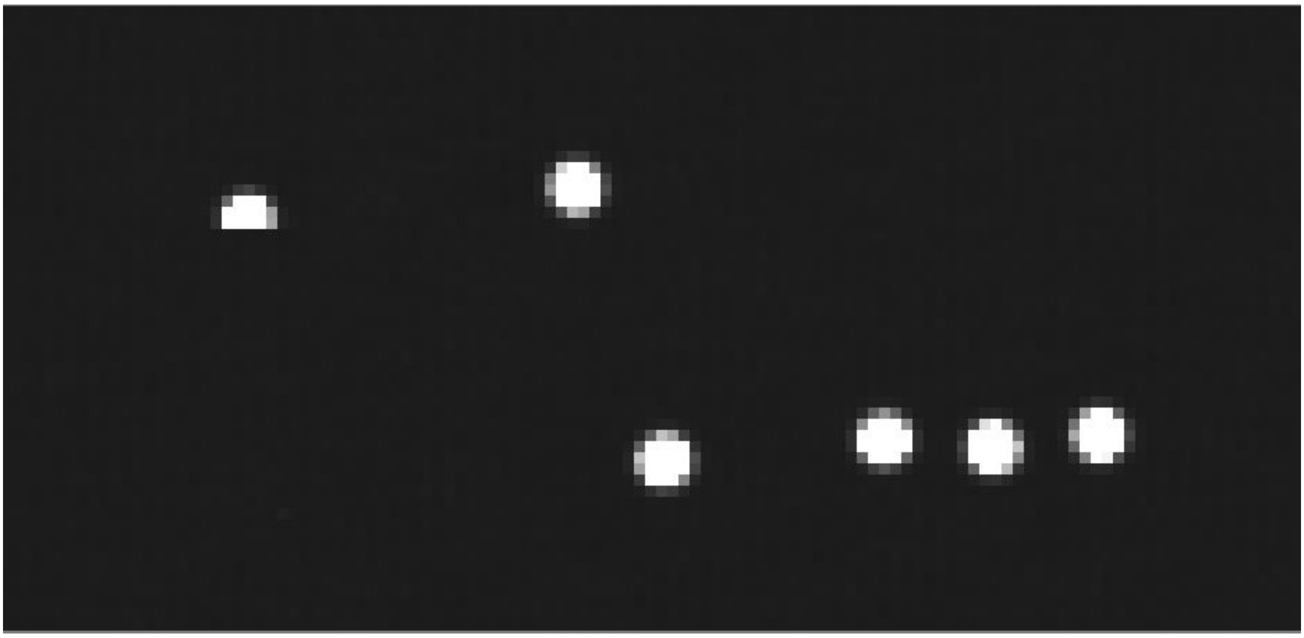

Figure 7-1 : Pixel array SET captured under $^{83}Kr^{25+}$ heavy ion at normal angle

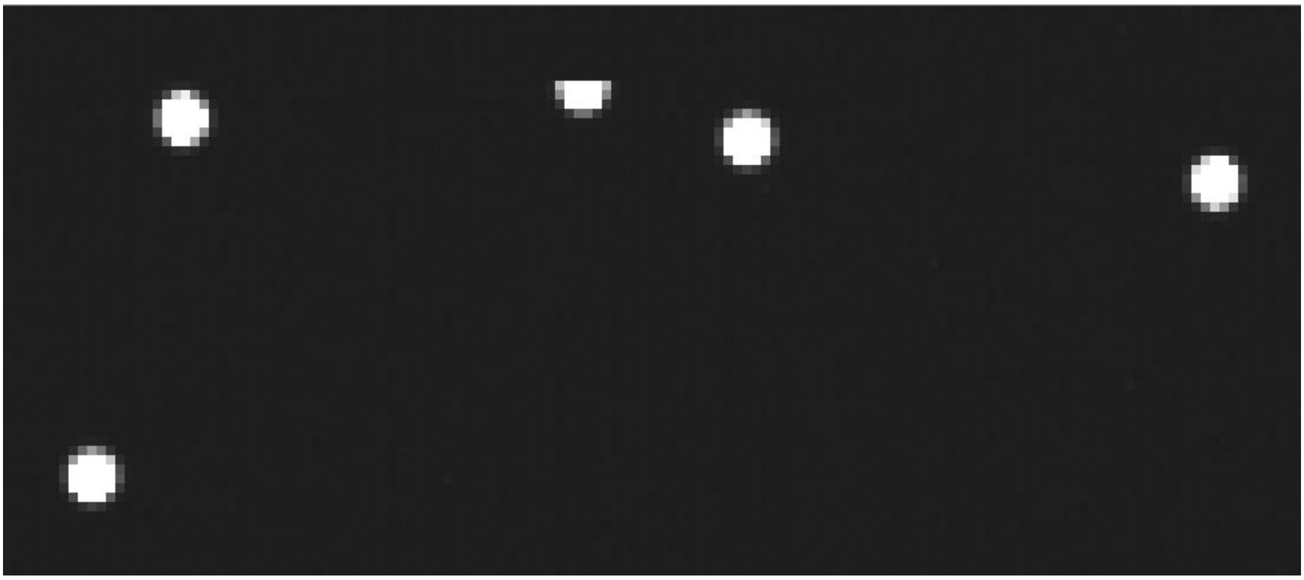

Figure 7-2 : Pixel array SET captured under $^{83}Kr^{25+}$ heavy ion at 60° angle

7.3.2. DR addressing per line operating mode

No corruption has been observed during testing in DR addressing per line operating mode. Changes in spot shape (except the one due to rolling shutter truncation) or changes in spot density have not been detected.

However, one exception was noted: one error appeared on a single line of one of the images of run 7 (effective heavy ion LET of 65.2 MeV/mg/cm²). In Figure 7-4, all the pixels of this line have a signal level slightly higher (~570 LSB) than the normal ones (~460 LSB). This error could be due to heavy ion hit occurring either in the address shift registers (right after the address upload) or in the column amplifier control circuitry (during signal or reference sampling). A change in the PGA gain or offset could be also invoked.

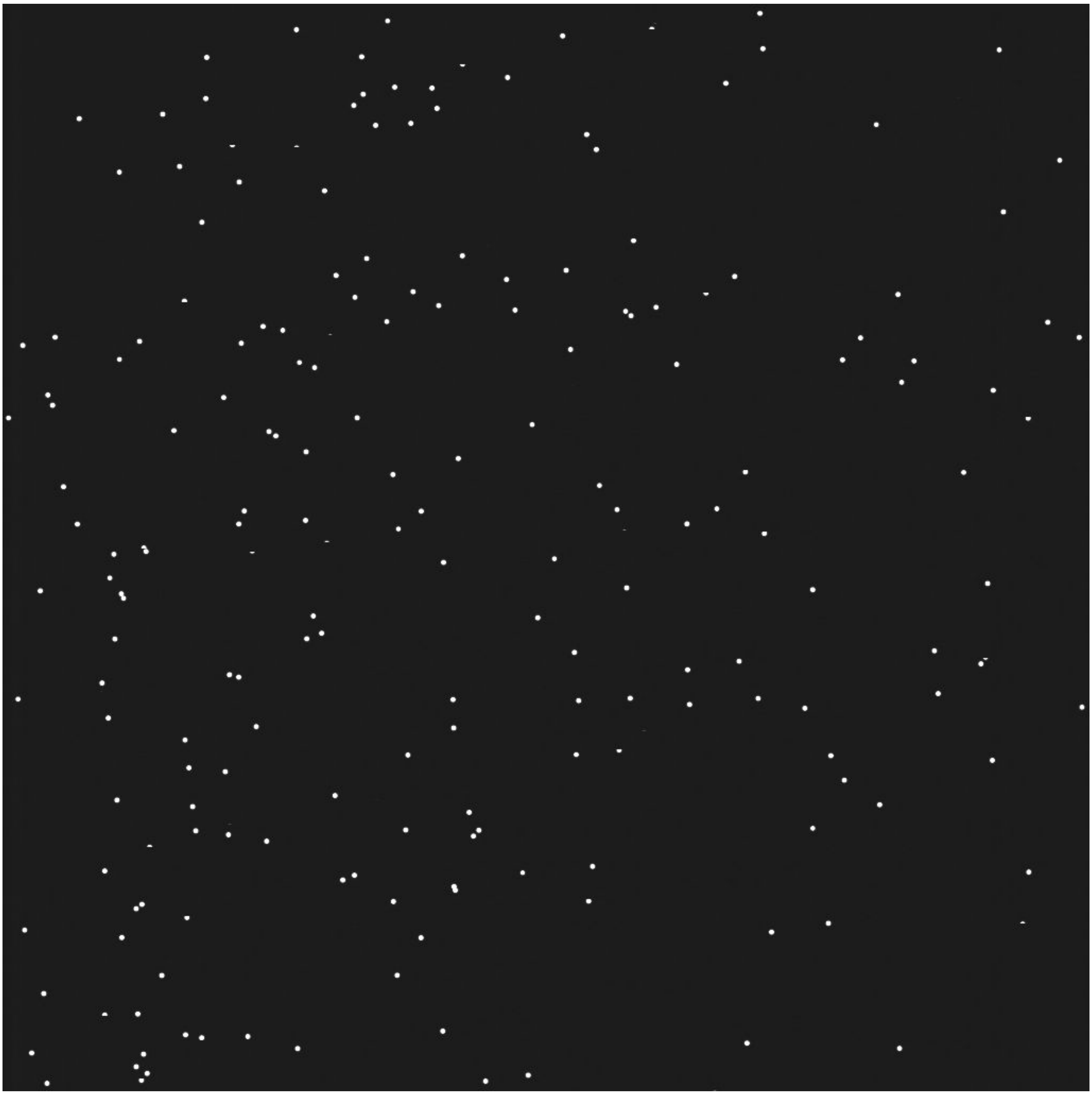

Figure 7-3 : Image of 1024x1024 pixels acquired under $^{83}Kr^{25+}$ heavy ion flux in DR mode with 16 ms integration time and addressing per line operation – no corruption

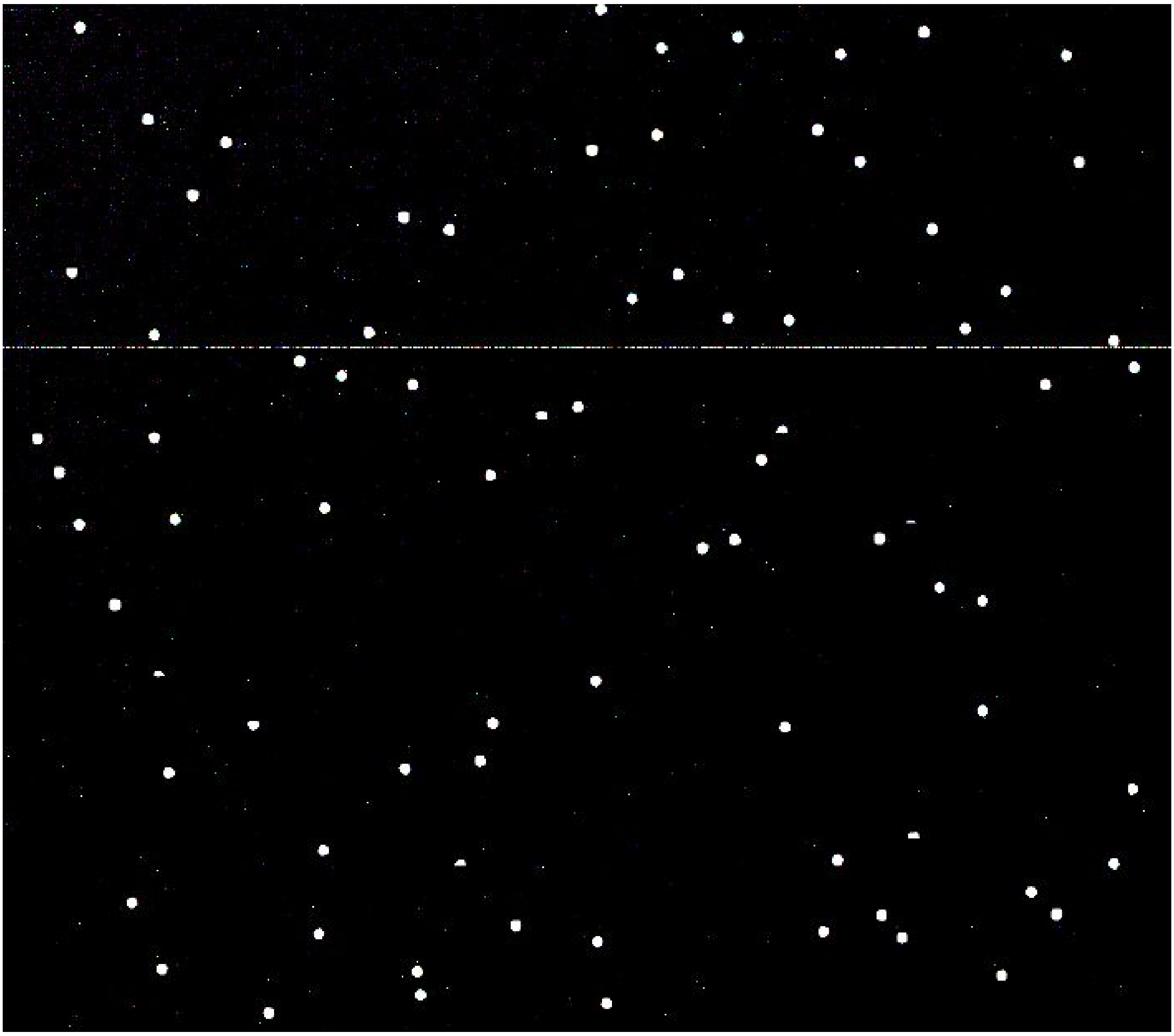

Figure 7-4 : Image acquired under $^{83}Kr^{25+}$ ion beam 60° tilted in DR mode with 16 ms integration time and addressing per line operation – 1 line in error (enhanced contrast)

7.3.3. DR addressing per frame operating mode

Several image corruptions have been observed during DR addressing per frame operating mode testing. Changes in spot amplitude and spot density appeared on several images per movie. Example of the effect on an image is presented in Figure 7-5. The corrupted area exhibits a high density of spots with a low level of signal. The first line and the size of this area are randomly spread over the pixel array. The number of corrupted images increases with heavy ion LET. In some case, more than one SET seems to occur in a single image (Figure 7-6). No corruption has been observed below 10.2 MeV.cm²/mg.

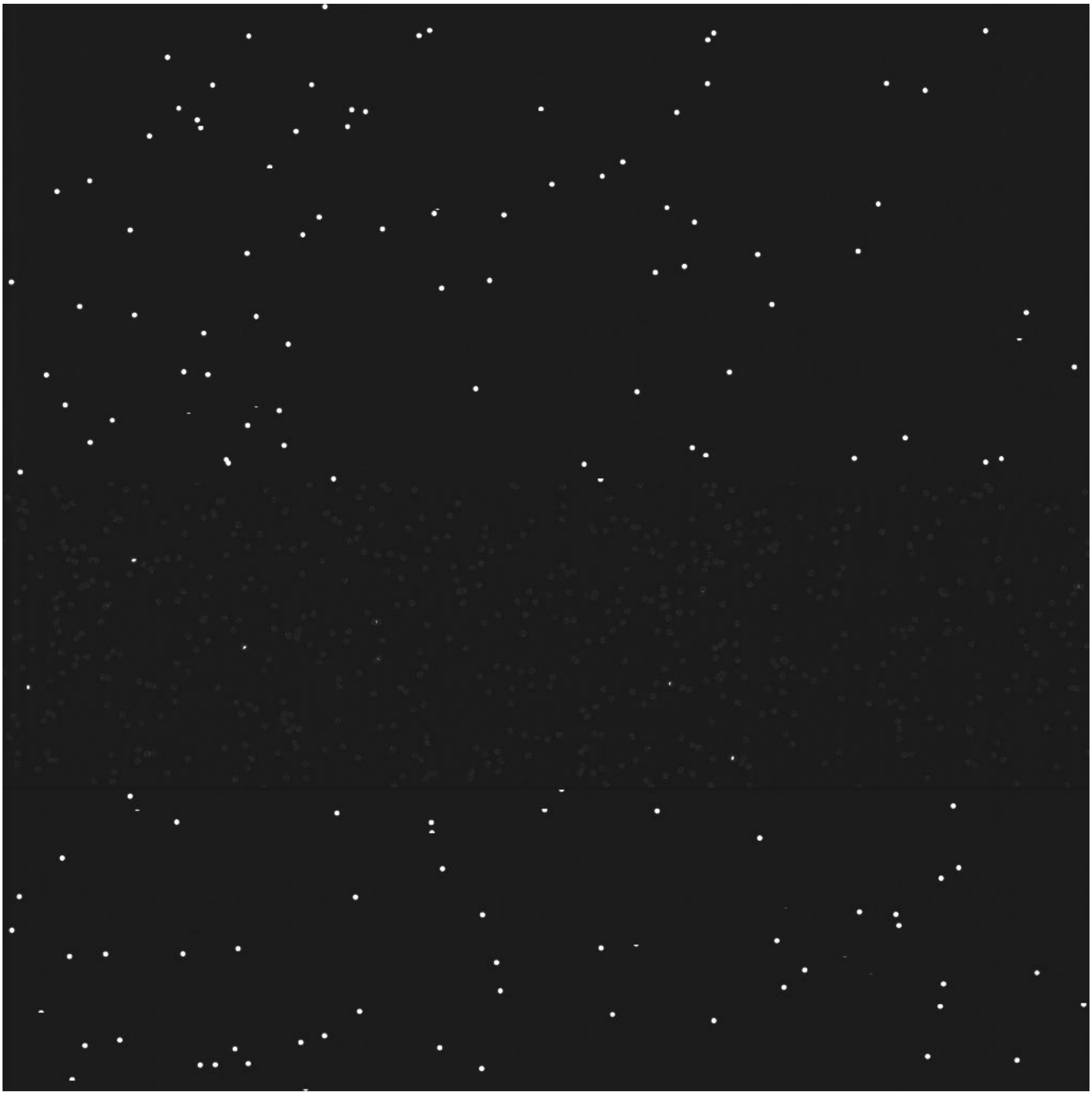

Figure 7-5 : Image acquired under $^{83}Kr^{25+}$ ion beam at 0° in DR mode with 16 ms integration time and addressing per frame operation –corrupted area is observed

Figure 7-6 : Image acquired under $^{83}Kr^{25+}$ ion beam at 0° in DR mode with 16 ms integration time and addressing per frame operation –several corrupted areas observed

7.3.4. NDR addressing per frame operating mode

Several image corruptions have been observed during NDR addressing per frame operating mode testing. Both reference and video full frame images have been scanned. The beam flux is 2 times higher compared to DR testing flux. Integration time is 10 times higher compared to DR testing condition. Consequently, much more SET spots are generated in the video images. Typical image obtained after subtraction is presented in Figure 7-7. Because of the very short time between reset and reference sampling, no pixel array SET spots are captured on the reference image (Figure 7-8).

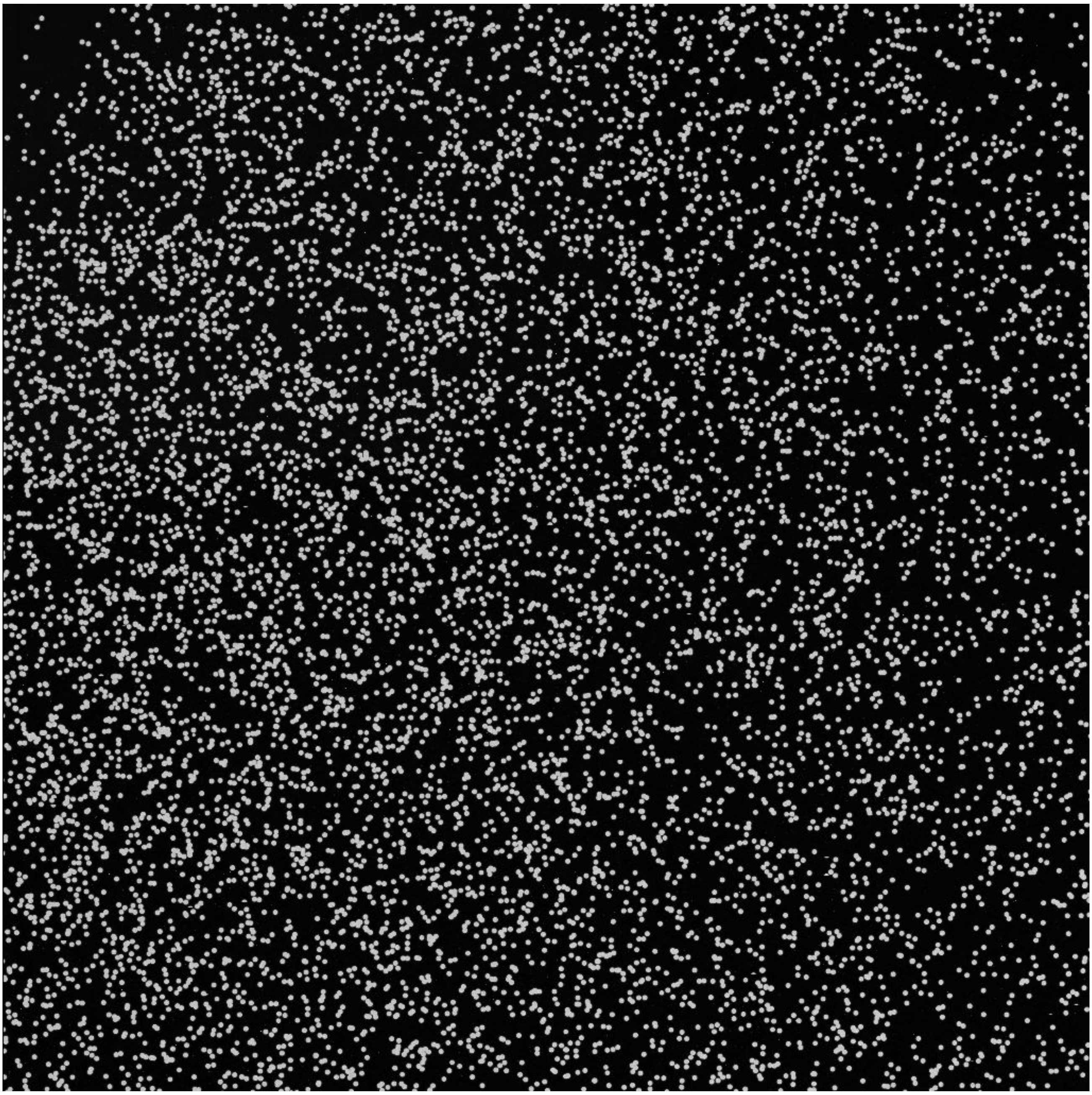

Figure 7-7 : Typical full frame final image acquired under $^{83}Kr^{25+}$ ion beam flux with 200 ms integration time in addressing per frame NDR mode

Corruptions of image acquisition are illustrated in Figure 7-8 for reference image and in Figure 7-9 video image. Similarly as for DR mode, more than one upset can occur in a single frame (for instance in Figure 7-8). The first line and the size of corrupted area are randomly spread over the pixel array. The corrupted areas exhibit changes in spot signal size and spot density. The number of corrupted images increases with heavy ion LET. No corruption has been observed below 10.2 MeV.cm²/mg.

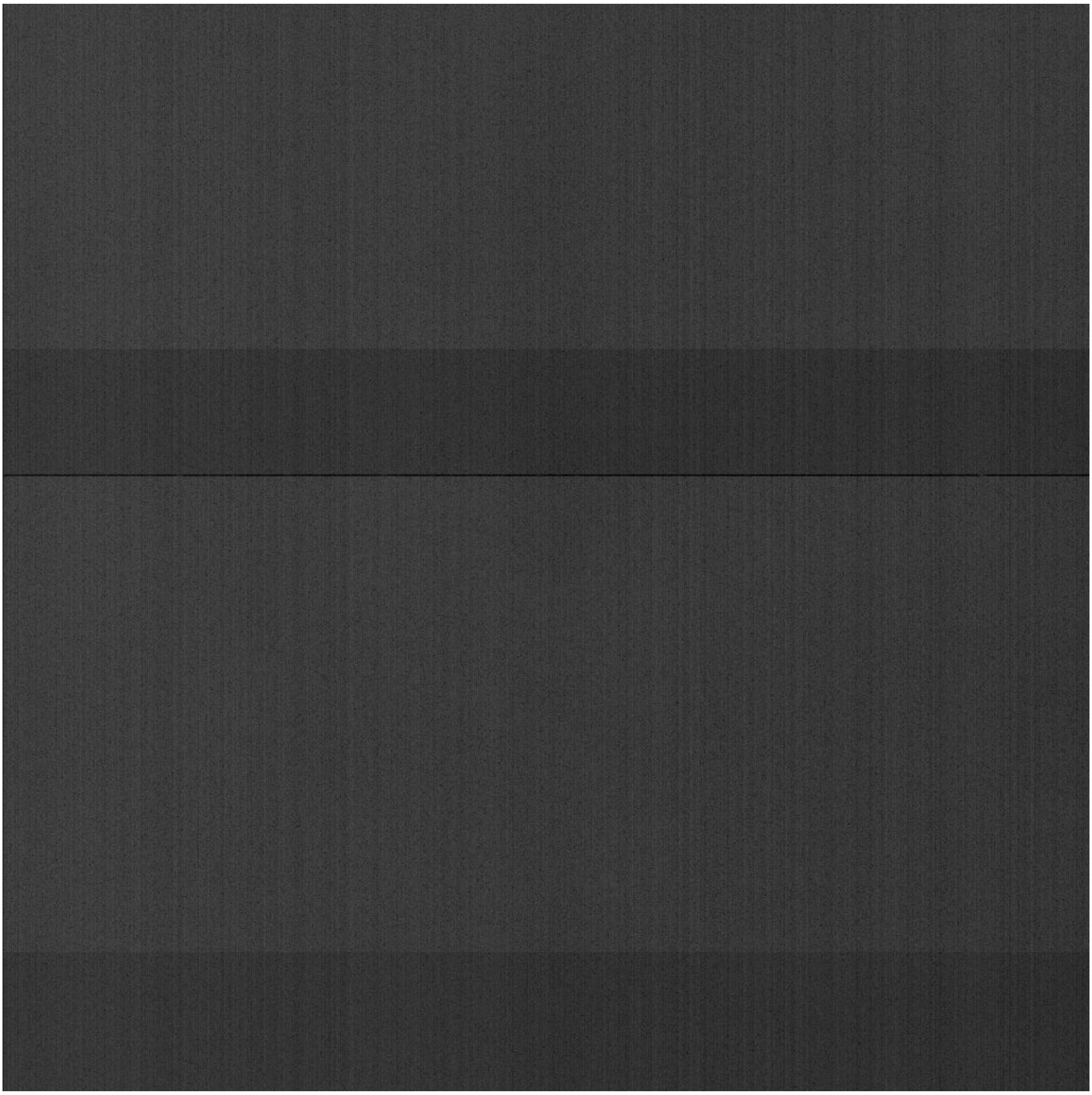

Figure 7-8 : Reference image acquired under $^{83}Kr^{25+}$ ion beam at 200 ms integration time in addressing per frame NDR mode – image partially corrupted (2 upsets)

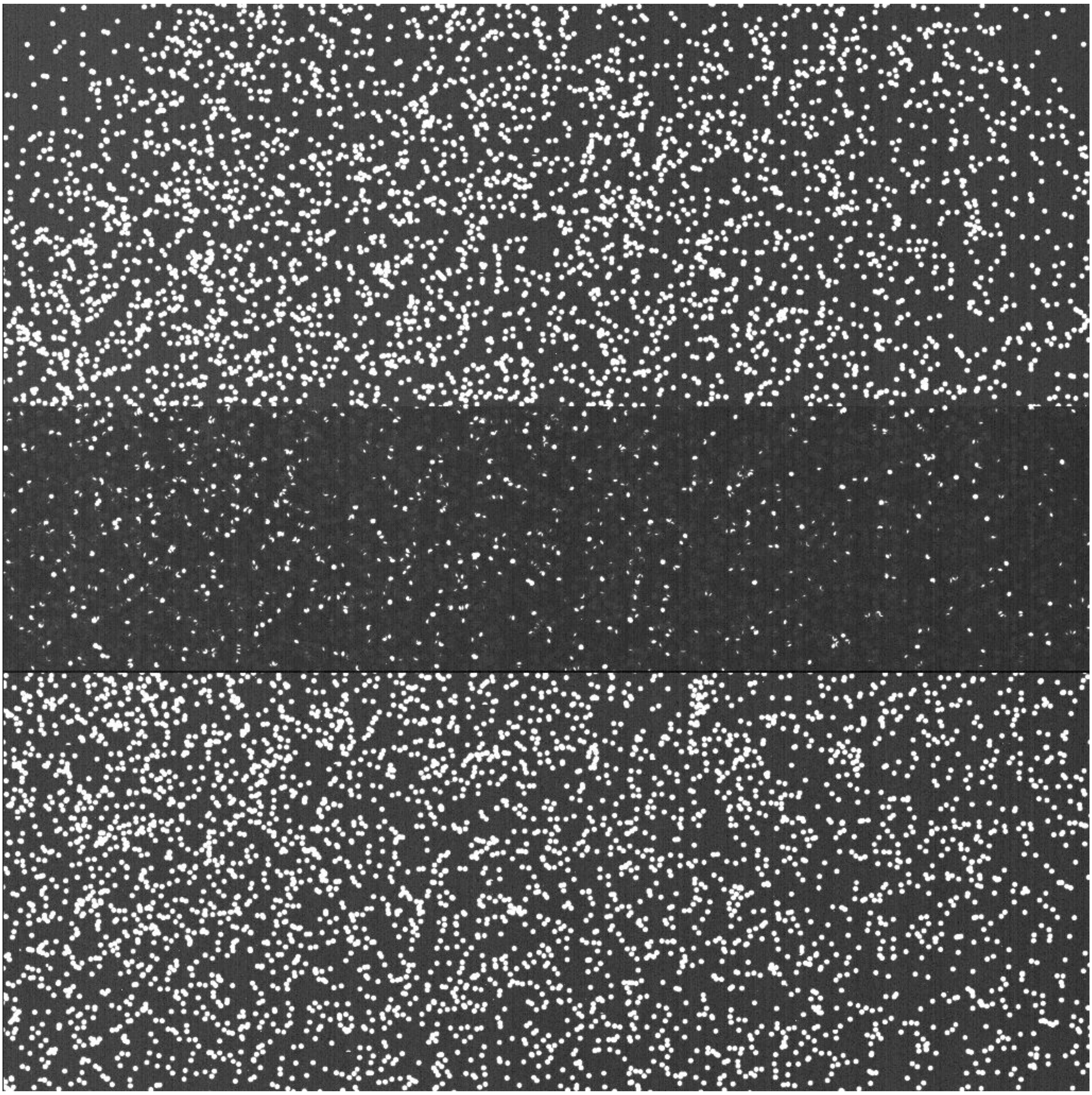

Figure 7-9 : Video levels image acquired under $^{83}Kr^{25+}$ ion beam with 200 ms integration time in addressing per frame NDR mode – image partially corrupted (1 upset)

A few events were captured probably related to an upset in the sensor output multiplexer (or in the PGA offset registers). These events are very much infrequent. Only two have been observed during the whole test campaign at the highest LET level.

One of these events occurred on one single video image acquired under $^{83}Kr^{25+}$ ion beam tilted at 45°. Part of the image was at 4095 LSB (Figure 7-10). This error is likely due to the untimely connection of the MUX output to one of the analogue inputs instead of the pixel array. The other event occurred on one single reference image acquired under $^{83}Kr^{25+}$ ion beam at normal angle. The end of the image was also clamped at 4095 LSB (Figure 7-11).

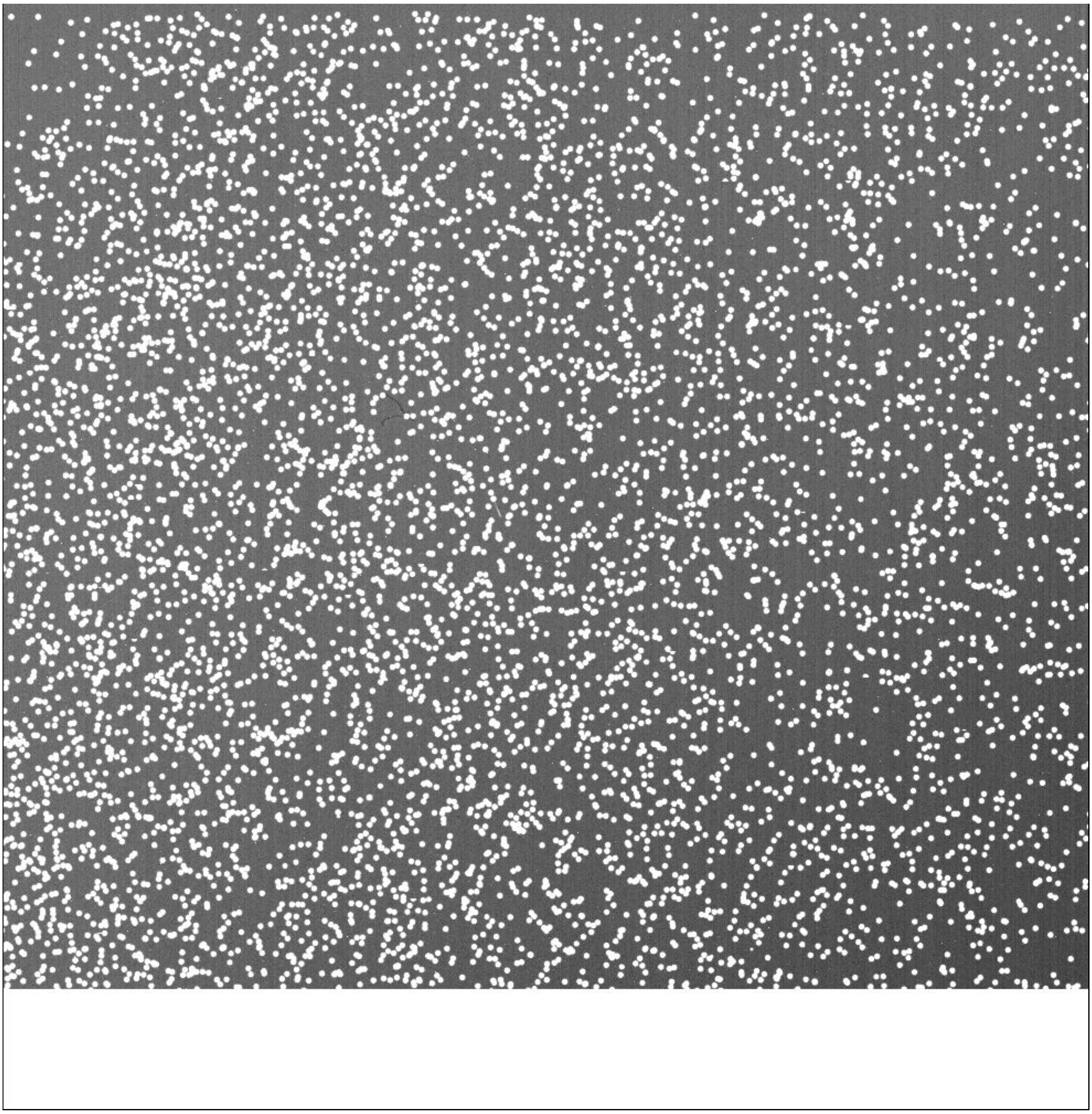

Figure 7-10 : Video levels acquired under $^{83}Kr^{25+}$ ion beam tilted at 45° with 200 ms integration time in addressing per frame NDR mode – image partially at 4095 LSB

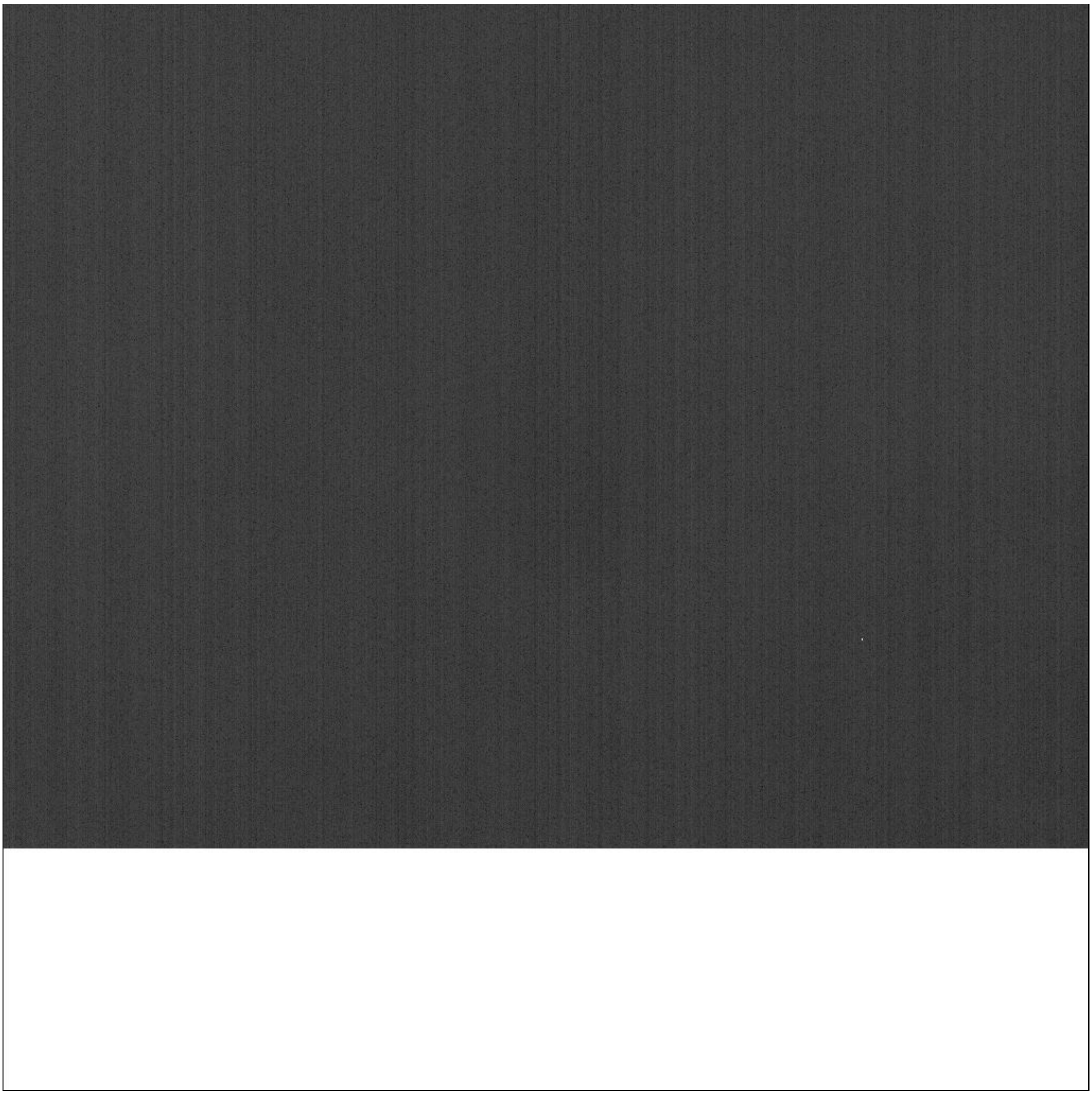

Figure 7-11 : Reference levels acquired under $^{83}Kr^{25+}$ ion beam at 0° with 200 ms integration time in addressing per frame NDR mode - image partially at 4095 LSB

7.4. SET cross section curves

Address registers upset cross sections versus LET are summarized in Figure 7-12 and Figure 7-13.

The curve in Figure 7-12 is taken from HAS2 qualification report which was covering high LET heavy ion cocktail ([RD 2]). This test campaign was performed in DR mode only.

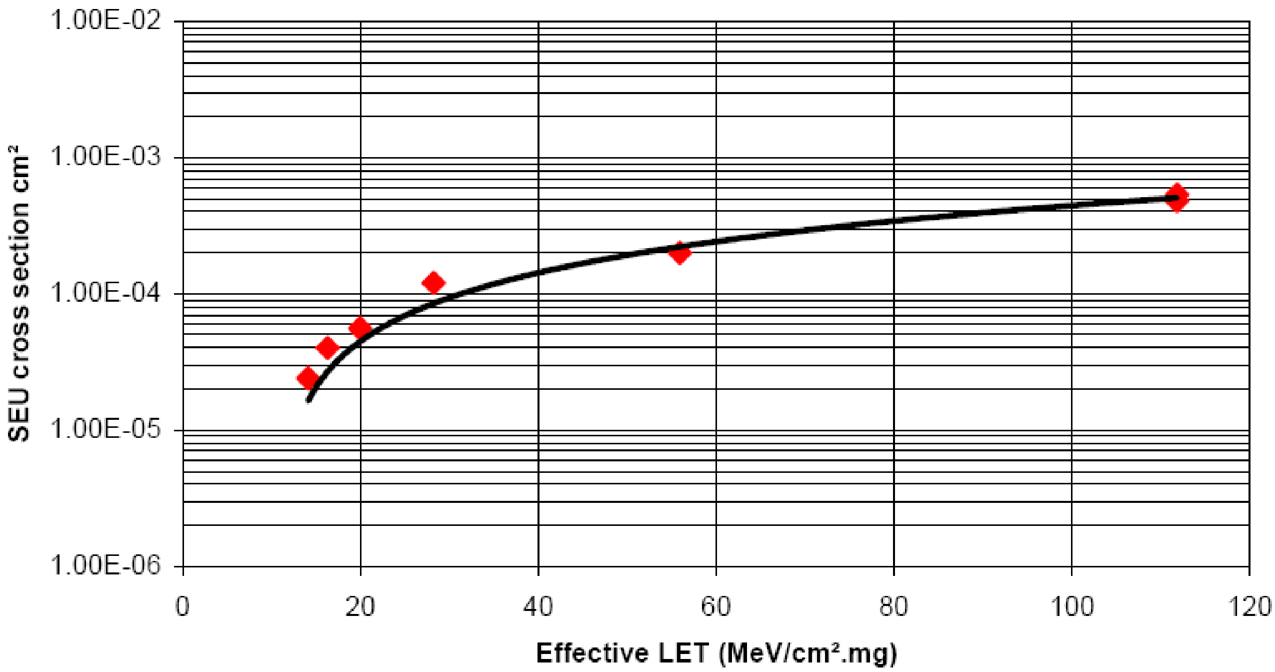

Figure 7-12 : Address registers upset cross section versus effective LET (from [RD 2])

The curve above can be compared to the curve obtained herein with the low LET cocktail (Figure 7-13).

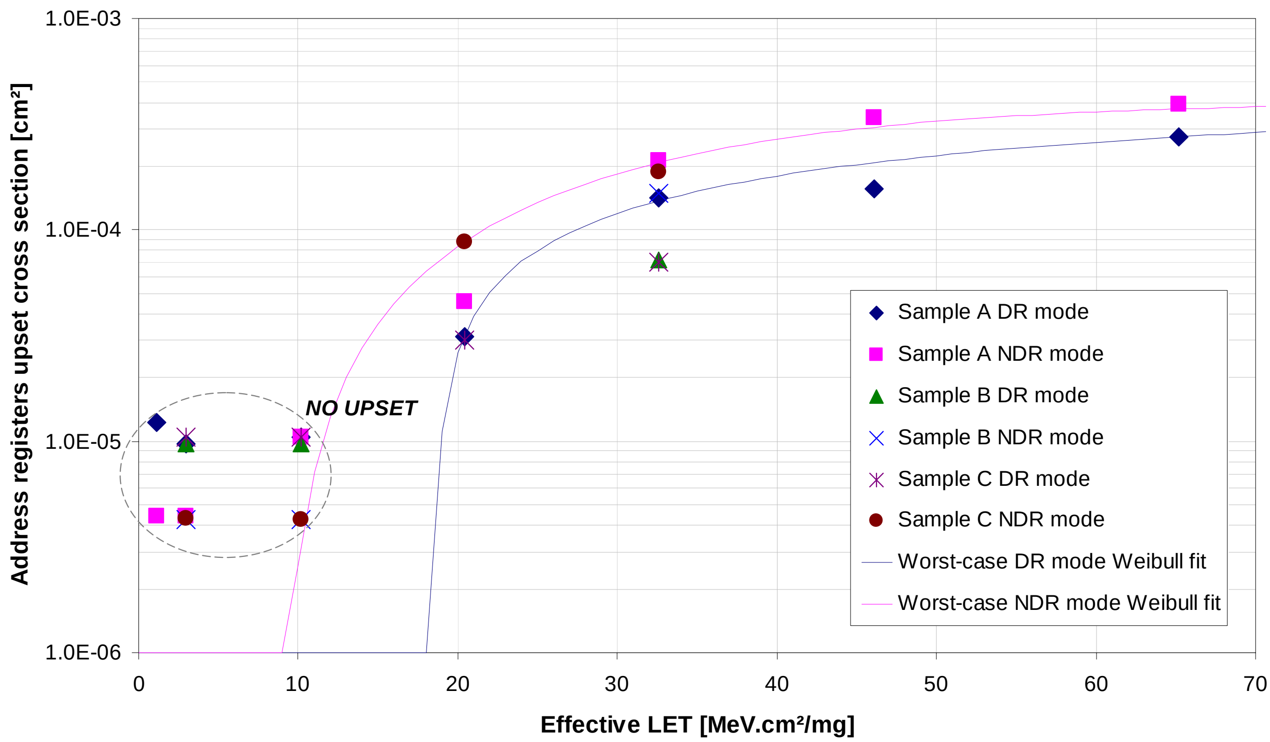

Figure 7-13 : Address registers upset cross section versus heavy ion effective LET

DR mode cross section is quite similar to the previous cross section obtained during the qualification campaign ([RD 2]).

NDR mode is systematically more sensitive than DR mode.

Address registers cross section versus LET can be modelled by a Weibull function with the following parameters (least squares fitting on worst-case values):

$$\sigma = \sigma_{sat} \cdot \left[1 - \exp\left(-\frac{LET - LET_{th}}{W} \right)^{S} \right]$$

Parameter	DR mode	NDR mode
LET_{th}	18.5 MeV.cm²/mg	9 MeV.cm²/mg
σ_{sat}	4.5E-04 cm²	4.0E-04 cm²
W	50 MeV.cm²/mg	29 MeV.cm²/mg
S	0.8	1.5

No difference has been observed between neutron irradiated device and unirradiated devices.

Output multiplexer upset cross section is very low around 2.0E-06 cm² with a LET threshold between 20.4 and 32.6 MeV.cm²/mg

8.CONCLUSIONS

The HAS2 image sensor has been tested under heavy ions at low LET and in both Destructive and Non Destructive Readout mode

No Latch-up and **no SEFI** have been observed up the applied LET of **65.2 MeV.cm²/mg**.

The **address registers** upset cross section is in line with the results obtained during the previous radiation test campaign with a **saturation cross section** of **4.5E-04 cm²** and a **LET threshold** around **9 MeV.cm²/mg** in NDR mode.

Experimental results have confirmed that the HAS2 address registers are not sensitive up to 10.2 MeV.cm²/mg (cross-section lower than 4.3E-06 cm²).

Output **MUX** upset **cross section** is around **2.0E-06 cm²** with a **LET threshold** between **20.4** and **32.6 MeV.cm²/mg**.