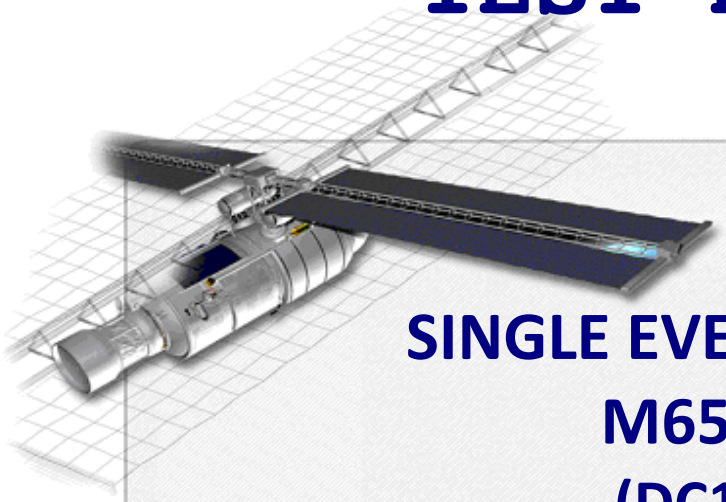
PROTON
TEST REPORT



SINGLE EVENT EFFECTS
M65608E
(DC1203)
Rad. Tolerant 128k x 8, 5-Volt SRAM
From
ATMEL

TRAD/TP/M65608/DC1203/ESA/BV/1312 Rev1		Labège, December 20th 2013
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CONTENTS

1. Introduction 5
2. Documents 5
2.1. Applicable documents 5
2.2. Reference documents 5
3. Organization of Activities 5
4. Parts information 6
4.1. Device description 6
4.2. Identification 6
4.3. Procurement information 6
4.4. Sample Preparation 6
4.5. Sample pictures 7
4.5.1. External view 7
4.5.2. Internal view 7
5. Irradiation Facility 8
5.1. PSI Proton Test Facility (Paul Scherrer Institute - Switzerland) 8
5.2. PIF Main features 8
5.3. Beam characteristics 8
6. Test Procedure and Setup 9
6.1. Test procedure 9
6.1.1. Description of the test method 9
6.2. Test bench description 9
6.2.1. Preparation of test hardware and program 9
6.2.2. Software description 11
6.2.3. Hardware description 12
6.2.4. Test Bench operation 12
6.2.5. Test equipment identification 14
6.2.6. Device setup and Test conditions 15
7. Non conformance 15
8. RESULTS 16
8.1. Summary of runs 16
8.2. SEU tests results 17
8.2.1. SEU Cross sections 17
8.3. MBU tests results 18
8.4. Complementary test result analysis 18
9. Conclusion 19

FIGURES

Figure 1: package marking 7
Figure 2: Internal overall view 7
Figure 3: Die marking 7
Figure 4 : Synoptic view of the test bench 9
Figure 5 : test bench pictures 10
Figure 6 : Test bench software architecture 11
Figure 7 : Test bench software screenshot 11
Figure 8 : Global view of the test bench hardware 12
Figure 9 : Test bench operation 13
Figure 10 : Three-dimensional image of the memory tested 14
Figure 11: SEU cross section curve for M65608E 17

TABLES

Table 1: Organization of activities 5
Table 2: M65608E Test Conditions 15
Table 3: M65608E test results 16
Table 4: SEU cross section results 17
Table 5: SEU & MBU distribution – according to number of bits upseted 18
Table 6: Error types distribution 18
Table 7: Transition ‘0’ to ‘1’ and ‘1’ to ‘0’ distribution 19
Table 8: Upsets per bit distribution 19

1. Introduction

This report includes the test results of the proton Single Event Effects (SEEs) test sequence carried out on the **M65608E**, a **Rad. Tolerant 128k x 8 bit CMOS SRAM** from **ATMEL**.

This test was performed for the **European Space Agency** on the **M65608E** susceptible to show Single Event Upset (**SEU**) and Multiple Bit Upset (**MBU**) induced by protons.

2. Documents

2.1. Applicable documents

SoW TEC-QEC/CP/SOW/2013-9

2.2. Reference documents

Basic specification: ESCC No. 25100 Issue 1, October 2002.
Data Sheet: M65608E, Rad. Tolerant 128Kx8, 5-Volt, Very Low Power, CMOS SRAM, Rev. 4151P–AERO–11/12

3. Organization of Activities

The relevant company has performed the following tasks during this evaluation:

1	Procurement of Test Samples	ESA
2	Preparation of Test Samples (delidding)	TRAD
3	Preparation of Test Hardware and Test Program	TRAD
4	Samples Check out	TRAD
5	Accelerator Test	TRAD/ESA
6	Proton Test Report	TRAD

Table 1: Organization of activities

4. Parts information

4.1. Device description

The M65608E is a very low power CMOS static RAM organized as 131072 x 8 bits. Utilizing an array of six transistors (6T) memory cells, the M65608E combines an extremely low standby supply current (Typical value = 0.2 µA) with a fast access time at 30 ns over the full military temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise. The M65608E is processed according to the methods of the latest revision of the MIL PRF 38535 or ESCC 9000.

4.2. Identification

Type:	M65608E
Manufacturer:	ATMEL
Function:	Rad. Tolerant 128k x 8 bit CMOS SRAM

4.3. Procurement information

Packaging:	FP32
Date Code:	1203
FR No.:	58096-2
Sample size:	10 parts provided by ESA.

4.4. Sample Preparation

Two parts were delidded by TRAD. A functional test sequence was performed on delidded samples to check that devices were not degraded by the delidding operation. This process showed that no sample was damaged during the delidding operation.

4.5. Sample pictures

4.5.1. External view

Figure 1: package marking

4.5.2. Internal view

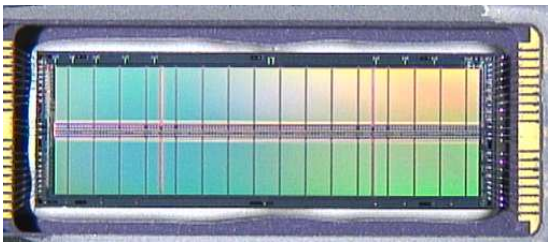


Figure 2: Internal overall view

Figure 3: Die marking

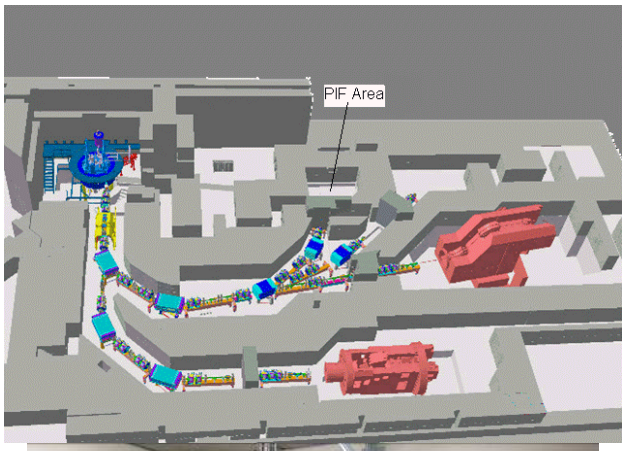
5. Irradiation Facility

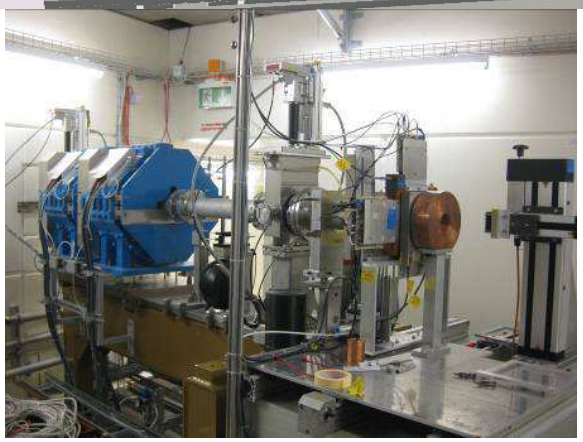
The test was performed at PSI (Paul Scherrer Institute) on December 1st, 2013. Four samples were irradiated.

5.1. PSI Proton Test Facility (Paul Scherrer Institute - Switzerland)

PIF (Proton Irradiation Facility).

The initial proton beam for PIF is delivered from the PROSCAN accelerator with the help of the primary energy degrader, which allows setting the initial beam energy from 230 MeV down to 74 MeV.
The beam is subsequently guided to the Experimental Area where PIF facility is located.
The PIF experimental set-up consists of the local PIF energy degrader, beam collimating and monitoring devices.
According to the experience and user requirements, the monitor detectors are selected for each experiment individually: ionization chambers, Si-detectors, plastic scintillators.
Beam flux values are monitored through a set of counters and a PC-based data acquisition system. The system monitors proton flux and dose rate, calculates the total deposited dose and controls beam focus parameters. It also allows for setting the beam energy with the help of the PIF local energy degrader. Irradiations are usually carried out in air.





5.2. PIF Main features

- Initial proton energies: 230, 200, 150, 100 and 74 MeV.
- Energies available using the PIF degrader: quasi continuously from 6 MeV up to 230 MeV
- Maximum flux at 230 MeV for the focused beam: ~ $2*10^9$ protons/sec/cm^2
- Beam profiles are of Gaussian-form with standard (typical) : FWHM=10 cm
- Irradiations take place in air
- The maximum diameter of the irradiated area: 9 cm
- The accuracy of the flux/dose determination: 5%
- Neutron background: less than 10^{-4} neutrons/proton/cm^2
- Irradiations, devices and sample positioning are supervised by the computer
- Data acquisition system allows automatic runs with user pre-defined irradiation criteria

5.3. Beam characteristics

The beam flux was set between 2.06E+07 and 3.52E+07 protons/cm²/s based on the device sensitivity. Proton energies used were 230MeV, 200MeV, 151MeV, 101MeV, 75MeV, 39MeV and 23MeV. The initial energy was 230 MeV, the rest of energies were obtained with the use of degraders.

6. Test Procedure and Setup

6.1. Test procedure

6.1.1. Description of the test method

Runs were performed up to a fluence of 1.0E+10 Protons/cm^2.

During the irradiation, the M65608E was continuously read for error detection. Write cycles were only applied in case of SEU or MBU identification in order to verify the ability of the memory to be written back to its initial state after an upset (test conditions summarized in table 2).

This test method was applied to verify the SEU and MBU sensitivity of the device.

The test was terminated when the maximum fluence was reached or when enough events (several thousands) were recorded that are statistically representative of the part behaviour.

6.2. Test bench description

6.2.1. Preparation of test hardware and program

The test bench consists of a Labview-based software, laboratory equipment, and electronic board as part of the hardware. It allows the testing of parts under high energy beam by giving the possibility to separate test boards from the irradiated board charged with Units Under Test (UUT). A remote communication between the irradiated board and the other test boards protects all electronic parts constituting the latter from the irradiation of the high energy beam.

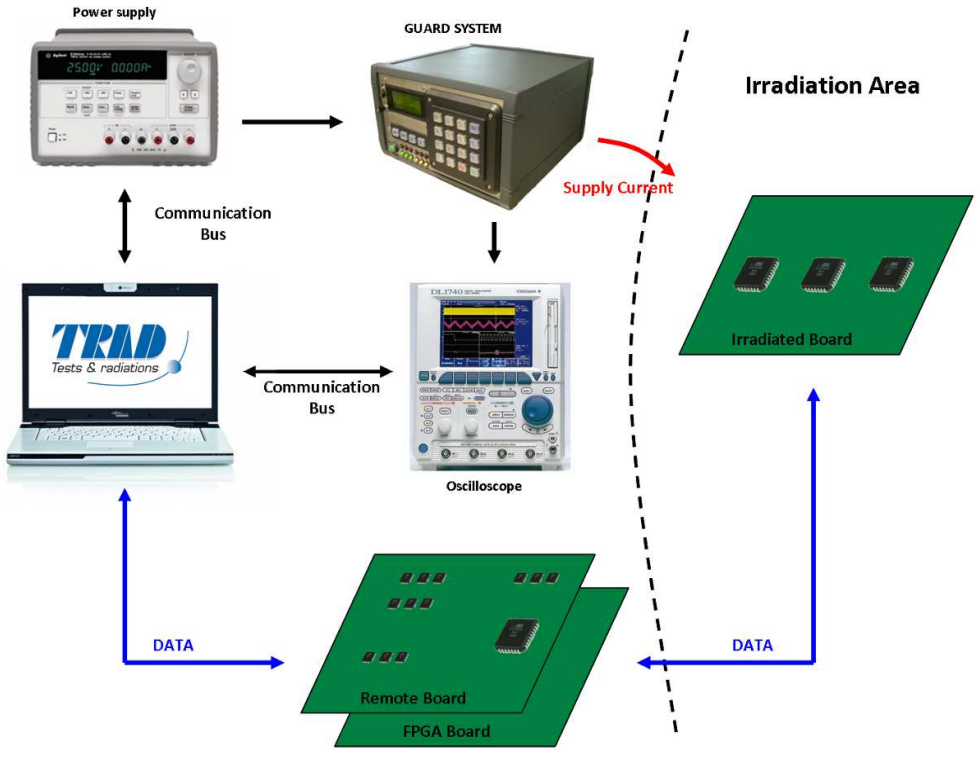


Figure 4 : Synoptic view of the test bench

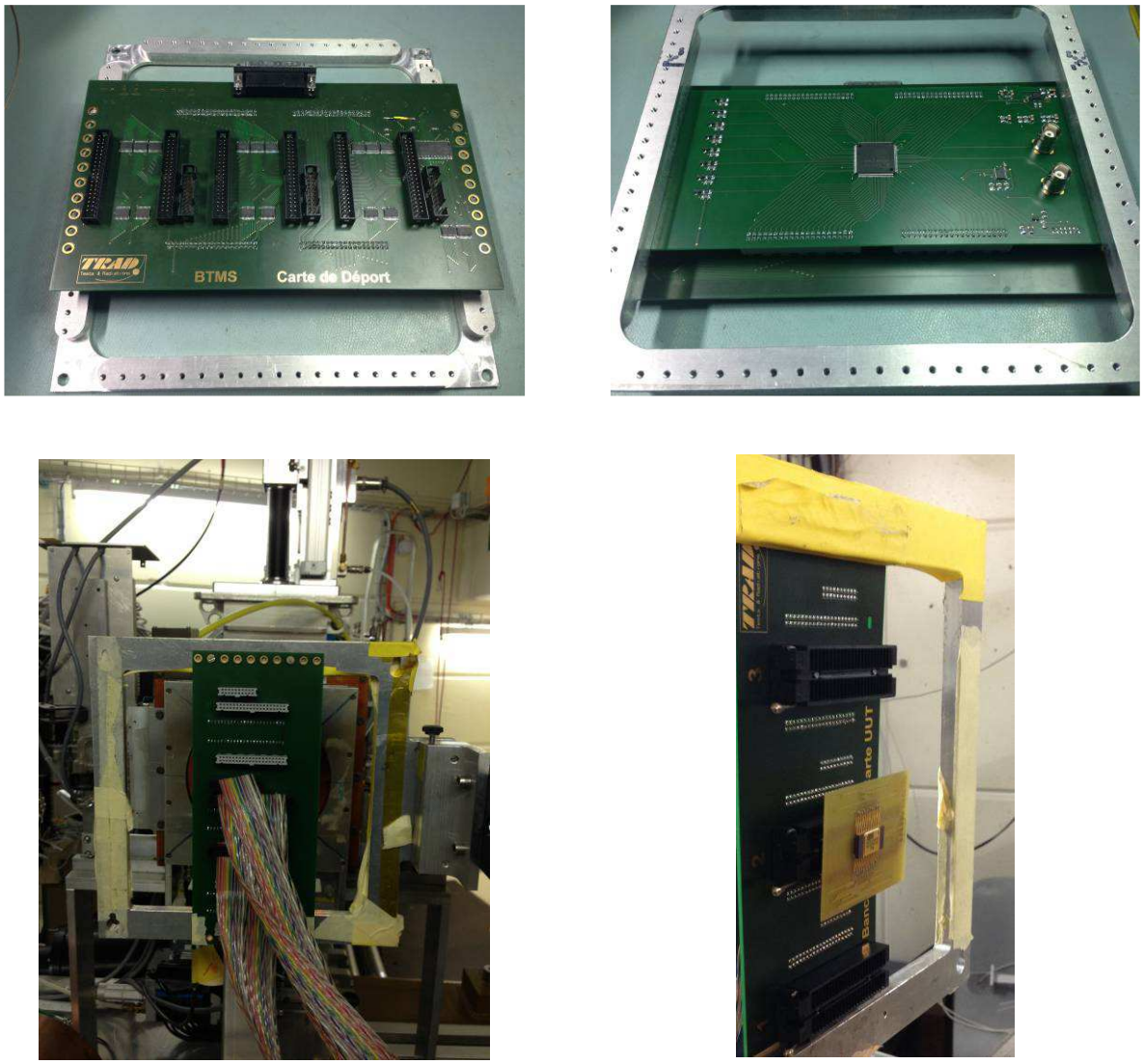


Figure 5 : test bench pictures

6.2.2. Software description

The software is designed as a user interface that drives the hardware and manages all the data flow for storage and visualization in real-time during the experiment. It also ensures the communication with laboratory equipment, then gathering all the necessary functions for the operator to drive the experiment from a single interface.

Considering a software-module based approach, the following figure describes the test bench software:

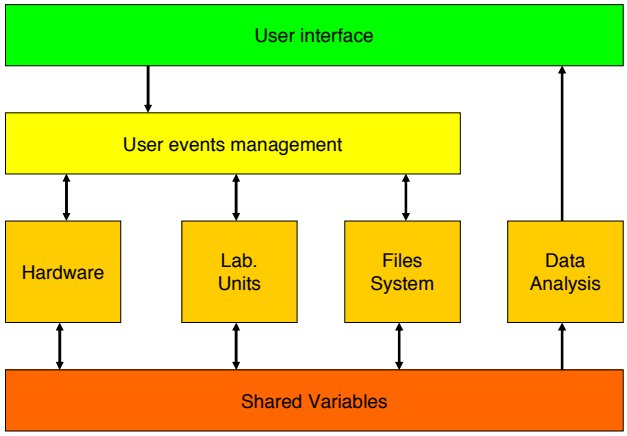


Figure 6 : Test bench software architecture

Each functional block of the software has been designed to run independently, sharing common variables, and all of them are driven by the “User events management” block. This architecture provides good stability by using a small amount of CPU charge and keeping the physical memory available at all times, to avoid a system crash during an experiment.

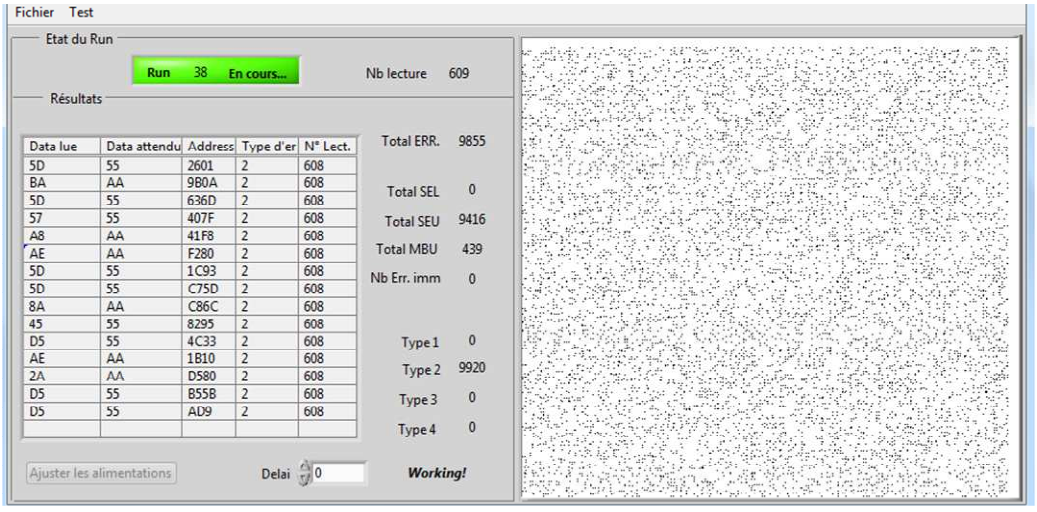


Figure 7 : Test bench software screenshot

6.2.3. Hardware description

The hardware is designed around an FPGA to provide an efficient way to manage the required design flexibility combined with a robust architecture. Then, by reconfiguration of the memory controller, the test bench can address any SRAM for testing purposes up to 1.048.576 * 16 bits-words (20 address bits).

The power supply delivers the current for the UUT through the GUARD System, a specific unit designed by TRAD that monitors the supply current and protects the UUT against latchups. Each event detected by the GUARD system triggers the oscilloscope for latchup visualization.

Figure 8 is a global view of the Test Bench with its three boards represented.

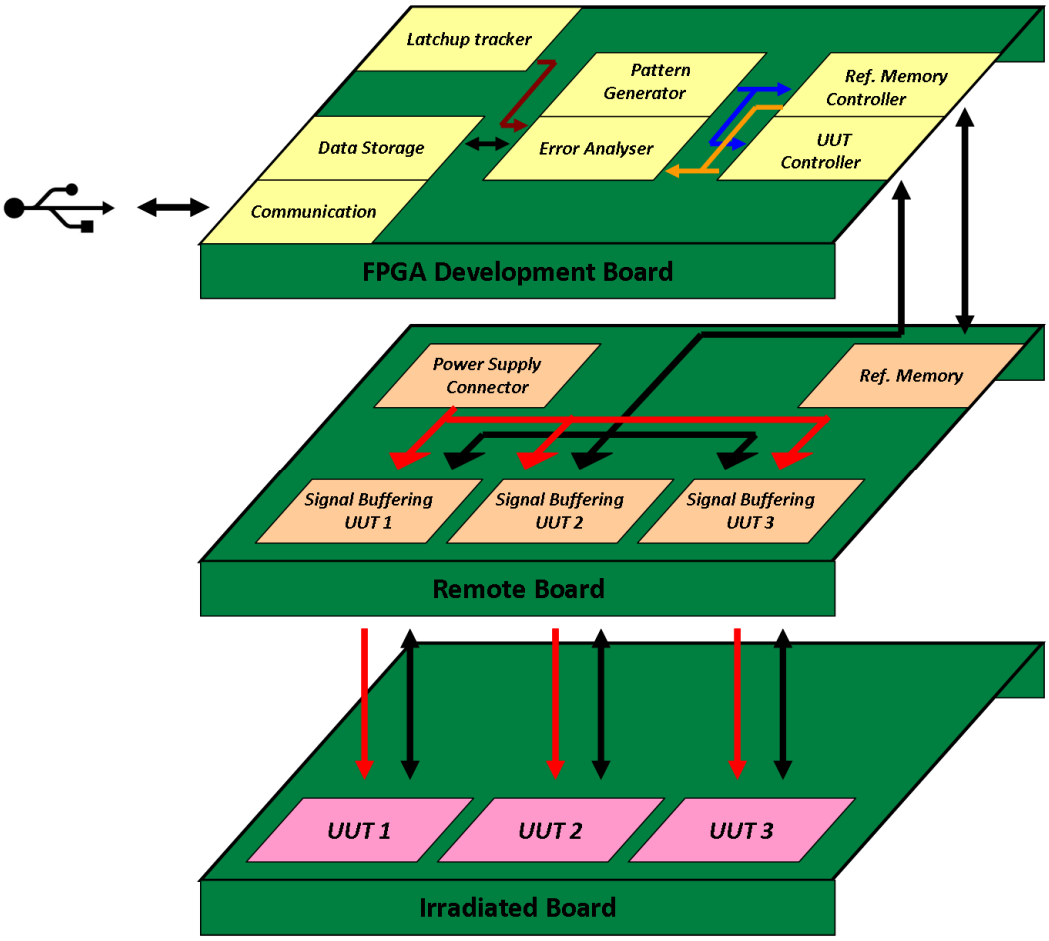


Figure 8 : Global view of the test bench hardware

6.2.4. Test Bench operation

Before each run, the reference memory and the UUT are filled with a checker-board pattern (e.g 10101010 at even addresses and 01010101 at odd addresses) from address 0 up to the maximum address of the UUT. A first verification of their contents is performed off beam.

During irradiation, the test bench reads both memories and compares their contents one address at a time. When the last address is reached, the FPGA sends a command to the Labview software to indicate

the end of the read/compare cycle. Depending on the user setting options, a new read/compare order is immediately sent back to the FPGA or an additional delay can be inserted before. If there is no event during the cycle, this operation is performed at the maximum system speed (test conditions summarized in table 2).

However, if the data read from the UUT doesn't fit the data from the reference memory, a sequence of operation is launched to determine the error type. This sequence is summarized in Figure 9.

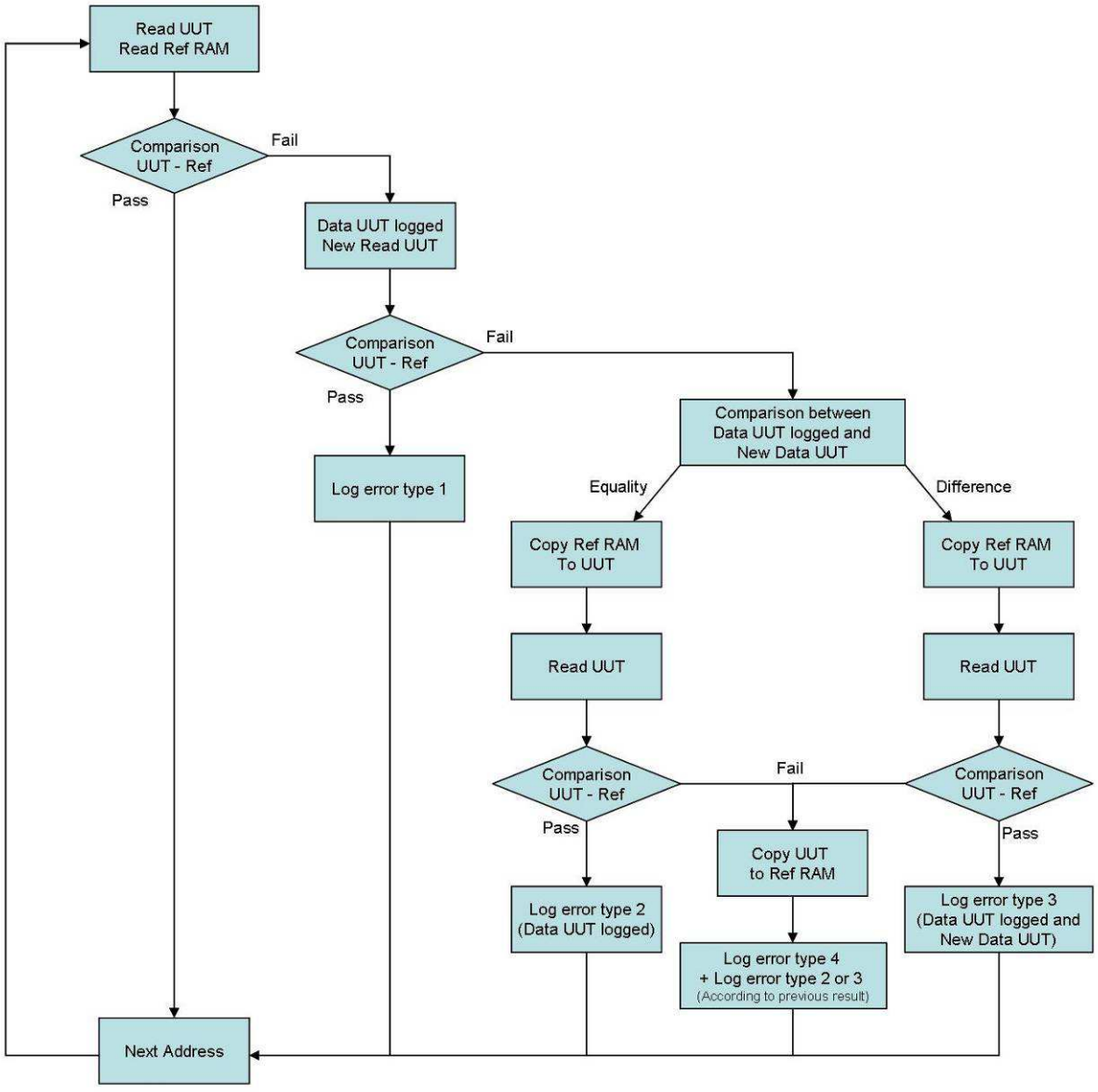


Figure 9 : Test bench operation

An error logged as "Type 1" is considered to be an SET (Single Event Transient) present on the output bus when it has been sampled. If the data from the UUT is correct after a second read cycle delayed by 1µs, it means that the storage element itself contains the expected value.
In the case of an upset in a storage element, the data from the UUT won't match the expected data (from the reference memory) after a second read cycle. This eliminates the possibility of a transient event. If the two read cycles give the same erroneous data, the error is logged as "Type 2". In case of a

difference between these two data, the error is logged as “Type 3”. In order to determine if the event is actually an SEU or a stuck bit, a write cycle is performed with the expected data, followed by a read cycle. The result of this third comparison determines the final error type. Either the data is correct again and an SEU is recorded (Type 2 or 3) or the memory cell can’t be written back to its initialization state and therefore the event is a stuck bit (Type 4).

All the events detected by the error analyser are sent to the Labview software through the communication module for real-time analysis and storage. Thus, an illustration of the memory area can be calculated and plotted in a three-dimensional image in which the first plane is representative of the memory area in address term and the third dimension gives the upset occurrence per address. This graphical view allows to verify the beam uniformity and to make sure that all the memory area is tested.

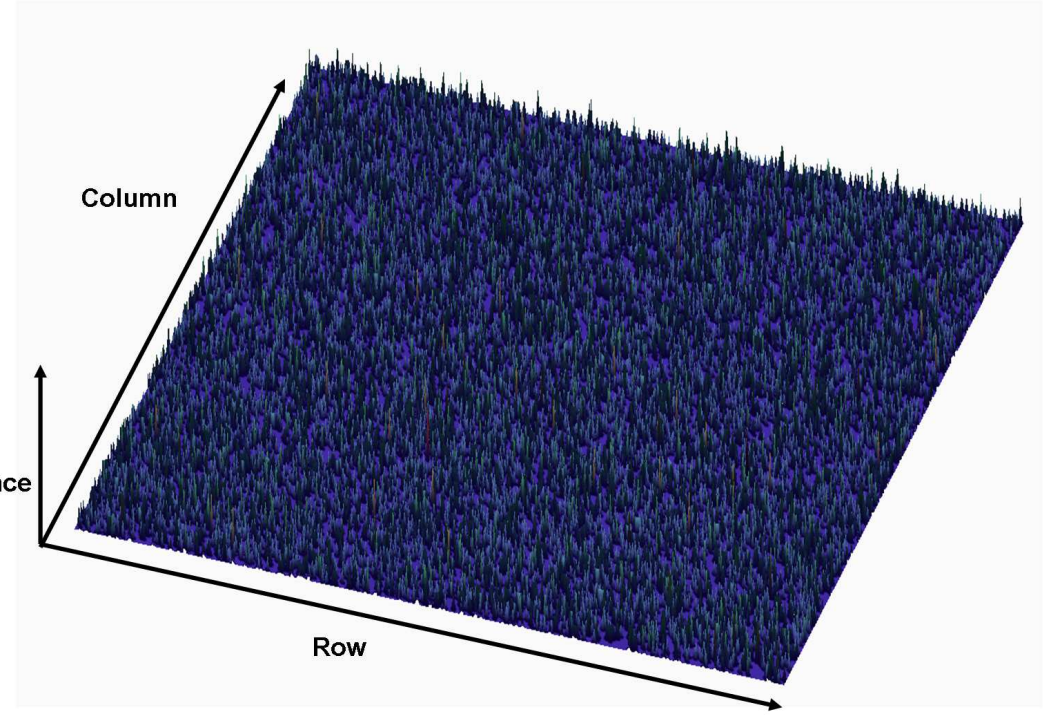


Figure 10 : Three-dimensional image of the memory tested.

6.2.5. Test equipment identification

The tests were carried out with the following list of equipment.

COMPUTER	MI-OP-40
REF. TEST BOARD	AGIS II - BTMS carte de déport - BTMS Carte UUT
EQUIPMENT	ME54 – GR51
TEST PROGRAM	BTMS_BV_1311_rev3.vi

6.2.6. Device setup and Test conditions

The device setup used to perform the proton SEE test is given in the following table:

Vcc	5.0V
Number of Address tested	131 072
Data mask	8 bits width data tested (no mask)
Delay between full device read cycles (note 1)	0s
Delay after 1st error detection (note 2)	1µs
Read Cycle time of the full memory (note 3)	0.328s (without error)
Pattern used	Checker board (xAA/x55)
Temperature	25°C (Room temperature)

Table 2: M65608E Test Conditions

Note 1 : When the last address is reached, an exposure delay can be inserted before initiating a new comparison cycle.
Note 2 : During a comparison cycle, if the data read from the UUT is wrong, a short delay is inserted before initiating a second read cycle (same address) to eliminate the possibility of a transient on the IO of the UUT during sampling.
Note 3 : If no error occurs on the memory, each address is read and compared with its previous value every 250ns. If errors occur on the memory, each address is read and compared with its previous value on average every 2µs (this value can be more important if the storage system is full).

7. Non conformance

Test sequence, test and measurement conditions were nominal.

8. RESULTS

8.1. Summary of runs

Runs performed during this campaign are shown hereafter.

M65608E VCC = 5.0V								SEU		MBU		Comments
RUN	Part	Energie (Mev)	Flux (p/cm2/s)	Time (s)	Fluence	Run Dose (krad)	Cumulated Dose (krad)	Events	Cross section	Events	Cross section	
11	88	230	2.57E+07	389	1.00E+10	0.535	0.535	149	1.49E-08	0	<1.00E-10	wrong settings
12	88	230	2.06E+07	485	1.00E+10	0.535	1.07	540	5.40E-08	0	<1.00E-10	
13	88	200	2.75E+07	364	1.00E+10	0.583	1.653	473	4.73E-08	0	<1.00E-10	
14	88	151	3.40E+07	294	1.00E+10	0.703	2.356	478	4.78E-08	0	<1.00E-10	
15	88	101	2.96E+07	338	1.00E+10	0.936	3.292	447	4.47E-08	0	<1.00E-10	
16	88	75	3.30E+07	303	1.00E+10	1.16	4.452	439	4.39E-08	0	<1.00E-10	
17	89	230	3.39E+07	295	1.00E+10	0.534	0.534	526	5.26E-08	0	<1.00E-10	
18	89	200	2.98E+07	336	1.00E+10	0.583	1.117	476	4.76E-08	0	<1.00E-10	
19	89	151	3.52E+07	284	1.00E+10	0.705	1.822	477	4.77E-08	0	<1.00E-10	
20	89	101	2.96E+07	338	1.00E+10	0.936	2.758	442	4.42E-08	0	<1.00E-10	
21	89	75	3.29E+07	304	1.00E+10	1.16	3.918	416	4.16E-08	0	<1.00E-10	
27	79	39	3.19E+07	313	1.00E+10	1.92	1.92	256	2.56E-08	0	<1.00E-10	
28	79	23	2.15E+07	465	1.00E+10	2.9	4.82	156	1.56E-08	0	<1.00E-10	
29	78	39	3.22E+07	311	1.00E+10	1.92	1.92	209	2.09E-08	0	<1.00E-10	
30	78	23	2.16E+07	463	1.00E+10	2.9	4.82	123	1.23E-08	0	<1.00E-10	

Table 3: M65608E test results

SEU events were detected during this test.
SEU test results are described hereafter.
From the 27th run, parts irradiated were delidded (part 78 & 79)

8.2. SEU tests results

The SEU test was performed at 25°C (Room temperature).

SEUs were observed down to the lowest test energy of 23 MeV.

8.2.1. SEU Cross sections

M65608E - SEU Cross Section (cm²)				
Energy (MeV)	88	89	79	78
230	5.40E-08	5.26E-08		
200	4.73E-08	4.76E-08		
151	4.78E-08	4.77E-08		
101	4.47E-08	4.42E-08		
75	4.39E-08	4.16E-08		
39			2.56E-08	2.09E-08
23			1.56E-08	1.23E-08

Table 4: SEU cross section results

The following figures present the cross section of the SEU event on the **M65608E** part.

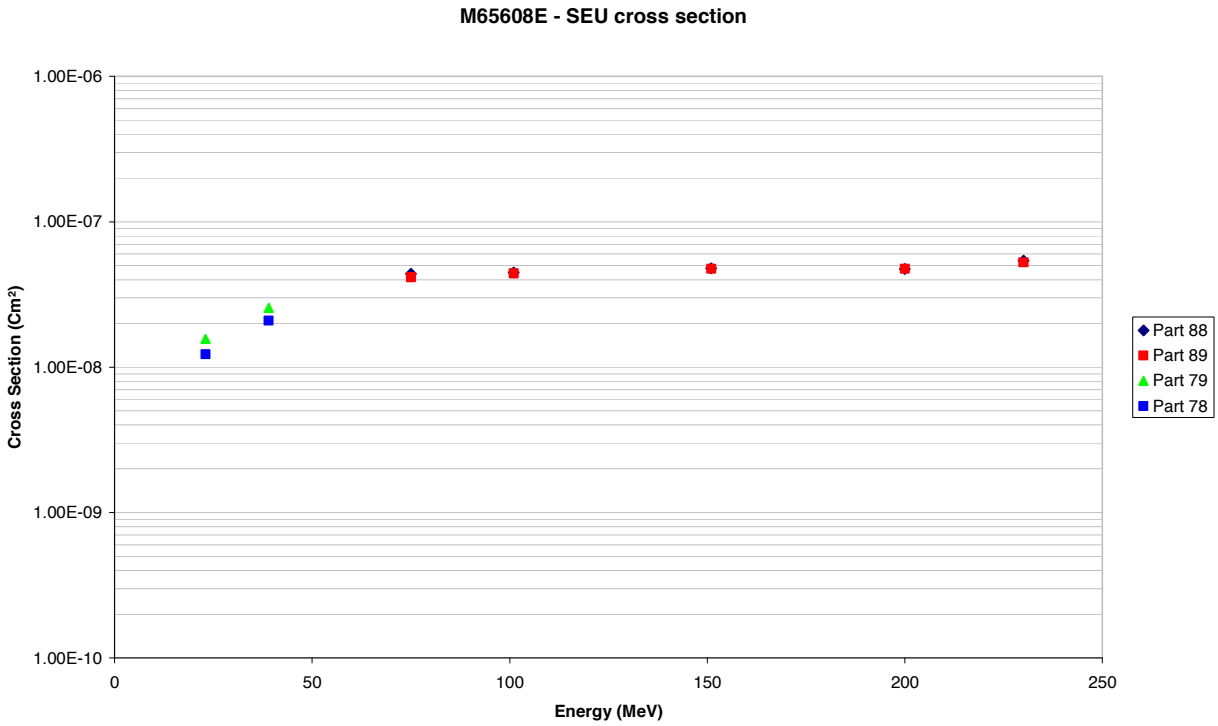


Figure 11: SEU cross section curve for M65608E

8.3. MBU tests results

The MBU test was performed at 25°C (Room temperature).

No MBUs were observed during the irradiation over the full energy range from 23 MeV to 230 MeV.

8.4. Complementary test result analysis

	SEU	MBU-2	MBU-3	MBU-4	MBU-5	MBU-6	MBU-7	MBU-8	Total events
Run N° 0012	540	0	0	0	0	0	0	0	540
Run N° 0013	473	0	0	0	0	0	0	0	473
Run N° 0014	478	0	0	0	0	0	0	0	478
Run N° 0015	447	0	0	0	0	0	0	0	447
Run N° 0016	439	0	0	0	0	0	0	0	439
Run N° 0017	526	0	0	0	0	0	0	0	526
Run N° 0018	476	0	0	0	0	0	0	0	476
Run N° 0019	477	0	0	0	0	0	0	0	477
Run N° 0020	442	0	0	0	0	0	0	0	442
Run N° 0021	416	0	0	0	0	0	0	0	416
Run N° 0027	256	0	0	0	0	0	0	0	256
Run N° 0028	156	0	0	0	0	0	0	0	156
Run N° 0029	209	0	0	0	0	0	0	0	209
Run N° 0030	123	0	0	0	0	0	0	0	123

Table 5: SEU & MBU distribution – according to number of bits upseted

	Err. Type 1	Err. Type 2	Err. Type 3	Err. Type 4	Total events
Run N° 0012	0	540	0	0	540
Run N° 0013	0	473	0	0	473
Run N° 0014	0	478	0	0	478
Run N° 0015	0	447	0	0	447
Run N° 0016	0	439	0	0	439
Run N° 0017	0	526	0	0	526
Run N° 0018	0	476	0	0	476
Run N° 0019	0	477	0	0	477
Run N° 0020	0	442	0	0	442
Run N° 0021	0	416	0	0	416
Run N° 0027	0	256	0	0	256
Run N° 0028	0	156	0	0	156
Run N° 0029	0	209	0	0	209
Run N° 0030	0	123	0	0	123

Table 6: Error types distribution

	0 ---> 1	1 --->0	Total events*
Run N° 0012	274	266	540
Run N° 0013	238	235	473
Run N° 0014	248	230	478
Run N° 0015	231	216	447
Run N° 0016	233	206	439
Run N° 0017	273	253	526
Run N° 0018	246	230	476
Run N° 0019	242	235	477
Run N° 0020	211	231	442
Run N° 0021	221	195	416
Run N° 0027	124	132	256
Run N° 0028	79	77	156
Run N° 0029	111	98	209
Run N° 0030	59	64	123

Table 7: Transition '0' to '1' and '1' to '0' distribution

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Total events*
Run N° 0012	69	76	59	70	66	80	65	55	540
Run N° 0013	60	77	53	54	54	61	59	55	473
Run N° 0014	82	54	41	50	65	56	61	69	478
Run N° 0015	64	58	53	48	49	57	62	56	447
Run N° 0016	56	54	48	57	51	63	53	57	439
Run N° 0017	69	65	64	66	61	56	68	77	526
Run N° 0018	53	67	58	49	67	63	61	58	476
Run N° 0019	62	54	65	69	53	57	59	58	477
Run N° 0020	46	58	47	56	63	55	59	58	442
Run N° 0021	48	51	63	54	67	54	49	30	416
Run N° 0027	27	26	35	36	29	39	35	29	256
Run N° 0028	18	17	21	20	19	23	19	19	156
Run N° 0029	25	32	32	20	21	26	26	27	209
Run N° 0030	17	19	18	13	11	16	12	17	123

Table 8: Upsets per bit distribution

*: On tables 7 and 8, the column Total events corresponds to the number of SEU and MBU detected during the run and not to the sum of all upsets detected. As an MBU is composed of 2 upsets minimum, those two totals are different.

9. Conclusion

Proton SEE tests were performed on **M65608E**, a **Rad. Tolerant 128k x 8 bit CMOS SRAM** from **ATMEL**. The aim of the test was to evaluate the sensitivity of the device versus **SEU** and **MBU**.

SEUs were observed down to the lowest test Energy of 23 MeV.

No **MBUs** were observed on the M65608E.