ATC18RHA

Rad-Hard 0.18µm CMOS cell-based ASIC family

for space use

Summary Report

V1.0 – 31/03/2005

Reference: ADF-DE-R0564-CUP

TABLE OF CONTENT

1. Introduction....3
2. Contractual context....3
3. Summary of the technical actions....3
   3.1. Library development....3
   3.2. characterization on test vehicle and radiation testing....4
      3.2.1. test vehicle specification....4
      3.2.2. Test vehicle characterization and correlation....5
      3.2.3. Radiation testing....5
      3.2.4. Design kits....6
4. Main results....6
   4.1. Characterization....6
   4.2. Correlation....6
   4.3. Radiation....6
   4.4. Conclusion....7
5. Proposed following activities....7
6. Technical data package....7
7. Commercial evaluation....9

1. Introduction

The purpose of this document is to present a summary of the works performed during the development of the ASIC ATC18RHA libraries from the specification to the release of the design kit. It also contains a commercial evaluation summarizing the expected utilization level of the technology.

2. Contractual context

Two contracts have been placed by the Space Agencies:
- on 8/11/2001: the CNES contract n°721/00/CNES/8286/00 – Lot 2 covering the development of memories libraries.
- on 14/02/2002: the ESA contract n° 15677/01/NL/FM covering the development of radiation hardened cell libraries.

It was initially planned to develop this ASIC family using the radiation hardened 0.25µm process. In 2002, the commercial 0.18µm process, so called AT58K, has been successfully evaluated under irradiation. In December 2002, ATMEL decides with the Agencies agreement to migrate from the 0.25µm to the 0.18µm process.

The completion date for both contracts, ESA and CNES, has been fixed at the end of March 2005.

3. Summary of the technical actions

The ATC18RHA project is split in 2 phases:
- the development of the libraries
- their characterization on test vehicle and the radiation testing.

For each phase, a design kit is issued, either before or at the completion of the works.

3.1. Library development

The library development consisted in 3 steps:
- The specification
- The library development itself
- The electrical characterization at simulation level over the military temperature range and applicable supply voltage range

This activity has been completed in March 2004.

A first selection of cells and buffers has been made among the existing commercial CMOS 0.18µm ATC18 libraries. The choice was based on the experience and statistics on the former families. A list of additional cells has also been built. The whole has been submitted to our major customers. Their feedback was positive and the final library content has been accordingly fixed.

As mentioned above, the commercial 0.18µm process (AT58K) has been evaluated under radiation. The conclusion was that it was not necessary to harden the technology provided a

hardening at design level was made. This hardening by design consisted in the re-layout of the 3.3V buffers. This has been the first step of the library design activity.

In order to be in line with the already qualified space assembly, all the existing buffers have been redesign with a pitch of 95µm. One of the ATC18RHA important feature was to provide as much cold sparing cells as possible. For this reason, all the pads have been re-designed.
Finally, the space specific cells (HDFF), the LVDS buffers and the PLL have been designed.

Once all the library element are designed, it is necessary to characterize them at simulation level. It consists in simulating the static and dynamic parameters. This also applies to the memories (characterization over the full military temperature range of the Virage compiler and Genesys synthesizer).

This task was completed when a major change occurred at process level, leading to new technology models. A new characterization has been done and the results have been included in the databooks of the Beta design kit.

3.2. characterization on test vehicle and radiation testing

3.2.1. test vehicle specification

In order to characterize the libraries at test level, it has been necessary first to specify and design the test vehicle.
It was not possible to use an existing ATC18 test vehicle since major changes had been done (3.3V transistors re-layout, new cells…). Therefore a test vehicle had been specified. It was mandatory for this test vehicle to be usable for the following purpose:

- to test the functionality and the performances of the ATC18RHA library main elements
- to calibrate the ATC18RHA libraries
- to test the ATC18RHA radiation performances (total dose and SEE)
- to be used as a Standard Evaluation Circuit (SEC)

It was in fact impossible to answer all those requests with only one die. It has therefore been decided to split the requirements into 2 groups and specify 2 test chips. There are respectively called V34 and V35.
The V34 test vehicle is dedicated to:

- radiation testing (TID, SEU and SEL)
- qualification (used as a SEC)
- memory performances characterization

The V35 test vehicle is dedicated to:

- IO33 and IO18 buffers characterization
- PLL and LVDS characterization
- calibration of cells and buffers libraries

Both circuits are designed on the same predefined die size, the ATC18RHA95_324 (~77mm²). They can be bonded in 3 different packages: MQFPF256, MQFPT352 and MCGA472. Only the MQFP packages have finally been used. The MQFPF256 for most of the characterization steps, and the MQFPT352 for the high speed tests. This is explained by the fact that there is no test socket available to date for the MQFPF256 which can bear above 100MHz.

Once specified, the circuits have been designed. This experience has been used to update the design manual and enrich it of recommendations for the future users of the ATC18RHA libraries.

This work has been completed in March 2004.

3.2.2. Test vehicle characterization and correlation

Samples of each of the test vehicles have been manufactured in August 2004, using the AT58K process. These samples have been used to perform the characterization and the radiation tests (TID and SEE). The results have been analyzed and correlated with the simulations. These tasks have been completed in March 2005.

The Characterization consisted in measuring the following parameters.
Static:

- Static consumption
- Input and Output voltage / currents on IO18 and IO33 buffers
- Pull-up/pull-down resistances on IO18 and IO33 buffers
- LVDS Buffers (receiver and transmitter)

Dynamic:

- Memory Access timings
- Ring oscillators.
- Propagation time on IO18 and IO33 buffers.
- LVDS Buffers timings.
- PLL frequency

The correlation consisted in comparing the test results obtained on silicon to the simulation results. Each discrepancy has been analyzed and explained. The final datasheet has been updated accordingly.

Some parts (V35) have also been used to determine the ESD class and check the static latch-up immunity.

3.2.3. Radiation testing

As the V34 has been specified for that, it has been used to perform the tests. 3 parts have been characterized under irradiation (SEL, SEU and TID).
The TID campaign has been done from September till November 2004. The SEL campaign has been done at the end of December 2004. It has been necessary to run 3 SEU campaigns (2 in

UCL, 1 in BNL), between December 2004 and March 2005, to complete the test of the memories and of the PLL.

3.2.4. Design kits

4 design kit releases have been issued:

- Alpha (simulation results at mil temp of the selected ATC18 libraries)	October 2003
- Beta (ATC18RHA libraries, no correlation with silicon)	March 2004
- Pre-production (updated design manual and additional power data)	December 2004
- Production (databook correlated with silicon)	March 2005

4. Main results

4.1. Characterization

All the expected results have been reached except for the PLL and LVDS RX buffers dynamic parameters. However, this does not compromise the content of the libraries which still answers to the current demand market.

The LVDS RX final datasheet is therefore:
F <= 400Mbits/s
200mV < VID < 600mV
400mV < VCM < 2V
Eye Width > 80% of Bit period

The PLL is proposed as a specific block in a reduced frequency range (first 2 VCOs: up to 160MHz)

The datasheet has been updated accordingly.

In terms of ESD and static latch-up:

- No latch-up phenomenon has been observed.
- The ATC18RHA is Class 1 with a critical path failure at 500V. This confirms the results obtained by Atmel on the AT58K process. Some improvements are under evaluation and will be implemented for the ATC18RHA when validated.

4.2. Correlation

The differences between the former design kits (before correlation) and the production design kit (after correlation) are the following:

- a factor of 7% has been applied on all capacitor components of extracted RC lines
- a factor of 5% has been applied on the memory timings

4.3. Radiation

The Total Ionizing Dose has been successfully tested up to 300Krads.

The Single Event Latch-up is better than 70MeV.
The Single Event Upset Threshold is better than 25MeV for all the hardened flip flops.
It is around 3MeV for the standard ones. The efficiency of the use of EDAC with the compiled memories and the hardened flip flops for the synthesized memories have been demonstrated.

4.4. Conclusion

Atmel has successfully developed a new standard cell ASIC family, the ATC18RHA with the following features:
- using the AT58KRHA CMOS 0.18µm process.
- Library content : set of standard and SEU hardened cells (25MeV), 3.3V and 1.8V IOs, High speed buffers (LVDS RX and TX) and a PLL
- 3.3V power supply for the periphery, 1.8V for the core
- Memory libraries: compiled (can be associated with the EDAC VHDL library) or synthesized (can use the hardened flip flops)
- Integration up to 5.5Mgates (typical)
- MQFP and MCGA packages up to 472 pins
- Total Ionizing Dose tested up to 300 krads
- Single Event Latch-up better than 70 MeV.cm²/mg

5. Proposed following activities

The gap between the 0.35µm and the 0.18µm regarding the reticule and silicon costs has already led Atmel in proposing with ESA support a Space Multi Project Wafer service.

This gap is also observed regarding the design tools and methodology. For this reason Atmel intends to set up a Design tools service with ESA support.
Another project regarding the HiRel pre-industrialization of this ATC18RHA family is proposed to be performed with ESA support.
Atmel is qualified for an assembly with a single pad ring configuration for MQFP up to 352 pins and MCGA up to 472 pins. The telecom market is requesting more than that. Atmel already took the opportunity to demonstrate that a double staggered pad rings configuration was possible at prototype level. It is therefore propose to qualify this at space level. This is a way to increase for a same die size the quantity of pads. However, it is also requested to increase the number of IOs. Atmel will issue a proposal to develop a 625 pins MCGA.

6. Technical data package

All the following documents are ATMEL Proprietary and, as such, for confidential use only.

ATC18RHA Libraries specification
ADF-DE-R0555-CUP V1.0 July 2003

Memory Generation specification
ADF-DE-R0558-CUP V1.0 April 2003

Memory Compiler specification
ADF-DE-R0556-CUP V1.0 April 2003

EDAC specification
ADF-DE-R0575-CUP V1.0 April 2003

Design flow specification
ADF-DE-R0557-CUP V1.0 April 2003

Design kits specification
ADF-DE-R0568-CUP V1.0 April 2003

ATC18RHA V34/V35 Test Chips Specification
ADF-DE-R0561-CUP V3.0 July 2004

ATC18RHA Libraries characterization
ADF-DE-R0604-CUP V1.0 August 2003

ATC18RHA Memory compiler characterization
ADF-DE-R0690-CUP V1.0 October 2003

SEU Hardened Cells
ADF-DE-R0602-CUP V2.0 November 2004

Production design kit:
ATC18RHA Cell Library databook
ATD-TS-LR-R0251 V1.0 March 2005

ATC18RHA Buffer standard library databook
ATD-TS-LR-R0252 V1.0 March 2005

ATC18RHA Specific library databook
ATD-TS-LR-R0253 V1.0 March 2005

ATC18RHA Memory library databook
ATD-TS-LR-R0254 V1.0 March 2005

Design manual
ATD-DE-GR-R0212 V1.0 March 2005

TID test report
ATD-PL-808-CUP V1.0 March 2005

SEE test report

7. Commercial evaluation

As mentioned earlier, the SMPW service will be available for any ATC18RHA European design. It allows to share the reticule and silicon costs among several customers and therefore to ease the access to this advance technology. In addition, the designs can be or not supported by ESA. Together with the release of the production design kit, Atmel is preparing several communication actions such as a press release, a Sales bulletin (Atmel sales internal communication document). Atmel also plans to organize with ESA a social event to promote the ATC18RHA to ESA personnel and potential users.

To date the foreseen opportunities to develop ATC18RHA ASIC's are the following:

2005 : Astrium Ottobrun – AGGA3 ASIC
2006 : Saab Ericsson Space – COLE ASIC
Saab Ericsson Space – RTC ASIC
1 ASIC for Galileo
Astrium UK - AHSBB ASIC
Thales Systèmes Aéroportés - 1 or 2 ASIC
AEO - DEMDEC (MH1RT) conversion
From 2007 : Alcatel Space Toulouse - QDMX Companion Chip
Astrium Ott – FFTC
Several designs and MH1RT conversions