DOCUMENT

Heavy ion Single Event Effect Assessment test of DAC8800 from Analog Devices

Test Report

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1 INTRODUCTION

This report gives heavy ion SEE test data on the octal, 8-bit Digital-to-Analog Converter (DAC) DAC8800 from Analog Devices. The experiment was performed in July 2013 at the heavy ion facility of UCL, Louvain-la-Neuve, Belgium. The purpose of the experiment was to provide an assessment of the SEE sensitivity of the DAC8800 parts. It does not provide an exhaustive analysis for any specific application. The tests and analysis were performed with the manpower and financial support of the TEC-QEC Technical Assessment programme.

2 APPLICABLE AND REFERENCE DOCUMENTS

2.1 Applicable documents

[AD1] ESCC25100, “Single Event Effect Test Method and Guidelines”

2.2 Reference documents

[RD1] Analog Devices, DAC8800 datasheet

[RD2] Guard Sytem, TRAD, ref. TRAD/GRDSYS/USERMAN/DC/0506

3 TESTED DEVICES

The tested devices are described in Table 1.

The devices were open before heavy ion testing (see Figure 1).

Reference	**DAC8800BR/883C**
Manufacturer	Analog Devices
Function	Octal 8-bit D/A converter
Package	20-pin CERDIP
Technology	CMOS
Date code	1109

Table 1: description of the tested devices.

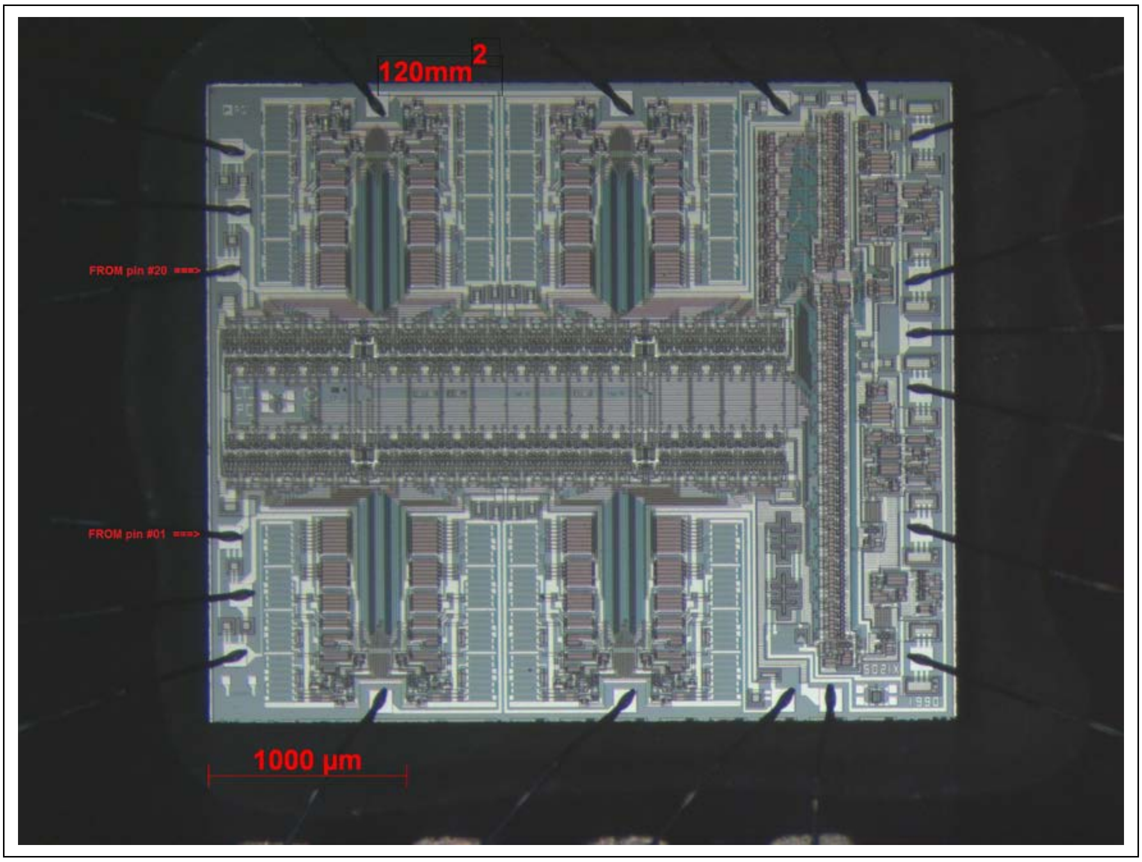

Figure 1 –Picture of the die

4 TEST FACILITY

The SEE experiment was performed with the HIF (heavy ion facility) of UCL (Université Catholique de Louvain), Louvain-la-Neuve, Belgium, with the high energy cocktail to ensure sufficient range. The highest LET ion beam (Krypton) was used. Devices were placed in vacuum.

Facility: UCL HIF

Experimenters: Michele Muschitiello, Véronique Ferlet-Cavrois, ESA-ESTEC, TEC-QEC

Operators : HIF operators, under the responsibility of Marc Loiselet and Nancy Postiau, UCL

Date: 3 July 2013

Ions: Kr 756 MeV, range 92 µm, LET 31 MeVcm^2/mg

5 TEST CONDITIONS

The DAC8800 was tested at room temperature and in dual supply configuration: V_{DD} +12V, V_{SS} -5V, with reference voltages, high V_{REF}H +12V and low V_{LOW}H -5V.

The GUARD system was used to detect potential latch-up [RD2], with the following parameters:

- current threshold 80mA,
- hold and cut-off times respectively 50ms and 200ms.

Only one DAC over the eight was selected and tested (DAC_A), though it was checked that the other DAC outputs provide qualitatively similar SEE test results. The digital content of the DAC internal register was programmed with the Agilent 81110A pattern generator before irradiation to get an intermediate output voltage value (see Table 2).

The analog output was monitored by an oscilloscope (Agilent MSO9404A). The oscilloscope is set in high impedance (1Mohms), with the following characteristics:

- Time: 2µs/div (shifted by 4µs), 125MSa/s (2k points per curve),
- Amplitude: 50mV/div (1.28V shift)

The oscilloscope was set to trigger on both positive and negative glitches. Unless specified, the triggering level is set at the DAC output level +/- half LSB (less significant bit) to detect small transients. The LSB voltage amplitude is defined by the reference voltage range (17 V, defined by VREFH +12V and low VLOWH -5V), divided by 256 (for 8-bit DAC). The DAC output level tends to shift slightly during the experiment (possible temperature or dose effects). It has to be checked between runs.

DAC_A Digital programme	DAC_A output measured on the oscilloscope	Half LSB	Triggering levels: DAC_A output +/- Half LSB
1011111	1.30 V	33 mV	1.333 V / 1.267 V

Table 2: Analog output voltage and triggering conditions.

6 TEST RESULTS

Irradiation test log is in Table 3. The device was tilted to increase the effective LET in run #57-58. The flux was kept constant at 4000 ions/cm²/s.

For the last run (#58), the triggering level is set at DAC_A output +/- 250mV to focus on large events. In all cases, a large number of positive single event transients (SETs), of either LSB or 250mV amplitude, are recorded (Figure 2).

In addition, large events are observed (Figure 3). These large events are attributed to a device reset or an upset in the DAC internal register. The permanent modification of the digital content of the DAC internal register modifies the DAC analog output value. The DAC has to be reprogrammed to recover to its initial output value. These large events are named "Resets" in Table 3.

At few occasions, the GUARD system registered single-event latch-up events (SELs). Additional testing at higher fluence, up to 1E7 cm^{-2}, at LET minimum 60 $MeVcm^2/mg$, in normal incidence and with sufficient range (>60 µm), would be required for better statistics. During the experiment, the SELs were not destructive because the DUT was protected by the GUARD system, which limits the supply current and power reset the DUT at each detected SEL.

Run #	Angle [deg.]	Eff. LET [MeVcm²/mg]	Fluence [cm⁻²]	Trigger level	SET #	SET XS [cm²]	Resets #	Reset XS [cm²]	SEL #	SEL XS [cm²]
56	0	31	2,43E6	LSB	1136	4.7E-4	0	0	0	0
57	60	62	1.42E6	LSB	1560	1.1E-3	20	1.4E-5	2	1.4E-6
58	60	62	1.35E6	250mV	77	5.7E-5	18	1.3E-5	4	3.0E-6

Table 3: Irradiation log. The SETs count the transients only (not the Resets-SEUs).

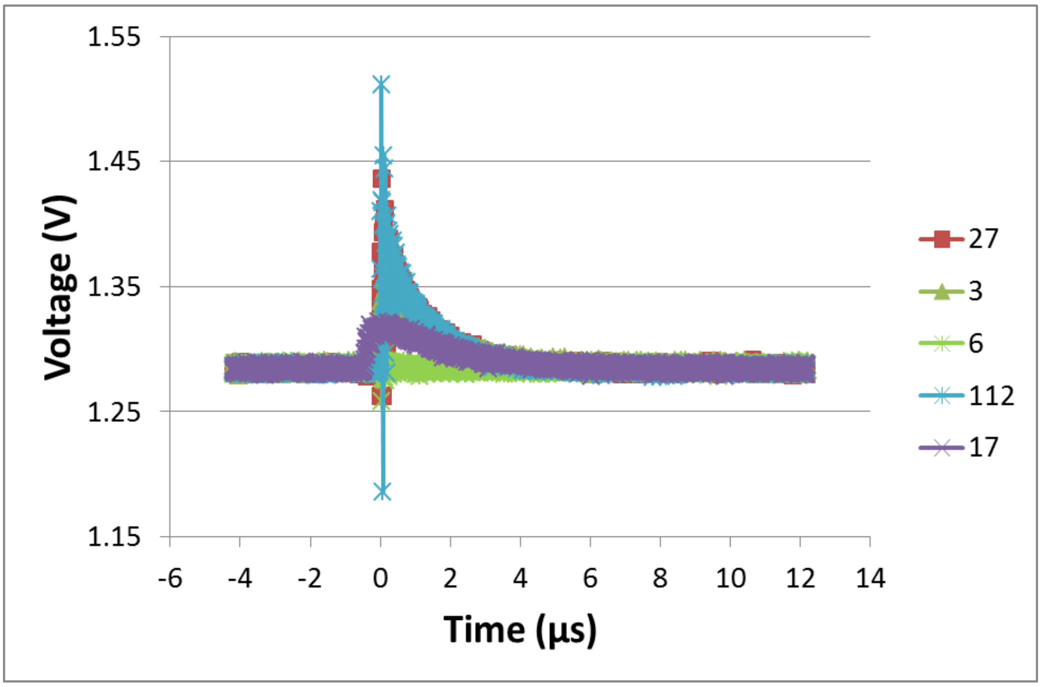

Figure 2: Examples of SETs (single event transients) measured during run #57. Similar SETs were measured during run #56.

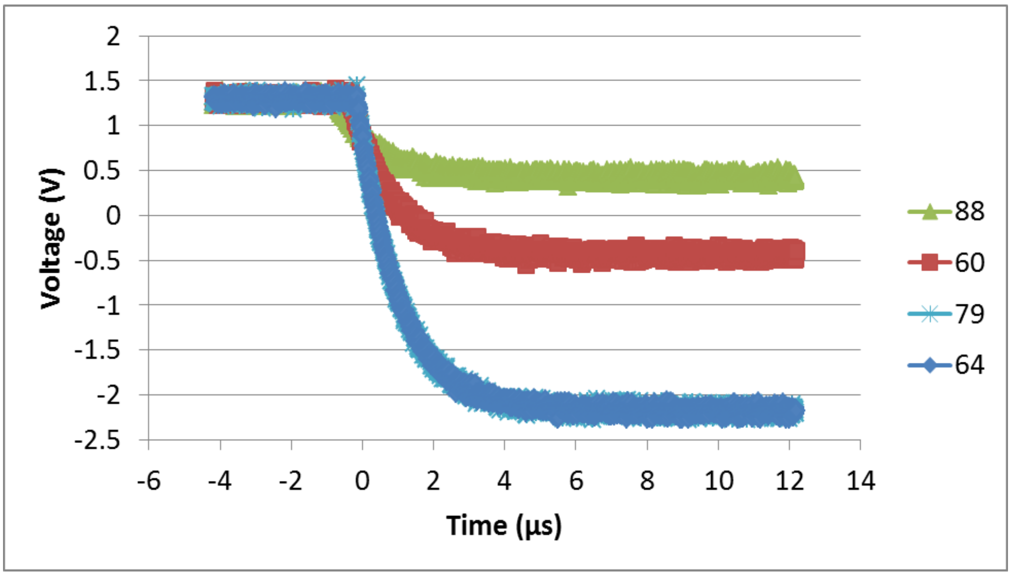

Figure 3: Examples of large events (Resets or Register SEUs) observed during run #58. Events #88 and #60 are the only intermediate level events. All other large events switch from +1.3V to about -2.2V, as run #64 and 79.

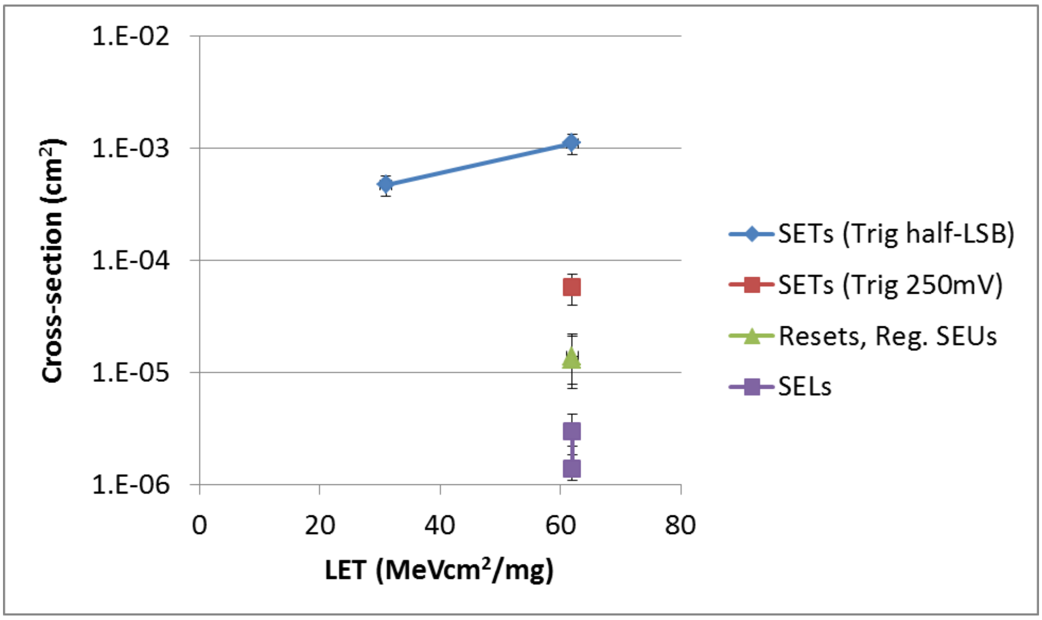

Figure 4: SEE cross-section versus ion effective LET. Error bars are plotted for a 95% confidence level.

7 CONCLUSION

The 8-bit DAC8800 from Analog Devices was tested at room temperature under heavy ions in dual supply and for one register digital content. The SEE test of the DAC8800, show that the device is sensitive to:

- **SEL:** Few SELs were observed at high LET (threshold > 31 MeVcm2/mg). The probability of SEL is relatively low. However SELs were measured at room temperature, which is not the worst-case (high temperature is the worst-case for SELs). Even if relatively rare, SELs should be taken into account by implementing a SEL circumvention circuitry.
- **Resets or SEUs in the DAC internal registers:** A significant number of these large events were measured at high LET (threshold > 31 $MeVcm^2/mg$). They induce a wrong output value. A mitigation should be implemented, by reprogramming the DAC register.
- **SETs:** numerous SETs were observed. They can however be filtered (maximum duration is 5µs),