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SINGLE EVENT EFFECTS
TEST REPORT

Test Type:	Heavy Ion
Test facility:	RADEF/JYFL, FINLAND
Test Date:	October 2009
Part Type:	HM5225165BTT-75, HM5257805BTD-75
Part Description:	256 Mbit SDR-SDRAM, 512 Mbit SDR-SDRAM
Part Manufacturer:	ELPIDA
ESA reference	ESA_QEC1002S_C
Issue	03
Date	June 17, 2010

ESA COO No2 under Contract No 22327/09/NL/SFe dated 15/10/09

Technical Officer: Fredrik Sturesson

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RESULTS SUMMARY

Facility	RADEF, JYFL, Finland
Test date	October 2009

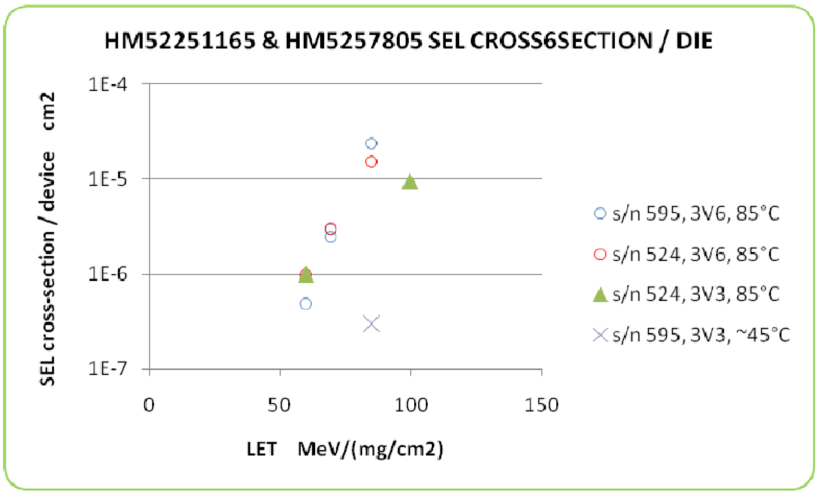
Device description

Part type:	HM5225165BTT-75
Description:	256 Mbit SDR-SDRAM
Package:	54-pin TSOP II
Technology:	-
Die dimensions:	8011.66 x 14501.46 µm
Device construction	1 chip

Part type:	HM5257805BTD-75
Description:	512 Mbit SDR-SDRAM
Package:	54-pin TSOP II
Technology:	-
Die dimensions:	8011.66 x 14501.46 µm
Device construction	2 chips back to back

Die is the same for the two devices

SEL Results



For convenience, LET values used in this plot are the ones at the DUT backside surface

For HM5257805BTD-75, only one die has been heavy ion tested.

No SEL with Xenon at normal incidence at ambient temperature with a LET between sixty and sixty nine MeV/(mg/cm2), depending on thinned die final thickness (LET is computed with SRIM 2008[1])

At 85°C SEL cross-section with the same conditions as above with Xenon of about 1 e-6 cm2
There is not much effect of DUT bias either at +3.3V or +3.6V.
Tilting the device increases the number of SELs drastically, until it goes down to none as the ion effective range decreases with the tilt angle.
This is linked with the averaged thicknesses of the samples which were prepared only for normal incidence at RADEF.

Lastly, it is worth to note that current step increases are observed even with Krypton at ambient temperatures. These steps might be linked with SEFIs occurrences however the present test was not capable of SEFI detection.

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[1] http://www.srim.org/SRIM/SRIMLEGL.htm

DOCUMENTATION CHANGE NOTICE

Issue	Date	Page	Change Item	
01	02/11/2009	All	Original issue	
02	15/02/2010	All	Including ESA comments	
03	17/06/2010	All	Including final ESA comments	

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1 Introduction

This report presents the results of Heavy Ion SEL test program carried out on ELPIDA 256 Mbit SDR-SDRAM referenced HM5225165BTT-75 and on HM5225165BTT-75 ELPIDA 512 Mbit SDR-SDRAM referenced HM5257805BTD-75.

The devices were heavy ion tested at RADEF, University of Jyväskylä, Department of Physics, Jyväskylä, Finland on 23th October 2009.

This work was performed for ESA under COO No2 under Contract No 22327/09/NL/SFe dated 15/10/09.

2 Applicable and Reference Documents

2.1 Applicable Documents

AD-1. HM5225165B Datasheet reference Elpida E0082H10 1st edition
AD-2. HM5257805B Datasheet reference Elpida E0081H10 1st edition
AD-3. Hirex proposal HRX/PRO/2739 Issue 02, dated June17, 2009

2.2 Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

3 DEVICE INFORMATION

3.1 Device description

The HM5225165B is a 256-Mbit Simple Data Rate SDRAM organized as 4194304-word x 16-bit x 4 bank. The HM5257805B is a 512-Mbit Simple Data Rate SDRAM organized as 16777216-word x 8-bit x 4 bank. All inputs and outputs are referred to the rising edge of the clock input.

Part Description: 256 Mbit SDR-SDRAM
Package: 54-pin TSOP II
Samples Used: S/N 524, S/N 520
Top Marking: 5225165BTT75
Die dimensions: 8011.66 x 14501.46 µm

Part Description: 512 Mbit SDR-SDRAM
Package: 54-pin TSOP II II
Samples Used: S/N 595
Top Marking: 5257805BRD75
Die dimensions: 8011.66 x 14501.46 µm

HM5257805B is a stacked 2- die package. In fact, these 2 dies are identical to the die used in the 256Mbit (by 16) HM5225165B memory but wired as two 512 Mbit (by 4). Die marking is shown in §3.2 here below.
For testing purpose only 1 die of HM5257805B has been considered.

3.2 Sample identification

The test was performed on three samples: two HM5225165B and one HM5257805B with a lot date code stock “0329”.

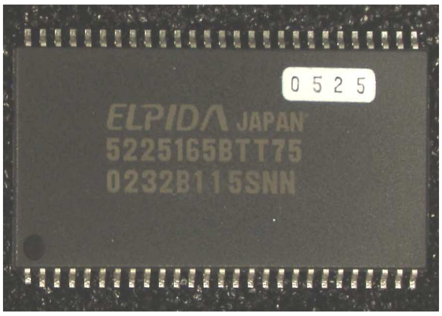


Photo 1 - Top Marking (HM5225165BTT-75)

Photo 2 - Die Marking (HM5225165BTT-75)

Photo 3 - Top Marking (HM5257805BTD-75)

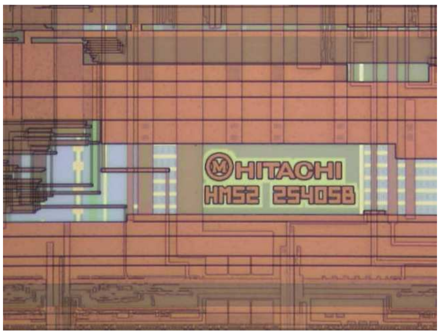


Photo 4 - Die Marking (HM5225165BTT-75)

Figure 1: Device identification

3.3 Sample preparation

The HM5225165B sample consists of one die. It is polished down to a thickness corresponding (to with) the penetration depth of the ion.

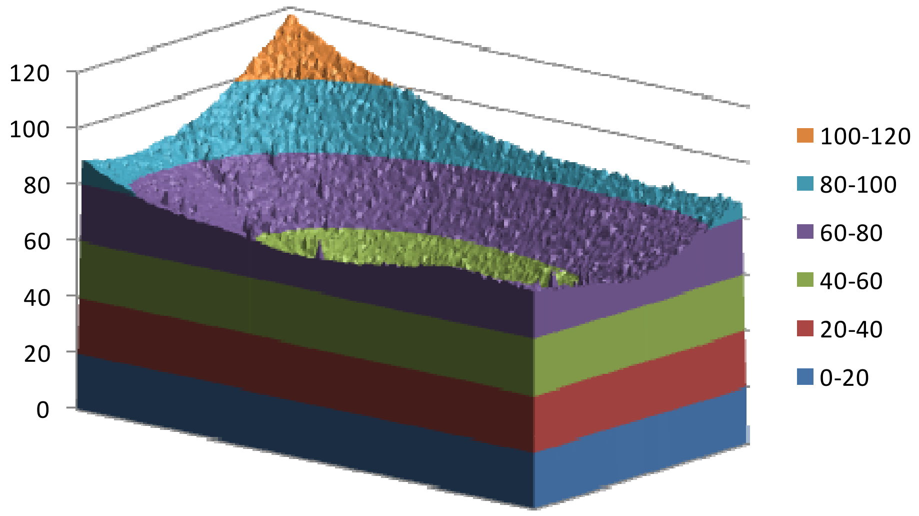
In case of the HM5257805BTD sample, it is composed of two back-to-back dies. Sample preparation is then to remove completely one die and then to polish the second one. After that, memories are fitted on separated DUT boards.

Once the samples are polished down the measurement of their thickness is executed. For this purpose the CHRocodile IT measuring system is used with accuracy of 1µm. The data obtained from the system is treated with the soft made by Hirex Engineering.

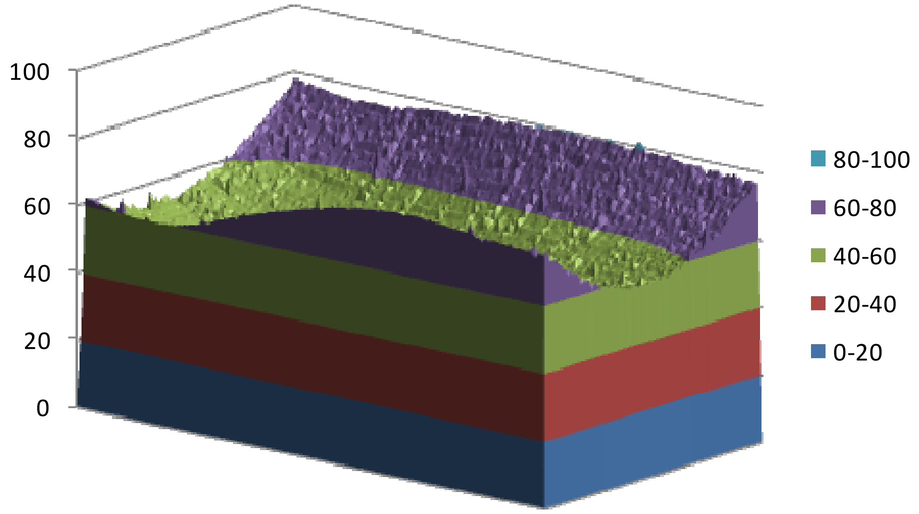
Figure 3 provides the % of die area as a function of die thickness and on the same graph, the LET value as a function of penetration depth is also plotted.

This figure helps for seeing the eventual variation of the LET value computed with SRIM2008[2] over a % of die area for the three samples prepared.

3.4 Thickness of the samples



S/N 520



S/N 524

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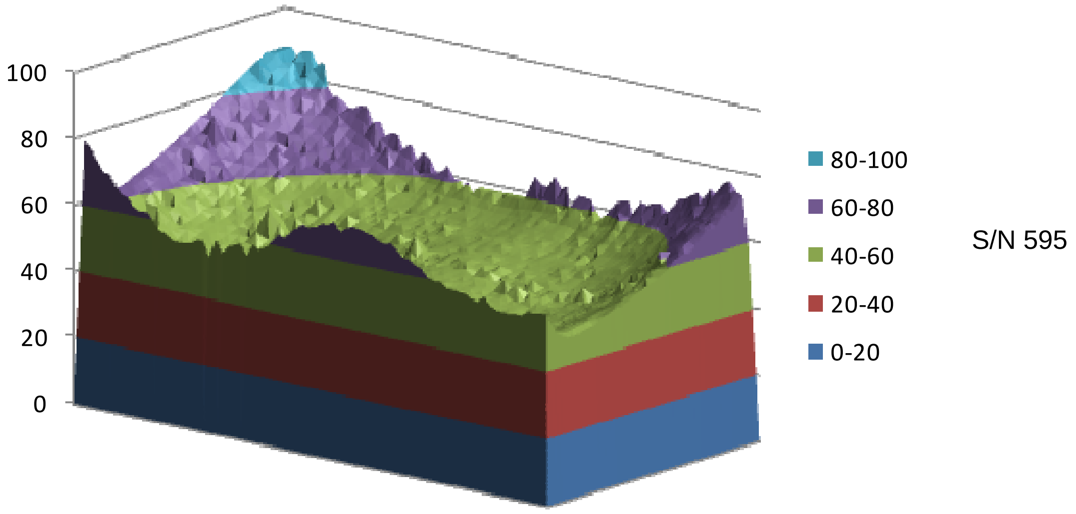
[2] http://www.srim.org/SRIM/SRIMLEGL.htm



X and Y axis units are in mm, Z axis in µm.

Figure 2: Thickness of the devices

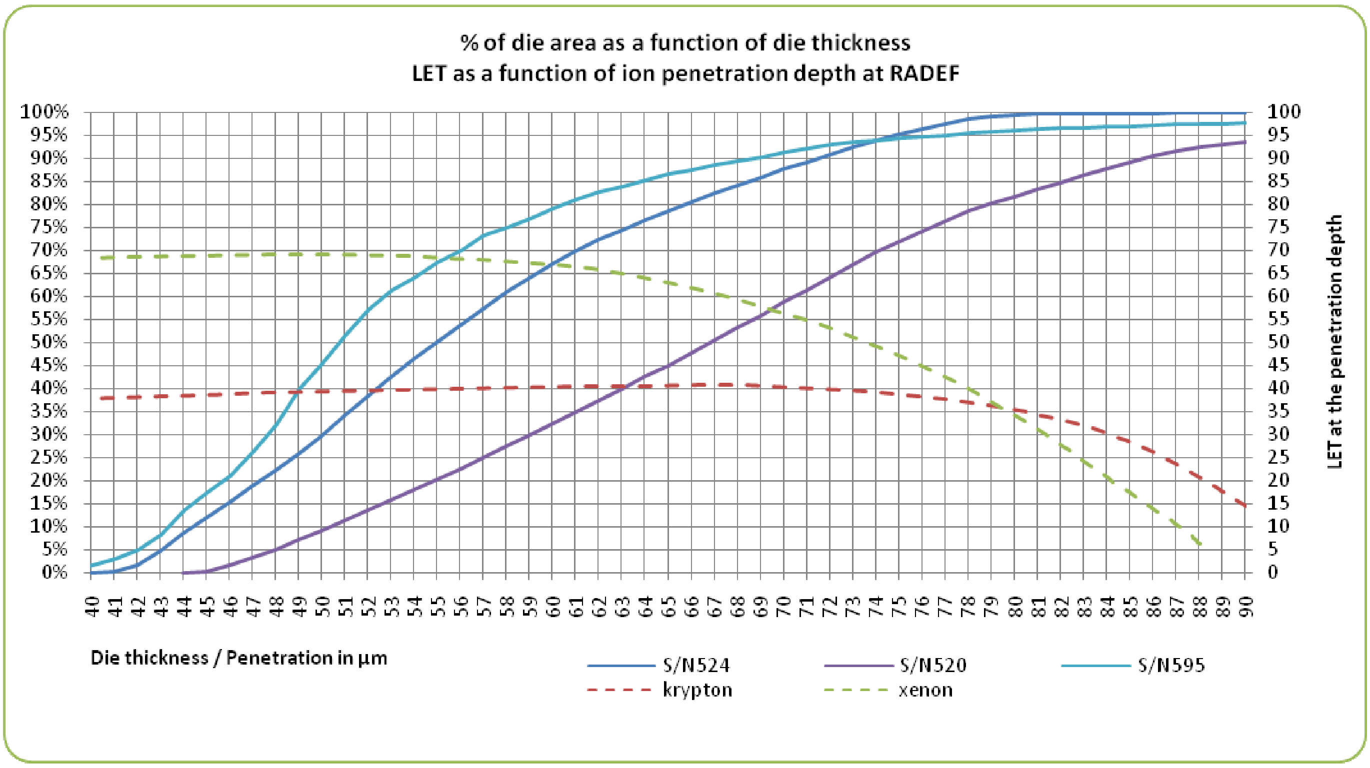


Figure 3 - % of die area as a function of die thickness together with LET values as a function of penetration depth at RADEF

4 Test definition

4.1 Test board

Figure 4 shows the principle of the Heavy Ion test system.

The devices are clocked at 50 MHz with signals generated by a Virtex 5 FPGA (Xilinx). Each memory has a dedicated +3.3V analogue supply with current limit set at 200 mA, which is approximately twice the nominal memory supply current of 100 mA. The supply voltage of the memory can reach +3.6 V

The Xilinx FPGA is powered from a separate external bench supply.

The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 16 independent channels.

A temperature Control system is used to heat the DUT. Tests are executed at different temperatures.

The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.

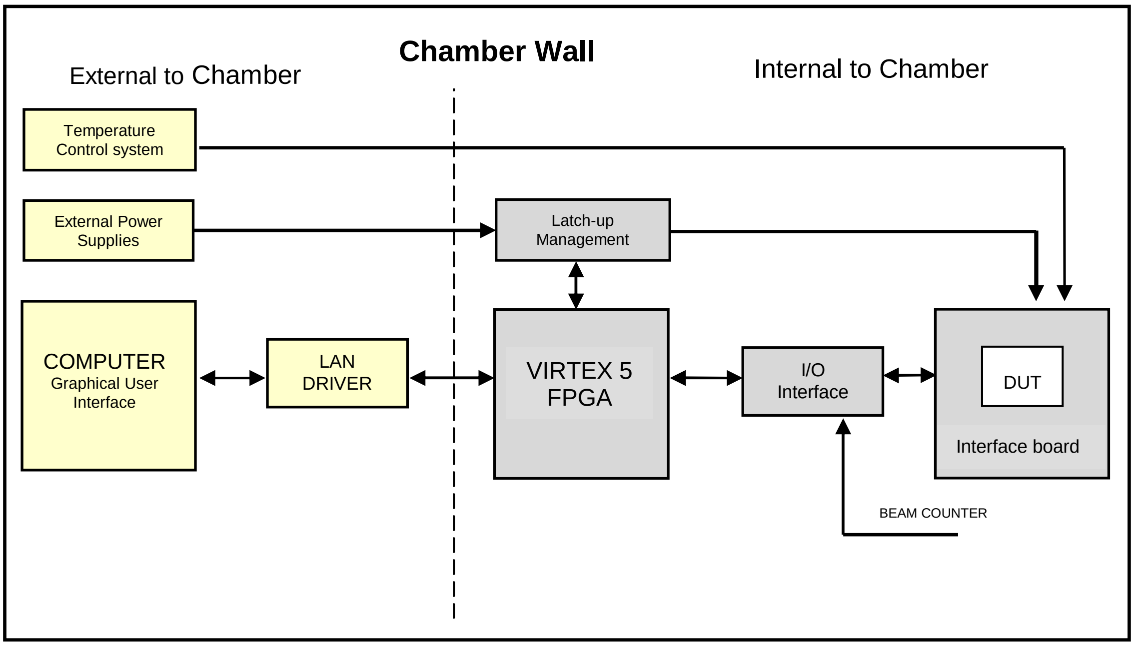


Figure 4: Heavy Ion test set-up

4.2 SDR-SDRAM Test configuration

The system provides the following features:

- 8 and 16 bits data width.
- From 256 Mbit to 512 Mbit
- Up to 4 Banks.
- Burst length of 1.
- CAS latency of 2.
- DUT Clock frequency at 50 MHz.
- Static and dynamic test conditions.
- Programmable Auto-Refresh (default value 8192 refresh cycles/49ms).
- Automatic Initialization of the DUT after power-on as well as latch-up recovery.
- “Manual” Initialization of the DUT supported at anytime.
- Fast and powerful test sequence generation.

The memory is tested in a static mode and the test sequence consists in successive iteration cycles. The time frame of one iteration cycle is approximately twelve seconds. That corresponds to the time for reading the memory plus the time to write to the entire memory and the auto refresh cycles. In case of errors detection, this cycle time can increase. During each cycle autorefresh command is sent to the memory. The memory is continuously exposed to the beam all along the test sequence.

SEL detection is performed by monitoring the DUT supply current. The SEL threshold can be adjusted during the test, but in general adjusted before starting the test.

The run test sequence is manually defined from the Graphical User Interface (GUI) providing the choice of static or dynamic test, auto refresh period, exposition time, device configuration, selected banks, SEL threshold, DUT supply voltage etc…

Test conditions
In the first test runs the value of the nominal DUT supply voltage is +3.3V. In later test runs it is increased to +3.6V. Detection SEL threshold is set at twice the nominal current value.
The tests are done at three different temperatures, room temperature (35 °C), about 45 °C and 85 °C.

5 RADEF Test Facility

Test at the cyclotron accelerator was performed at University of Jyvaskyla (JYFL) (Finland) under HIREX Engineering responsibility.

The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.
The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula

$$130\ Q^2/M,$$

where Q is the ion charge state and M is the mass in Atomic Mass Units.

Test chamber

Irradiation of components is performed in a vacuum chamber with an inside diameter of 75 cm and a height of 81 cm.
The vacuum in the chamber is achieved after 15 minutes of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the X, Y and Z directions. The possibility of rotation around the Y-axis is provided by a round table. The free movement area reserved for the components is 25 cm x 25 cm, which allows one to perform several consecutive irradiations for several different components without breaking the vacuum.
The assembly is equipped with a standard mounting fixture. The adapters required accommodating the special board configurations and the vacuum feed-throughs can also be made in the laboratory's workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components.
A CCD camera with a magnifying telescope is located at the other end of the beam line to determine accurate positioning of the components. The coordinates are stored in the computer's memory allowing fast positioning of various targets during the test.

Beam quality control

For measuring beam uniformity at low intensity, a CsI(Tl) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis.
A set of four collimated PIN-CsI(Tl) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.
Two beam wobblers and/or a 0.5 microns diffusion Gold foil can be used to achieve good beam homogeneity. The foil is placed 3 m in front of the chamber. The wobbler-coils vibrate the beam horizontally and vertically, the proper sweeping area being attained with the adjustable coil-currents.

Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI(Tl) detectors. Three collimators of different size and shape are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.
At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(Tl) detectors.

Used ions

The RADEF ions used are listed in the table below.

Ion	**Energy** (MeV)	**LET** (MeV.cm²/mg)	**Range (Si)** (µm)
131Xe35+	1217	32.10	94
83 Kr 22+	768	60	89

Table 1: Used ions and features thereof

6 SEE Test Results

Tested devices were not functional when checked before test exposure in the sense that a high number of errors were detected although DUT power consumption was normal. It was then decided to apply to the device the static test as described in §4.2 but with inactive SEU detection (without counting and recording the DUT cell errors). As no error is counted, SEFI detection is also inactive. Each time a SEL event occurs, the current iteration cycle is aborted. SEL is processed including a power off period and memory test is reinitialized followed by the next iteration.

The effective fluence for SEL corresponds to the total run fluence, minus the overall time duration during which the device is powered off after each SEL event. In this experiment, this overall time corresponds to the number of SELs multiplied by one second (one second is the duration programmed for power off time after SEL).

Detailed results per run are provided in the Table 2 of the paragraph 8.

6.1 SEL

For the three samples tested, no SEL was observed at ambient with Xenon at normal incidence. It corresponds to a LET value above sixty on more than 80% of die area for S/N 524 and S/N595 die (see Figure 3).

At about 45 °C and with a tilt of 45 deg few SELs were observed with a corresponding SEL cross-section / die of 3 e-07 cm2. There is not much difference between +3.3V and +3.6V bias conditions.

At 85°C SELs were observed at normal incidence with a corresponding SEL cross-section of about 1 e-06 cm2 / die. By tilting the device the SEL cross section increased drastically until the ion effective range is no more compatible with die thickness.
This can be observed in Figure 6 where S/N524 and a tilt of 53deg. show a decrease in SEL cross-section value which might be explained by the DUT lower supply voltage. However testing the device with a tilt angle of 60 deg. show no more SEL as ions are very likely stopped before sensitive volume.

To illustrate these results, LET plots versus ion range for two different ions and at two different energies in Silicon target have been produced thanks to SRIM2008 program[3]. It computes different features of the transport of ions in matter. Figure 7 and **Figure 8** have been plotted for Krypton and Xenon with nominal energy value of 768 MeV for Krypton and 1217 MeV for Xenon, respectively. The value 0 of Range corresponds to the start of the silicon surface (backside) For Xenon, several tilt angles have been considered. **Figure 8** shows that with 60 deg. the vertical range into the device is below -45 um which is less than the thickness of all the dies as visualized in Figure 2. Consequently no SEL can be achieved with 60 deg. tilting.

Lastly some DUT bias currents steps have been observed during the runs even with Krypton at ambient and normal incidence. It is possible that these steps might correspond to SEFI occurrences (see Figure 5).

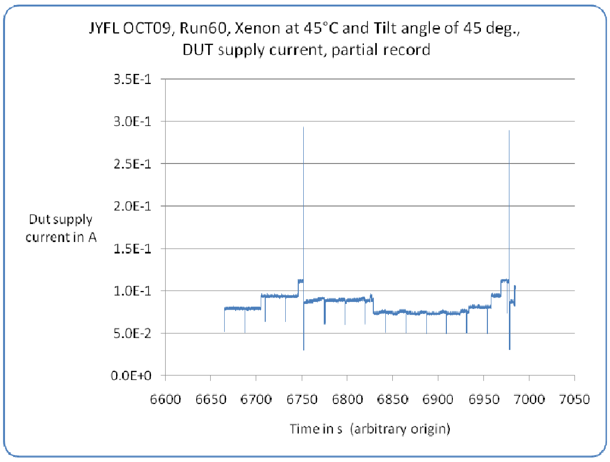


Figure 5 – DUT supply current record showing step currents in addition of two SELs

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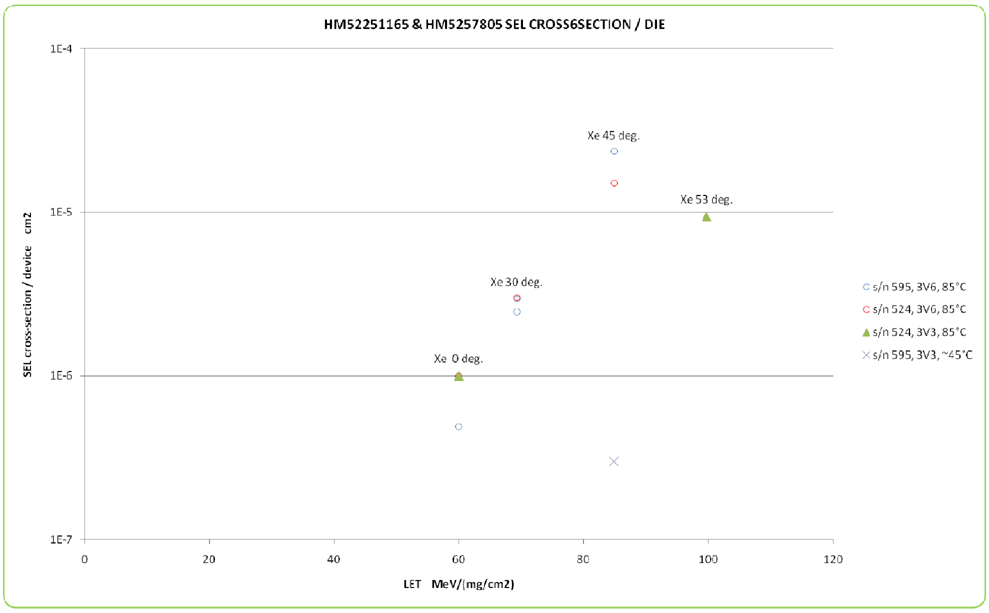
[3] http://www.srim.org/SRIM/SRIMLEGL.htm



LET values used are the one at the DUT backside surface

Figure 6: RADEF OCT 09, HM5257805 & HM5225165B, SEL cross-section/device

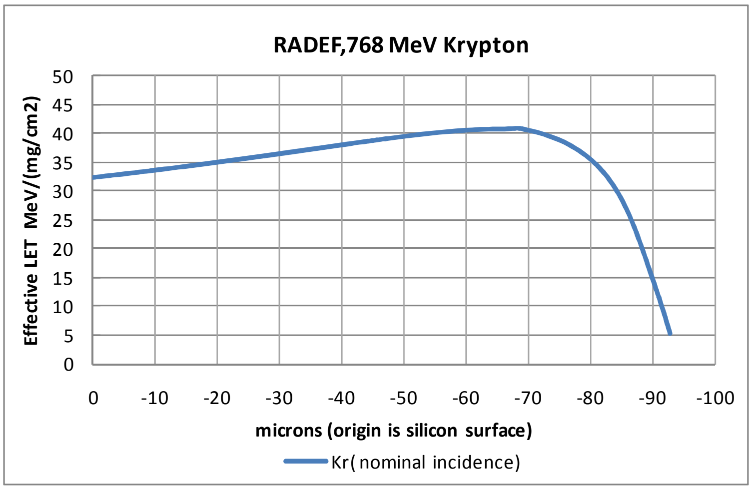


Figure 7: RADEF, 768 MeV Krypton (LET is computed with SRIM 2008[4])

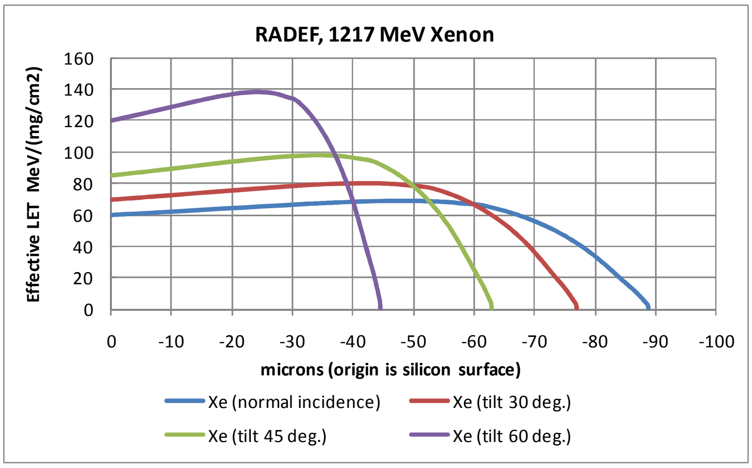


Figure 8: RADEF, 1217 MeV Xenon (LET is computed with SRIM 2008)

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[4] http://www.srim.org/SRIM/SRIMLEGL.htm

7 Detailed results per run

SEL run results table:

HRX RUN	Hirex test run number
Part Type	Type of sample
S/N	Hirex sample number
DUT Voltage	DUT supply voltage1 (V)
DUT Temp	DUT temperature (°C)
Ion	Ion specie
Energy	Ion incident energy (MeV)
LET	Linear Energy Transfer (MeV/(mg/cm^2))
TILT	DUT tilt angle with beam direction (deg)
Eff LET	LET / (cos(tilt angle) (MeV/(mg/cm^2))
Eff Range	Ion range in Silicon (microns)
Fluence	Cumulated number of ions over the test run (cm^{-2})
Total Time	Time with beam (s)
Flux	Effective Fluence (cm^{-2} x s^{-1})
SEL	Number of SELs
SEL X section	SEL error cross-section per device (cm^2)

7.1 Detailed run table

Part type	HRX RUN	S/N #	Test cond.	Auto refresh period ms	DUT bias voltage	DUT Temp.	ION	LET	TILT	LET eff at DUT back surface	Range at DUT back surface	Fluence	Total time (sec.)	Flux	SEL	SEL cross-section / die	Comment
HM5225165B	24	520	Auto-refresh	49 ms	3,6 V	25 °C	82Kr24	32,1	0 °	32,10	94	2,00E+06	443	4,51E+03	0		
HM5225165B	25	520	Auto-refresh	49 ms	3,6 V	25 °C	82Kr24	32,1	0 °	32,10	94	2,00E+06	445	4,49E+03	0		
HM5225165B	19	524	Auto-refresh	49 ms	3,3 V	25 °C	82Kr22	32,1	0 °	32,10	94	2,00E+06	1219	1,64E+03	0		
HM5225165B	33	524	Auto-refresh	49 ms	3,3 V	25 °C	131Xe+35	60	0 °	60,00	89	2,00E+06	628	3,18E+03	0		
HM5225165B	20	524	Auto-refresh	49 ms	3,6 V	25 °C	82Kr22	32,1	0 °	32,10	94	2,00E+06	547	3,66E+03	0		current steps
HM5225165B	34	524	Auto-refresh	49 ms	3,6 V	25 °C	131Xe+35	60	0 °	60,00	89	2,00E+06	696	2,87E+03	0		
HM5257805B	52	595	Auto-refresh	49 ms	3,3 V	25 °C	131Xe+35	60	0 °	60,00	89	2,65E+06	479	5,53E+03	0		
HM5257805B	53	595	Auto-refresh	49 ms	3,6 V	25 °C	131Xe+35	60	0 °	60,00	89	1,06E+06	198	5,35E+03	0		
HM5225165B	29	520	Auto-refresh	49 ms	3,3 V	45 °C	131Xe+35	60	0 °	60,00	89	2,00E+06	638	3,13E+03	0		
HM5225165B	30	520	Auto-refresh	49 ms	3,6 V	45 °C	131Xe+35	60	0 °	60,00	89	2,00E+06	542	3,69E+03	0		
HM5257805B	59	595	Auto-refresh	49 ms	3,3 V	45 °C	131Xe+35	60	45 °	84,85	89	1,00E+07	343	2,92E+04	0		
HM5257805B	60	595	Auto-refresh	49 ms	3,3 V	45 °C	131Xe+35	60	45 °	84,85	89	1,00E+07	343	2,92E+04	3	3,00E-07	
HM5257805B	61	595	Auto-refresh	49 ms	3,3 V	45 °C	131Xe+35	60	0 °	60,00	89	1,00E+07	343	2,92E+04	0		
HM5225165B	26	520	Auto-refresh	49 ms	3,6 V	85 °C	82Kr24	32,1	0 °	32,10	94	2,00E+06	448	4,46E+03	0		
HM5225165B	31	520	Auto-refresh	49 ms	3,6 V	85 °C	131Xe+35	60	0 °	60,00	89	2,00E+06	556	3,60E+03	3		
HM5225165B	22	524	Auto-refresh	49 ms	3,3 V	85 °C	82Kr23	32,1	0 °	32,10	94	2,00E+06	479	4,18E+03	0		
HM5225165B	38	524	Auto-refresh	49 ms	3,3 V	85 °C	131Xe+35	60	53 °	99,70	89	5,00E+06	517	9,67E+03	47	9,40E-06	
HM5225165B	39	524	Auto-refresh	49 ms	3,3 V	85 °C	131Xe+35	60	0 °	60,00	89	5,00E+06	166	3,01E+04	5	1,00E-06	
HM5225165B	23	524	Auto-refresh	49 ms	3,6 V	85 °C	82Kr24	32,1	0 °	32,10	94	2,00E+06	420	4,76E+03	0		
HM5225165B	35	524	Auto-refresh	49 ms	3,6 V	85 °C	131Xe+35	60	0 °	60,00	89	2,00E+06	575	3,48E+03	2	1,00E-06	
HM5225165B	36	524	Auto-refresh	49 ms	3,6 V	85 °C	131Xe+35	60	45 °	84,85	89	1,00E+06	416	2,40E+03	15	1,50E-05	
HM5225165B	37	524	Auto-refresh	49 ms	3,6 V	85 °C	131Xe+35	60	30 °	69,28	89	2,00E+06	565	3,54E+03	6	3,00E-06	
HM5257805B	57	595	Auto-refresh	49 ms	3,3 V	85 °C	131Xe+35	60	30 °	69,28	89	2,03E+06	343	5,92E+03	5	2,46E-06	
HM5257805B	54	595	Auto-refresh	49 ms	3,6 V	85 °C	131Xe+35	60	0 °	60,00	89	2,04E+06	421	4,85E+03	1	4,90E-07	
HM5257805B	55	595	Auto-refresh	49 ms	3,6 V	85 °C	131Xe+35	60	45 °	84,85	89	1,06E+06	343	3,09E+03	25	2,36E-05	
HM5257805B	56	595	Auto-refresh	49 ms	3,6 V	85 °C	131Xe+35	60	30 °	69,28	89	2,03E+06	343	5,92E+03	6	2,96E-06	
HM5257805B	58	595	Auto-refresh	49 ms	3,6 V	85 °C	131Xe+35	60	60 °	120,00	89	2,26E+06	343	6,59E+03	0		

Table 2: RADEF, OCT09, run table for the HM5225165 & HM5257805 dies