HIREL EXPERTISE
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SINGLE EVENT EFFECTS
TEST REPORT

Part Type:	A3PE3000L
Part Description:	ProASIC3L Flash Based FPGA
Part Manufacturer:	ACTEL
Test Facility	RADEF, Jyväskylä, Finland
Test Date	June 2010 & November 2010
Test Facility	PIF, PSI, Villigen, Switzerland
Test Date	March 2011
Issue	03
Date	August 23rd, 2011

ESA ESTEC Contract No 22327/09/NL/SFE

ESA ESTEC Technical Officer: Christian Poivey

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DOCUMENTATION CHANGE NOTICE

Issue	Date	Page	Change Item	
01	01/10/2010	All	Draft issue	
02	11/05/2011	All	Added RADEF November 2010 and PSI March 2011 campaign data	
03	23/08/2011	63	Modified the SRAM heavy ion cross-section plot and Weibull parameters values	
		68	Added samples status after the heavy ion and the samples status after all tests in the CONFIGURATION FLASH, CHARGE PUMP & IN SYSTEM PROGRAMMING paragraph.	
		89	Modified the SRAM conditions and SEU tables	

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RESULT SUMMARY

The A3PE3000L flash FPGA from the ProASIC3L family from ACTEL manufacturer was SEE characterized at the following facilities under ESA ESTEC contract number 22327/09/NL/SFE:

- ✓ RADEF, University of Jyväskylä, Jyväskylä, Finland in June and November 2010.
- ✓ PIF, PSI, Villigen, Switzerland in March 2011.

SEE mitigation methods applied on the same die were also characterized and their SEE sensitivities evaluated. 2 test vehicles (TV) were designed and tested. The first TV implemented 14 shift registers, one clock conditioning circuit with phase-locked loop and 100 % of the SRAM and UFROM memories. The second TV implemented SEU and SET mitigation on 6 shift registers. All shift registers of both TVs were made of 1024 registers made of D core flip-flop with clear and enable active high.

Device description:

Part type:	A3PE3000L
Part family	ProASIC3L
Manufacturer:	ACTEL
Package:	PQ208
Date code:	0922
Used samples:	Serialized from SN 1 to SN 24.
Package marking:	QHR8G
Die dimensions:	10.8 x 10.8 mm

SEL:

No SEL was observed up to a LET of 55 MeV.cm²/mg, a cumulated fluence of 1E7 p/cm², a temperature up to 125 °Celsius and a bias voltage of 1.65 Volts for the core voltage and 3.6 Volts for the input/output voltage.

SEFI:

One SEFI was detected and recorded during the campaign at RADEF on November 2010 on the RUN 112 with an effective LET of 55 MeV.cm²/mg. The device was configured with the TV2 and all shift registers were tested with a working frequency of 2 MHz. From the Iteration N° 257 (a fluence of 3.69E5 p/cm²) up to the end of the run (a fluence of 5E5 p/cm²) all the read data from the device were read at the low state (“0”). The device did not recover from the SEFI state by itself. The recovery took place after a power cycle of the device allowing the next run with the exact same conditions to be performed without any more SEFI detected.

SEU:

The flash (configuration and user) was not seen sensitive to SEE up to a LET of 55 MeV.cm²/mg. It remained intact. However the programming part of the flash was stated sensitive to SEU, SHE and to the cumulated dose deposited by the cumulated fluence.

Concerning the shift registers:

- ✓ The reference and standard shift register (TV1 - SR1) SEU cross-section is characterized with an asymptotic cross-section below 3E-7 cm² per bit and a LET threshold below 1.8 MeV.cm²/mg. An extremely light influence of the working frequency can be seen on the SEU cross-section. Most errors are SBUs where almost 2/3 is due to clear transition. Some MBUs largely made of arbitrary numbers of consecutive reset bits (clear bit) were counted as well. A reference Weibull curve plotted on the Figure 1 was estimated from the measured points and added to all SEU cross-sectional area per bit for comparison purpose.
- ✓ The channel implementing combinational cells on the enable signal path (TV1 - SR2) results in an SEU cross-sectional area per bit similar to the reference. The frequency does not appear to influence the SEU cross-section or so lightly than it is not visible on the cross-section curve. Most errors are SBUs with more than half due to clear transition. MBUs are made of errors with the same signatures than the reference channel. However another signature shows un-shifted quartets caused by an SET on the enable signal caught at the active edge of the clock: data are held from shifting. Very few SETs on the enable signal were caught that way.
- ✓ The channel implementing combinational cells on the reset signal path (TV1 - SR3) results in a SEU

cross-sectional area per bit characterized with an asymptotic cross-section below 1E-6 cm² and a LET threshold around 1.8 MeV.cm²/mg. This SEU cross-section per bit is higher than the reference. Almost 80% of SEUs are SBUs and 70% of those are due to clear transition. There is a high count of MBU compared to the reference channel and almost all of those are due to arbitrary numbers of reset bits.

- ✓ The channel implementing combinational cells in-between each register (TV1 - SR4) results in an SEU cross-sectional area per bit similar to the reference. A very light influence of the working frequency can be seen on the SEU cross-section. Most SEUs are SBUs and 2/3 of those are due to clear transition. Comparing SEU cross-section and error signatures, this channel seems very similar to the reference one.
- ✓ The channels implementing the DDR I/O registers (TV1 - SR5 to 8) and the channels implementing LVDS buffers (TV1 - SR9 and 10) show a SEU cross-sectional area per bit very similar to the reference. SEE signatures are also like the references ones.
- ✓ The channels clocked by the PLL output clock (TV1 - SR11 to 14) have a SEU cross-sectional area per bit identical to the reference. Most SEUs are SBUs with more than half due to clear transition. MBUs are largely attended to reset bits and flipped bits: it was not seen a total flip or stuck bit of the channels that could lead to a total or partial stop of the PLL output clock.
- ✓ The channel implementing sequential cell triplication (TV2 - SR1) results in a SEU cross-sectional area per bit characterized with an asymptotic cross-section below 2E-9 cm². There is a large difference (around 2 decades) on its SEU cross-section and the reference one. It is based on a poor statistic attended to the small number of errors. More than 70 % of SEUs are SBUs and all of those are due to clear transition. The high percentage of MBU (almost 30 %) compared to the reference channel is made of arbitrary numbers of reset bits. The sequential cell triplication SEU mitigation decreases the total amount of SEU and changes the SBU vs. MBU ratio. All events appearing on the only asynchronous global (or local) reset signal shared between all registers induced all recorded SEU without any available correction from the voter.
- ✓ The channel implementing sequential cell triplication and I/O bank triplication (TV2 - SR2) has a SEU cross-sectional area per bit characterized with an asymptotic cross-section below 2E-7 cm² and a LET threshold below 10 MeV.cm²/mg, lower than the reference but still higher than the channel implementing only sequential cell triplication. This result seems unrealistic compared to the other channels implementing only the sequential cell triplication (TV2 SR1). Because both channels use the same sequential cell triplication as SEU mitigation, a smaller (or in the worst case an equivalent) cross-section was expected on the SR2 channel. No explanation has been found yet to explain the result on this channel.
- ✓ The channel implementing the SET filtering method with a delay of 2 ns (TV2 - SR3) has a SEU cross-sectional area per bit similar to the reference. Its SEEs signatures are also very like the reference channel.
- ✓ The channel implementing sequential cell triplication, I/O block triplication and SET filtering with a delay of 3 ns (TV2 - SR4) did not show any event up to a LET of 55 MeV.cm²/mg and a cumulated fluence of 2E6 p/cm².
- ✓ The channel implementing sequential cell triplication, I/O block triplication and logic duplication (TV2 - SR5) did not show any event up to a LET of 55 MeV.cm²/mg and a cumulated fluence of 2E6 p/cm².
- ✓ The channel made of full TMR mitigation (TV2 - SR6) was the source of only 2 SBUs (single bit cleared). Based on an extremely poor statistic this channel look close to the result of the channel implementing only sequential cell triplication (TV2 - SR1).
- ✓ All the channels of the TV1, expected the channels clocked with the PLL output clock were tested to proton. They all have the same proton SEU cross-section per bit measured from a low sensitivity (with a low number of errors) below 1E-13 cm² at 230 MeV. The reference channel proton SEU cross-section is plotted on the Figure 2.

The SRAM heavy ion SEU cross-sectional area per bit is characterized with an asymptotic cross-section around 4E-8 cm² per bit and a LET threshold below 1.8 MeV.cm²/mg. The SRAM proton SEU cross-sectional area per bit is characterized with an asymptotic cross-section below 1E-13 cm² and an energy threshold below 23.5 MeV. All SEEs are upsets with a very large majority of SBUs very well balanced on bit position, on set / clear transitions and on RAM block position.

The PLL output clock never stopped. However the PLL lock signal is sensitive to PLL lock signal SEFI and to SET. It can be seen than the frequency influences those sensitivities. Because the PLL was set on a static mode to a nominal frequency of 200 MHz, increasing the gap between the nominal frequency and the working frequency increased those sensitivities. In nominal condition no any PLL lock signal SEFI was recorded on the PLL lock signal while its SET cross-sectional area based on a poor statistic attended to the small number of errors is characterized with an asymptotic cross-section below 1E-5 cm² and a LET threshold around 1.8 MeV.cm²/mg.

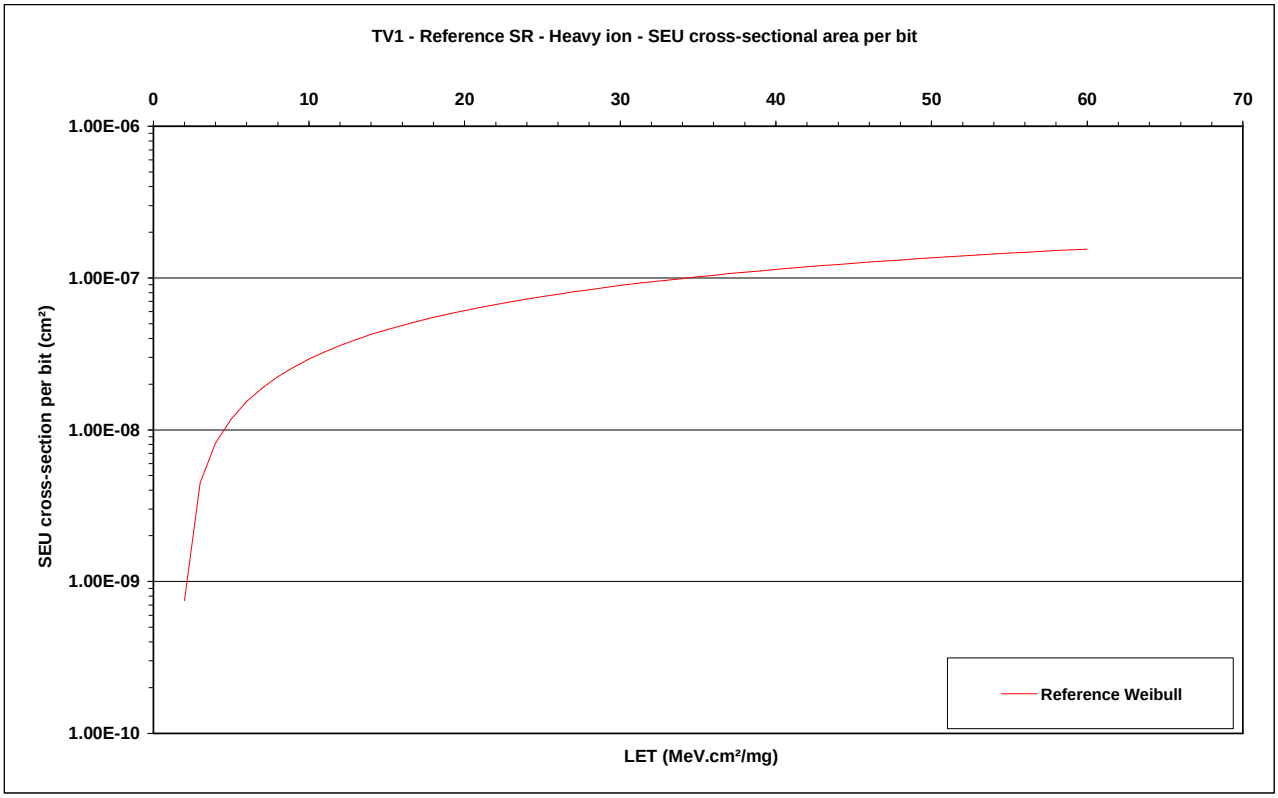

Figure 1: TV1 - Reference SR - Heavy ion - SEU cross-sectional area per bit

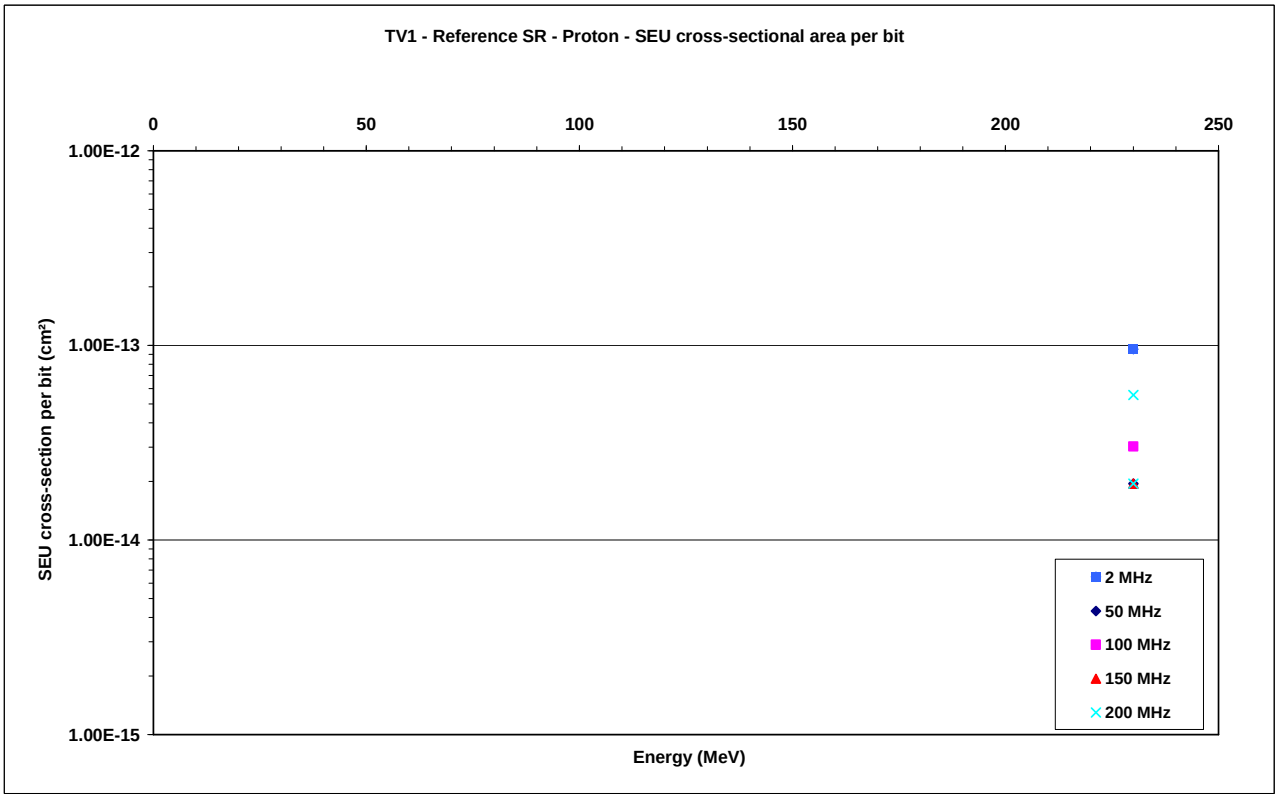

Figure 2: TV1 - Reference SR - Proton - SEU cross-sectional area per bit

A3PE3000L SEE TEST REPORT
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1 Introduction

ACTEL ProASIC3 flash FPGA family offers the unique combination of re-programmability and non-volatility in a high density programmable logic product. At the start of the project, the family was the only one that covered the 1 Million gates capacity requirements for space applications. Preliminary radiation test RD-1 and RD-2 results were promising. For those reasons, the ProASIC3 family was very attractive for space applications.

The objective of this study is to fully characterize the radiation sensitivity of the ProASIC3 FPGA, by performing heavy ions, proton and total ionization dose tests.

This report presents the results of Single Event Effect characterization program carried out on the device referred A3PE3000L from the ACTEL ProASIC3L Flash Based FPGA family. The Single Event Effects were characterized using:

- ✓ Heavy ions accelerator at RADEF, University of Jyväskylä, Department of Physics, Jyväskylä, Finland in June 2010 and November 2010.
- ✓ Proton accelerator at PIF, Paul Scherrer Institut (PSI), Villigen, Switzerland in March 2011.

This work was performed for ESA ESTEC under the contract number 22327/09/NL/SFE.

2 Applicable and Reference Documents

2.1 Applicable Documents

AD-1 Statement Of Work, Radiation Testing of Candidate Microelectronics Parts for Space Applications - Frame Contract, Reference TEC-QCA/CP/SOW/2008-1 Issue: 1, Revision C, 26.06.2008

AD-2 Statement Of Work, Radiation Testing of Candidate Microelectronics Parts for Space Applications - Call-Off Order 1, Reference TEC-QCA/CP/SOW/2008-2-COO1 Issue: 1, Revision C, 26.06.2008

AD-3 Hirex Engineering Proposal, Radiation Characterization of ACTEL ProASIC3L family, reference HRX/PRO/2427, Issue 1, September 15th, 2009

AD-4 ProASIC3L low power flash FPGAs Datasheet v1.3, February 2009

AD-5 Hirex Engineering A3PE3000L design report referred HRX/SEE/0286

2.2 Reference Documents

RD-1. S. Rezgui & al., “New Reprogrammable and Non-Volatile Radiation Tolerant FPGA: RTA3P,” presented at RADECS 2007, Deauville, France, September 2007

RD-2. S. Rezgui & al., “New Methodologies for SET Characterization and Mitigation in Flash-Based FPGAs,” IEEE Trans. Nuc. Sci., vol, 54, n°6, pp. 2512-2524, Dec. 2007

RD-3. ECSS Q 60-02, “Space Product Assurance, ASIC and FPGA development,” July 2007

RD-4. Proton Irradiation Facility at the PROSCAN project of the Paul Scherrer Institute PIF facility at PSI, Ulrike Grossner, Wojtek Hajdas, Ken Egli, Roger Brun, and Reno Harboe-Sorensen, RADECS 2009.

3 DEVICE INFORMATION

3.1 Device description

The tested device is the A3PE3000L. It is the biggest device by the number of gates from the ProASIC3L FPGA family from ACTEL: It includes 3 Million gates. This device is a commercial device manufactured with a 0.13 µm CMOS flash technology packaged in a PQFP 208 pins. The Radiation-Tolerant (RT) family uses the same designs and processes. So the RT3PE3000L Radiation-Tolerant device uses the same silicon as the commercial device A3PE3000L. The Table 1 summarizes the description of the device.

Part type	A3PE3000L
Part Family	ProASIC3L
Manufacturer	ACTEL
Package	PQ208
Date code	0922
Package marking	QHR8G
Die dimensions	10.8 x 10.8 mm
Used samples	Serialized from Serial Number (SN) 1 to 24

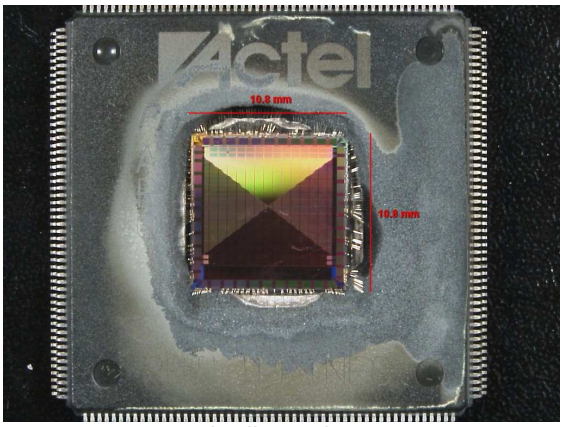
Table 1: Device description

3.2 Device Procurement

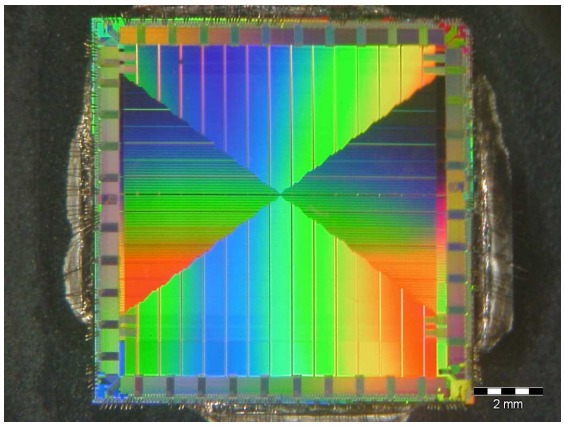
40 samples of A3PE3000L packaged in a PQFP 208 pins were provided by ACTEL to ESA. All samples were delivered at HIREX. 18 samples (serialized from SN 1 to SN 18) were dedicated to heavy ion testing and were delidded. 6 samples (serialized from SN 19 to SN 24) were reserved for proton testing and were left untouched. The left over samples were reserved for Total Ionization Dose (TID) testing.

3.3 Device identification

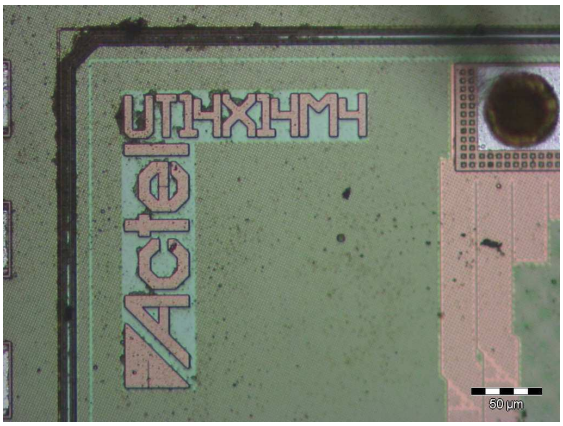
Package marking



Die dimensions



Full die view



Die marking

Figure 3: Device identification

3.4 Samples identification

The device identification code (IDCODE) is 3E74E1CF. All samples are from the same reference (same device) and share the same IDCODE. However each sample is stamped with its own Flash Serial Number (FSN). The FSN of used samples are provided in the following Table 2.

Serial Number (SN)	Flash Serial Number (FSN)
1	00f5dd483c70
2	00f5dd4c1c64
3	00f5dd484064
4	00f5dd483870
5	00f5dd4c2468
6	00f5dd4c1c70
7	00f5dd480c70
8	00f5dd48286c
9	00f5dd4c2c78
10	00f5dd48206c
11	00f5dd4c405c
12	00f5dd4c304c
13	00f5dd4c2884
14	00f5dd4c2860
15	00f5dd4c3078
16	00f5dd4c1874
17	00f5dd4c4074
18	00f5dd4c3478
19	00f5dd4c487c
20	00f5dd4c2478
21	00f5dd481c64
22	00f5dd4c4078
23	00f5dd481470
24	00f5dd4c2078

Table 2: Sample identification

A visual identification was materialized on each DUT board where the serial number of the sample was incised. The SN and FSN correspondence was verified at all time.

4 RADEF TEST FACILITY

2 Heavy ions test campaign were performed at the cyclotron accelerator at the University of Jyväskylä, Finland in June and November 2010 under HIREX Engineering responsibility.

The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.

The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula

$$130\ Q^2/M,$$

Where Q is the ion charge state and M is the mass in Atomic Mass Units.

4.1 Beam quality control

For measuring beam uniformity at low intensity, a CsI(Tl) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis.

A set of four collimated PIN-CsI(Tl) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.

Two beam wobblers and/or a 0.5 microns diffusion Gold foil can be used to achieve good beam homogeneity. The foil is placed 3 m in front of the chamber. The wobbler-coils vibrate the beam horizontally and vertically, the proper sweeping area being attained with the adjustable coil-currents.

4.2 Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI (Tl) detectors. Three collimators of different size and shape are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.

At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(Tl) detectors.

4.3 Used ions

The RADEF used ions are listed in the following table.

Ion specie	Energy (MeV)	LET Meas. @ Surface (MeV.cm²/mg)	Range (Si) (µm)
$^{15}N^{+4}$	139	1.87	202
$^{20}Ne^{+6}$	186	3.68	146
$^{40}Ar^{+12}$	372	10.08	118
$^{56}Fe^{+15}$	523	18.84	97
$^{82}Kr^{+22}$	768	30.44	94
$^{131}Xe^{+35}$	1217	54.95	89

Table 3: RADEF, used ions and features

5 PIF TEST FACILITY

Proton tests were performed at the Proton Irradiation Facility (PIF) at Paul Scherrer Institut (PSI), Villigen, Switzerland in March 2011 under HIREX Engineering responsibility.

A description of PIF test facility can be found in RD-4. As shown in Figure 4, proton beam from COMET cyclotron is delivered to the experimental PIF cave with an input energy that can be varied from few MeVs up to 250 MeV. Then in PIF room, local copper degraders can be inserted into the beam to obtain the different user energies.

In March 2011, 230 MeV input beam's energy was selected and calibrated. The corresponding calibration result is shown in Figure 5.

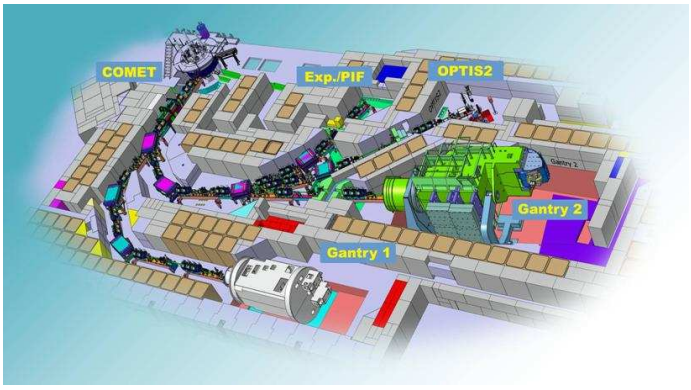


Figure 4: Proscan facility

						Target(1)	Degr(2)	Target(1)	Degr(2)	Target(1)	Degr(2)	
	Energy	Degr.	Plastic	IC-target	IC-degr	Fac. 20nA	Fac. 20nA	Fac. 200nA	Fac. 200nA	Fac. 2 uA	Fac. 2 uA	PL6
	[MeV]	[mm]	[cnt/1s]	[cnt/1s]	[cnt/1s]	[p/cnt/cm2]	[p/cnt/cm2]					distance 5.0 cm to collim
Pos 1	**230**	**0.0**	265698	724	288	6143.5	15548.5					collim 20 mm diam
1	**230**	**0.0**	265662	721	286	6168.3	15656.4					1 sec test
			4.5	3.20	3.2	**6.16E+03**	**1.56E+04**	**6.16E+04**	**1.56E+05**	**6.16E+05**	**1.56E+06**	
Pos 1	**200**	**11.5**	235645	752	289	5244.8	13741.6					
2	**200**	**11.5**	234835	747	289	5262.0	13694.3					
			4.5	3.20	3.2	**5.25E+03**	**1.37E+04**	**5.25E+04**	**1.37E+05**	**5.25E+05**	**1.37E+06**	
Pos 1	**151.2**	**28.0**	151773	824	288	3081.7	8881.6					
3	**151.2**	**28.0**	151410	824	289	3074.3	8829.3					
			4.5	3.20	3.2	**3.08E+03**	**8.86E+03**	**3.08E+04**	**8.86E+04**	**3.08E+05**	**8.86E+05**	
Pos 1	**101.4**	**41.4**	90201	1015	291	1485.7	5223.3					
4	**101.4**	**41.4**	88679	1008	289	1470.8	5171.1					
			4.5	3.20	3.2	**1.48E+03**	**5.20E+03**	**1.48E+04**	**5.20E+04**	**1.48E+05**	**5.20E+05**	
Pos 1	**75.3**	**47.0**	62202	1223	291	849.8	3601.9					
5	**75.3**	**47.0**	61877	1212	288	853.1	3620.8					
			4.5	3.20	3.2	**8.51E+02**	**3.61E+03**	**8.51E+03**	**3.61E+04**	**8.51E+04**	**3.61E+05**	
Pos 1	**50.9**	**50.9**	46004	1536	292	500.2	2654.6					
5	**50.9**	**50.9**	45969	1536	291	499.8	2661.8					
			4.5	3.20	3.2	**5.00E+02**	**2.66E+03**	**5.00E+03**	**2.66E+04**	**5.00E+04**	**2.66E+05**	
Pos 1	**23.5**	**54.0**	20311	2829	286	119.8	1196.8					
5	**23.5**	**54.0**	19743	2885	287	114.2	1159.2					
			4.5	3.20	3.2	**1.17E+02**	**1.18E+03**	**1.17E+03**	**1.18E+04**	**1.17E+04**	**1.18E+05**	

Figure 5: Calibration results - input energy 230 MeV proton

6 STATEMENT OF WORK - REQUIREMENTS

The Statement of Work (SOW) requirements were defined in AD-1 and AD-2. Here follows the bolded parts:

- ✓ Perform heavy ion, proton and total ionization dose tests on an A3PE3000L device.
- ✓ Evaluate the sensitivities of SEL, SEU, SET, SEFI and SEGR.
- ✓ Check configuration flash after each irradiation steps and additional run should be performed while the device is in configuration process.
- ✓ Perform tests at room temperature. Further tests performed at 80 °C to evaluate the parts to the SEL sensitivity while power supplies are raised to a higher level than the nominal one.
- ✓ Use static 0, static 1, checker board and checker board complemented patterns.
- ✓ Shift registers clock frequency set to 2, 50, 100 and 200 MHz.
- ✓ Perform tests in dynamic condition.
- ✓ All errors should be detected, time stamped, recorded and reported with the relevant information like word address, expected value, word in error, error signature, etc.

To do such characterization, the project included the design of 2 Test Vehicles (TVs).

6.1 TEST VEHICLE DESIGN REQUIREMENTS

Two test vehicle designs were required. The aim of first test vehicle was to characterize the different elements of the FPGA while the second test vehicle was to implement SEE mitigation. RD-1, RD-2 and RD-3 were applicable.

The first test vehicle was to be made of shift register chains with or without layers of combinational logic (inverters) between the flip-flops as shown in Figure 6 and the combinational logic made of 8 levels of inverters [or less depending on the timing simulation results]. It was also requested, each four register in some chains, a separate fan-out tree with 8 inverters [or less depending on the timing simulation results] in enable or reset paths.

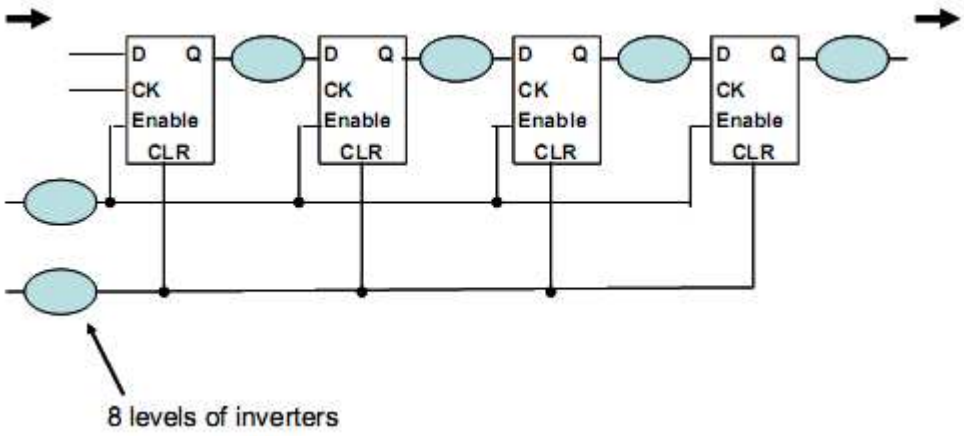


Figure 6: Basic shift register block

In addition to standard 3.3 V LVCMOS I/Os, some chains were required to use LVDS differential I/Os and DDR I/Os. Finally, some chains were requested to be clocked with a 200 MHz clock generated from the FPGA internal PLL: all other channels having a common external clock inputs. Table 4 summarizes the characteristics of the different shift registers of the TV1. Each channel made of 1024 registers. The four last registers outputs of each channel were requested to be accessible externally: this allowing the test of the channel at a frequency four times slower than the channel clock frequency.

In addition it was required in the test vehicle a specific interface design to test the FPGA internal SRAM (512x9) (read and write), and flash ROM (128x8) (read only).

The second test vehicle was required to be made of shift registers with or without layers of combinational logic (inverters) between the flip-flops as the first test vehicle, plus implementing SEU and SET mitigation. Only LVCMOS I/Os standard was to be used in this design.

Chain #	Clock	Logic between registers	Register enable fanout	Register CLR fanout	I/O type
1	External	no	no	no	LVCMOS 3.3V
2	External	no	yes	no	LVCMOS 3.3V
3	External	no	no	yes	LVCMOS 3.3V
4	External	yes	no	no	LVCMOS 3.3V
5	External	no	no	no	DDR 3.3V
6	External	no	no	no	DDR 3.3V
7	External	no	no	no	DDR 3.3V
8	External	no	no	no	DDR 3.3V
9	External	no	no	no	LVDS 2.5V
10	External	no	no	no	LVDS 2.5V
11	Internal, PLL 200 MHz	no	no	no	LVCMOS 3.3V
12	Internal, PLL 200 MHz	no	no	no	LVCMOS 3.3V
13	Internal, PLL 200 MHz	no	no	no	LVCMOS 3.3V
14	Internal, PLL 200 MHz	no	no	no	LVCMOS 3.3V

Table 4: TV1 - shift registers characteristics

7 TEST VEHICLE DESIGNS

The first phase of the project was to design two Test Vehicles (TVs). The design phase included:

- ✓ Specification
- ✓ Description
- ✓ Simulation
- ✓ Test and validation

The result of the Test Vehicle designs phase is reported in AD-5.

The first TV was used to characterize the sensitivity of the device while the second was used to characterize the SEE mitigation techniques. As a consequence the TV1 implemented:

- ✓ Shift Registers (SR) with different input/output configurations
- ✓ Clock Conditioning Circuit (CCC) with Phase-locked Loop (PLL)
- ✓ SRAM memory
- ✓ UFROM memory

While the second TV was fully used to implements SEE mitigation techniques on shift registers.

All shift registers of both TVs were made of 1024 registers each and, if not specified otherwise, used common:

- ✓ Reset (clear)
- ✓ Clock
- ✓ Enable
- ✓ Input data

The common clock, enable and reset signals were routed on global network resources of the device. All used sequential logic core (registers) were implemented by D type flip-flop with enable and clear active high. The place and route processes of the design were left at the charge of the manufacturer's design software (not placed/routed by hand).

7.1 TV1 - SHIFT REGISTERS

The Table 5 summarizes the specifications of shift register channels implemented on the TV1.

Shift Register	Clock	I/O Type	Particularity
1	External	3.3 V LVCMOS	Reference
2	External	3.3 V LVCMOS	Global Enable C-cell
3	External	3.3 V LVCMOS	Global Reset C-cell
4	External	3.3 V LVCMOS	C-cell
5	External	3.3 V LVCMOS - DDR	DDR I/O
6	External	3.3 V LVCMOS - DDR	DDR I/O
7	External	3.3 V LVCMOS - DDR	DDR I/O
8	External	3.3 V LVCMOS - DDR	DDR I/O
9	External	2.5 V LVDS	LVDS I/O
10	External	2.5 V LVDS	LVDS I/O
11	CCC/PLL	3.3 V LVCMOS	CCC/PLL Clock
12	CCC/PLL	3.3 V LVCMOS	CCC/PLL Clock
13	CCC/PLL	3.3 V LVCMOS	CCC/PLL Clock
14	CCC/PLL	3.3 V LVCMOS	CCC/PLL Clock

Table 5: TV1 - Shift Register specifications

The first SR is the reference. It is a standard SR as it can be seen on the Figure 7.

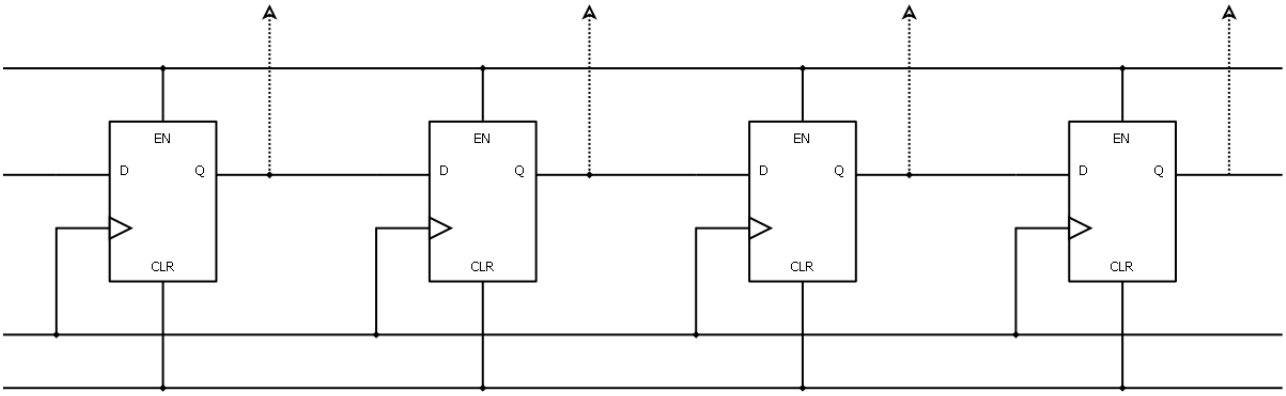


Figure 7: TV1 - SR1 - Schematic

On the previous shift register schematic as well as for the following shift register schematics, all dotted outputs of the D flip-flops are applicable for the four last registers outputs of all shift registers because they are accessible externally.

The second shift register is identical to the reference adding combinational cells (C-Cell) on the global enable signal. Each four register stages have a separate level of 4 inverters computing a “local enable signal” from the global one. This principle is detailed on the Figure 8. To increase the maximum working frequency of this channel, the number of inverters on the enable signal was decrease from 4 to 2 in October 2010 (after the first RADEF campaign) to conform to the decision taken during the phone review meeting of October 22^{sd} 2010.

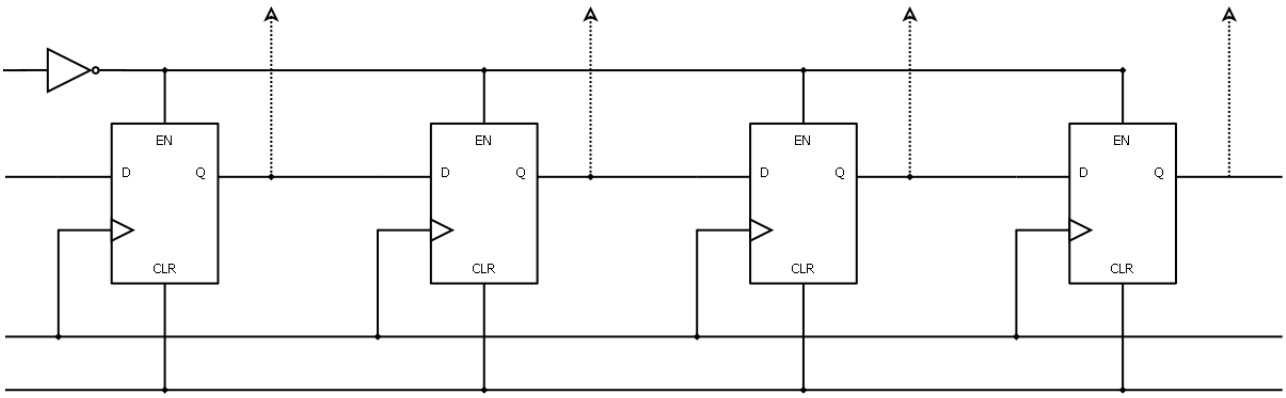


Figure 8: TV1 - SR2 - Schematic

The third shift register is identical to the reference adding combinational cells (C-Cell) on the global reset signal. Each four register stages have a separate level of 4 inverters computing a “local reset signal” from the global one. This principle is detailed on the Figure 9. The number of inverters on the reset signal was decrease from 4 to 2 in October 2010 (after the first RADEF campaign) to conform to the decision taken during the phone review meeting of October 22^{sd} 2010.

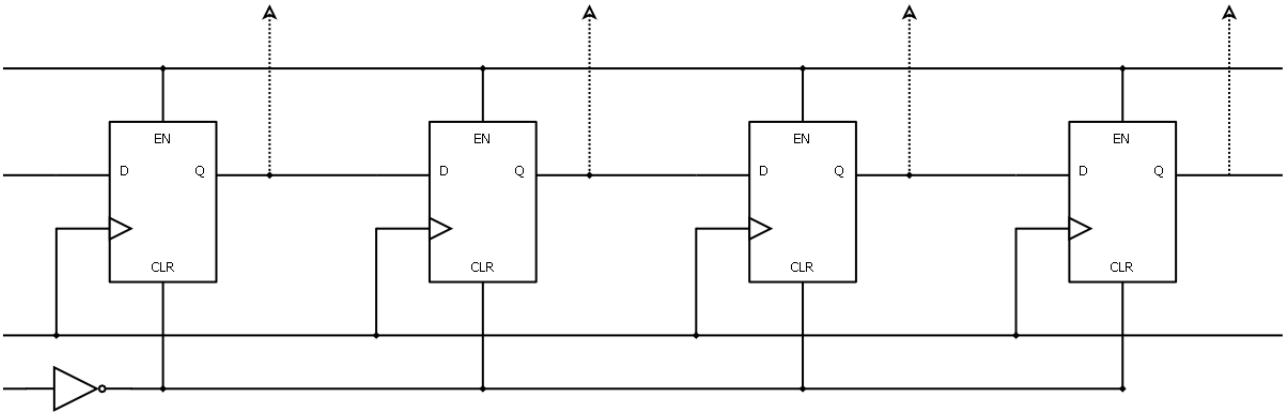


Figure 9: TV1 - SR3 - Schematic

The fourth shift register is identical to the reference adding combinational cells (C-Cell) between each register. Each combinational path has a separate level of 4 inverters. This principle is detailed on the Figure 10. To increase the maximum working frequency of this channel, the number of inverters between each register was decrease from 4 to 2 in October 2010 (after the first RADEF campaign) to conform to the decision taken during the phone review meeting of October 22^{sd} 2010.

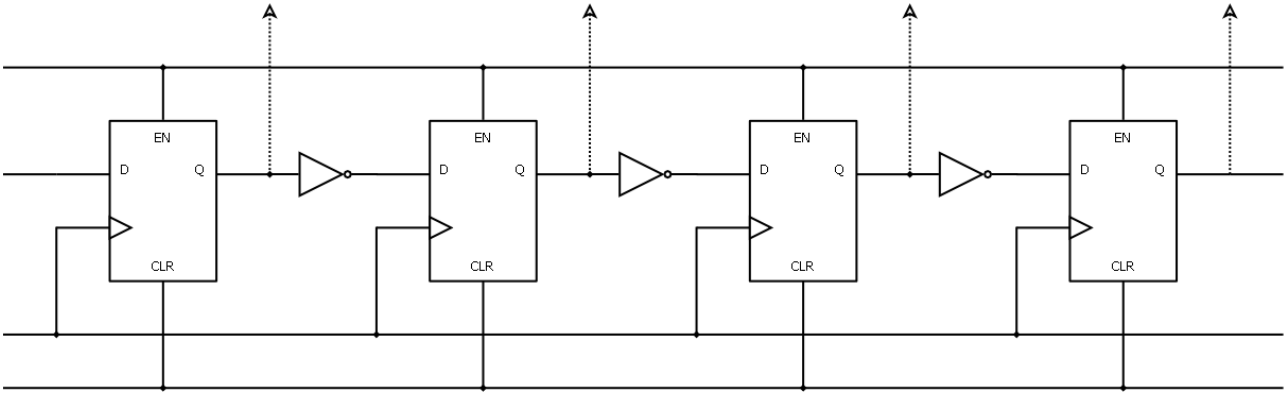


Figure 10: TV1 - SR4 - Schematic

The shift registers from the fifth to the eighth are identical to the reference. Using 2 shift registers mounted as pair, both pairs include a 3.3 V LVCMOS Double Data Rate (DDR) input standard to drive the shift registers inputs data and also use a 3.3 V LVCMOS DDR standard to drive 2 data outputs each. That principle is detailed on the Figure 11.

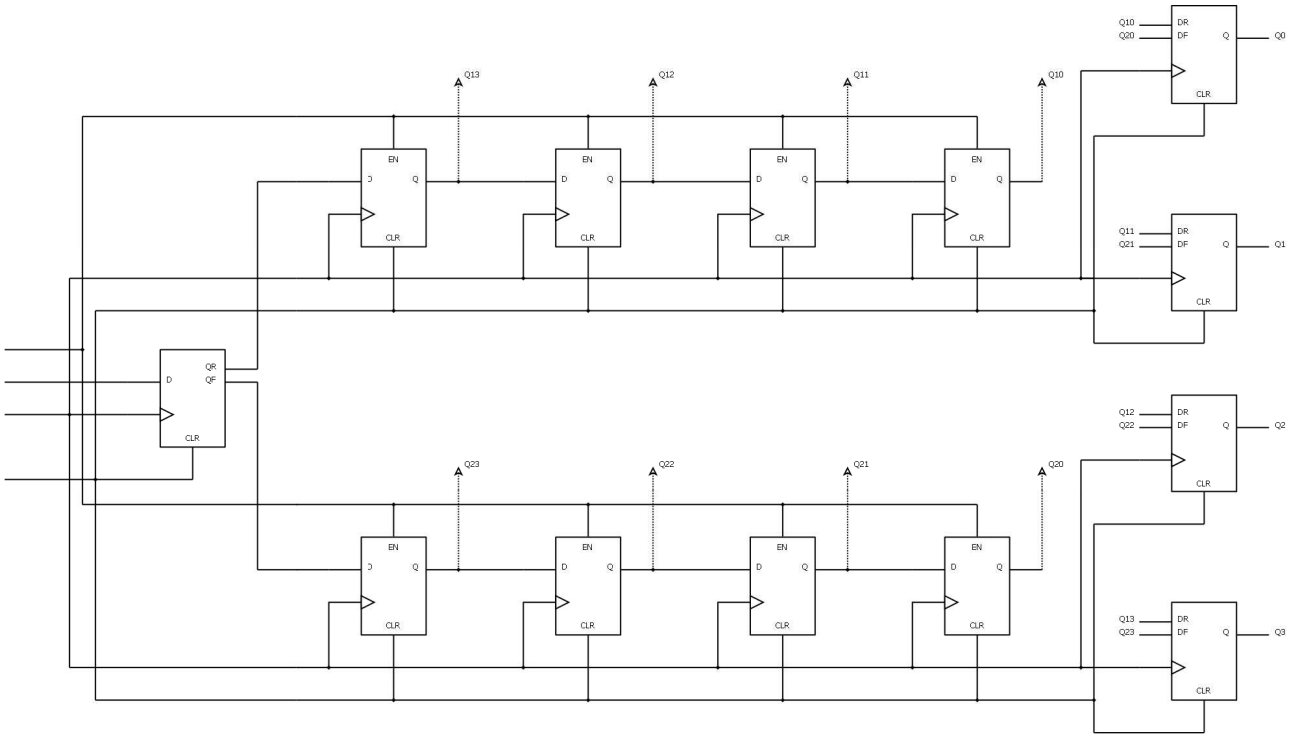


Figure 11: TV1 - SR5, 6, 7 and 8 - Schematic

The ninth and tenth shift registers are identical to the SR1. However those channels use a 2.5 V LVDS standard as input and output standard.

The 4 shift registers from the eleventh to the fourteenth are identical to the SR1. However the clock is generated by the internal CCC with a PLL module from a global input clock.

Those 14 shift registers used around 30% of the FPGA's logic tiles and 71 inputs/outputs pads.

With the decrease number of inverters (2 instead of 4), the maximum working frequency of the shift registers is 200 MHz.

7.2 TV2 - SHIFT REGISTERS

The Table 6 summarizes the specifications of shift registers implemented on the TV2. 6 Shift registers use 5 different SEU and SET mitigation methods.

Shift Register	Sequential Cell Triplication	I/O Block Triplication	SET Filtering	Combinational Cell Duplication	Combinational Cell Triplication
1	✓				
2	✓	✓			
3			✓		
4	✓	✓	✓		
5	✓	✓		✓	
6	✓	✓			✓

Table 6: TV2 - Shift Register specifications

The first SR of the TV2 is identical to the TV1 SR1 (the reference). However it includes sequential cell (register) triplication and a voter at the input of each register stage. This SR uses the Triple Modular Redundancy (TMR) of the sequential logic as SEU mitigation method. Only 1 data input drives the shift register while 3 data output. The same global signals (clock, reset and enable) routed on the global network are shared between the 3 lines. That principle is detailed on the Figure 12.

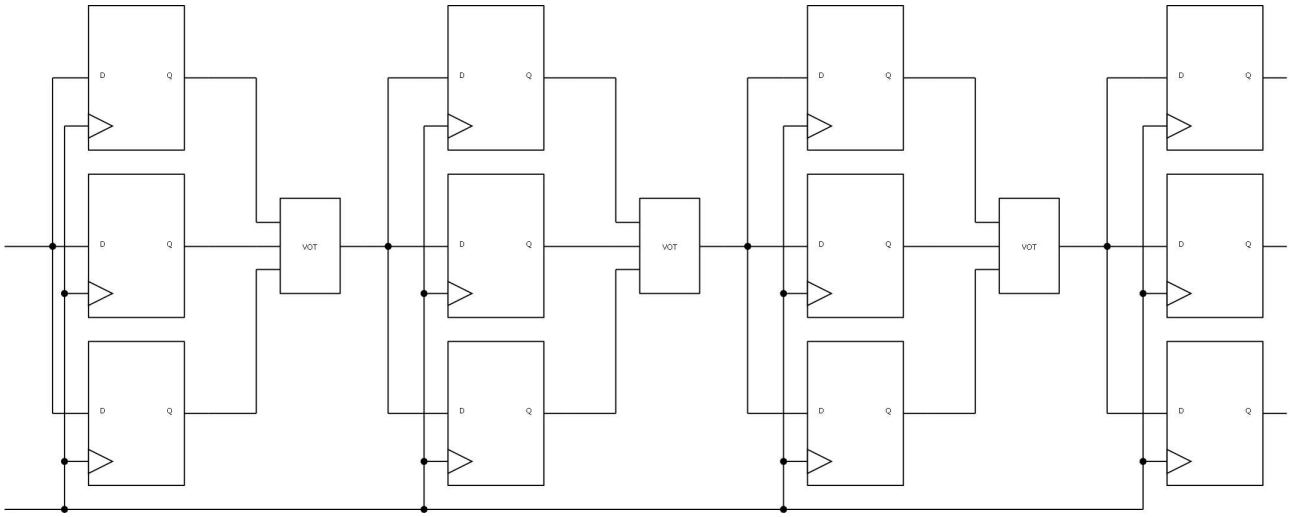


Figure 12: TV2 - SR1 - Schematic

To ease the understanding of the schematic, on the previous figure as well as for the following ones, the previous dotted lines for the 4 data outputs of the last 4 register stages as well as the global enable and clear signals have not been drawn but still remain applicable.

The second shift register is similar to the SR1 (of the TV2) using the triplication of the sequential logic as SEU mitigation, but also includes triplication of the input and output by using 3 different I/O banks for each input and output as SEU and SET mitigation. Each D flip-flop input is generated using a separate voter and so 3 voters are used at each register stage. That principle is detailed on the Figure 13.

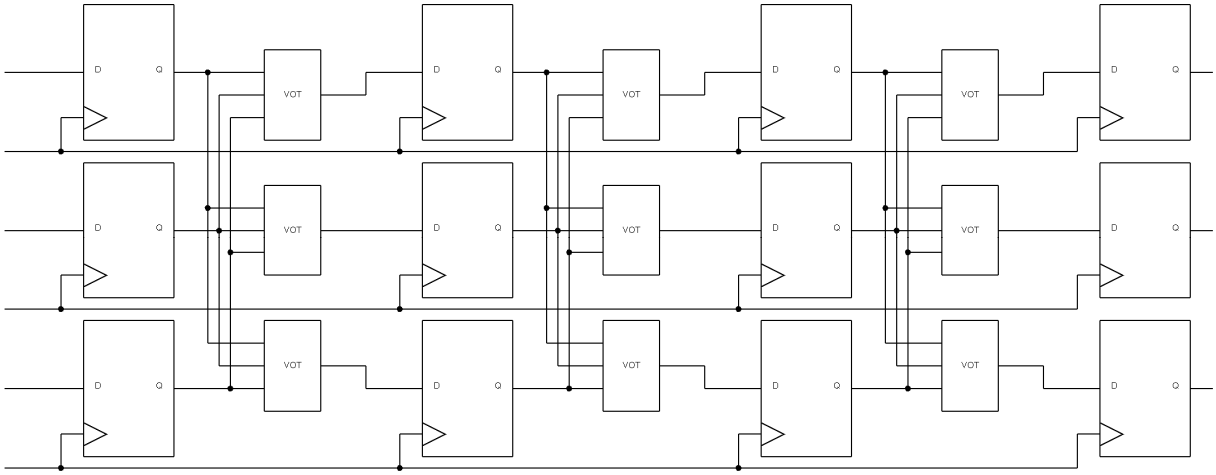


Figure 13: TV2 - SR2 - Schematic

The third shift register is identical to the SR1 of the TV1 (the reference) plus it includes SET filtering method at the combinational logic output as SET mitigation. This method consists of voting, with a guard gate, the current state of the output of the combinational logic with its own state delayed (here with a delay around 2 ns). That principle is detailed on the Figure 14.

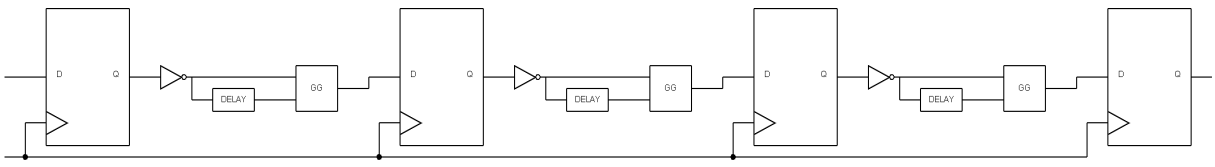


Figure 14: TV2 - SR3 - Schematic

The fourth shift register is identical to the TV2 SR2 including sequential logic and I/O bank triplication. In addition it includes an SET filtering mitigation with a delay around 3 ns. This shift register principle is detailed on the Figure 15.

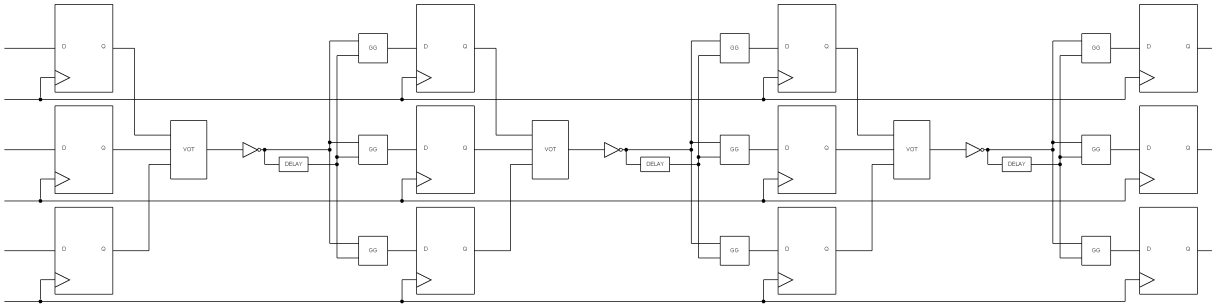


Figure 15: TV2 - SR4 - Schematic

The fifth shift register includes sequential logic triplication, IO bank triplication and combinational logic duplication as SEU and SET mitigation. That principle is detailed on the Figure 16.

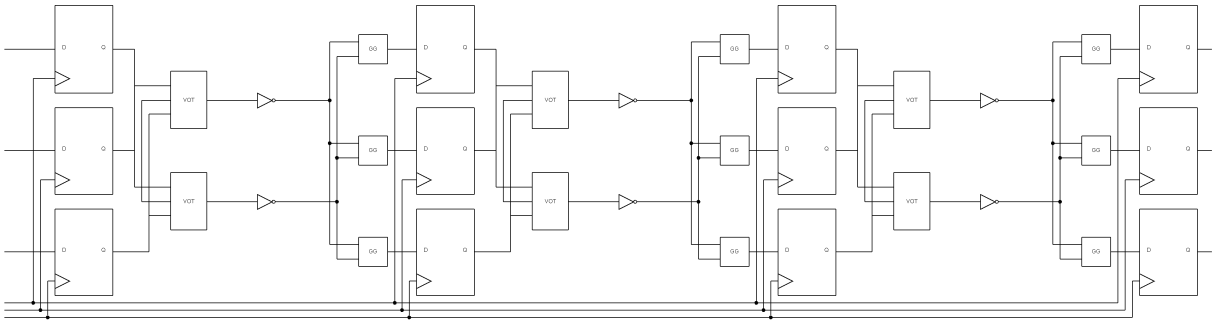


Figure 16: TV2 - SR5 - Schematic

The sixth shift register implements the full triplication (full TMR) as SEE mitigation. That principle is detailed on the Figure 17.

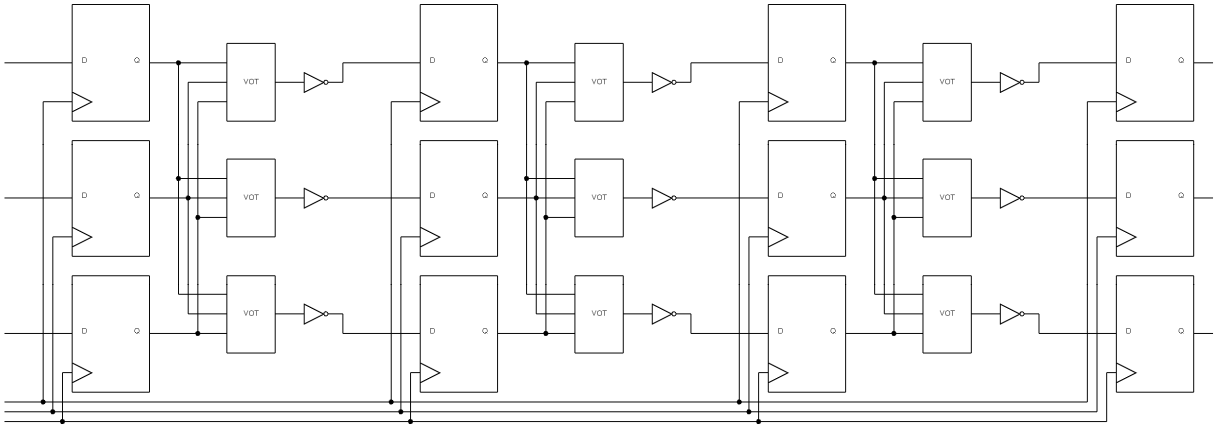


Figure 17: TV2 - SR6 - Schematic

With 2 inverters as SET generation line (combinational path) between each register cell, 1 logic tile to generate a voter as well as a guard gate (with a combinational loop) and specified delay lines this design uses around 78% of the logic tiles and 76 inputs/outputs.

Time penalties induced by the combinational paths, voters, delay lines, guard gates and additional routing delays limit the maximum working frequency of the shift registers to 50 MHz (70 MHz for some channels).

7.3 SRAM

100 % of the device embedded SRAM is used on the TV1. The first half made of 56 blocks of 512 words of 9 bits is located on the north side of the die while the other half is located on the south. To access all memory blocks, all blocks are cascaded and the output is multiplexed. The SRAM is implemented in synchronous mode for both read/write operations. The SRAM functional block uses dedicated clock routed on one global line, control signals, address and data buses and is so entirely independent of the remain of the design.

The Flash Freeze type 1 is also implemented on the design.

7.4 UFROM

100 % of the device embedded UFROM was used on the TV1. The UFROM block was made of 128 words of 8 bits configured with a checkerboard interleaved with its complement. The UFROM functional block used dedicated clock, address and data buses and was so entirely independent of the remain of the design.

7.5 CLOCK CONDITIONING CIRCUIT / PHASE-LOOKED LOOP

The TV1 included one CCC with PLL configured in a static mode set on 200 MHz. The input clock signal was the global input clock while the PLL output was routed on one global line. The PLL output was used to clock 4 shift registers of the TV1. The PLL lock and power-down signals were output and input of the design.

The TV2 design did not implemented the CCC with PLL blocks.

7.6 TV RESOURCES USAGE

The Table 7 summarizes the resources usage of both TVs.

	Total Number	Total Number on TV1	Total number on TV2
Core tiles	75264	22758 (30%)	58368 (78%)
Core tiles used as combinational cell	-	8415 (37%)	41984 (72%)
Core tiles used as sequential cell	-	14343 (63%)	16384 (28%)
I/O	147	139 (95%)	76 (52%)
I/O used as differential	65	13 (20%)	0 (0%)
Chip Global	6	6 (100%)	6 (100%)
Quadrant Global	12	0 (0%)	0 (0%)
Local Clock	-	0	3
PLL	2	1 (50%)	0 (0%)
RAM (Block)	112	112 (100%)	0 (0%)
Low Static ICC	1	0 (0%)	0 (0%)
User Flash ROM (Block)	1	1 (100%)	0 (0%)
User JTAG	1	0 (0%)	0 (0%)
Flash Freeze	1	Type 1	No

Table 7: TVs - Resources usage

8 TEST SET-UP AND CONDITIONS

The test system is based on a Virtex-5 FPGA (XILINX). It has 168 I/O including 44 LVDS channels. The set of test board includes a DUT power supplies controller which manages the DUT power supplies up to 24 independent channels. A temperature control and regulation system is added to heat the DUT whenever needed. Ambient temperature is used otherwise. The communication between the under vacuum test system and the computer running the controlling GUI software is made using a 100 MBit/s Ethernet link. The Figure 18 displays the principle of the test system used for heavy ion tests.

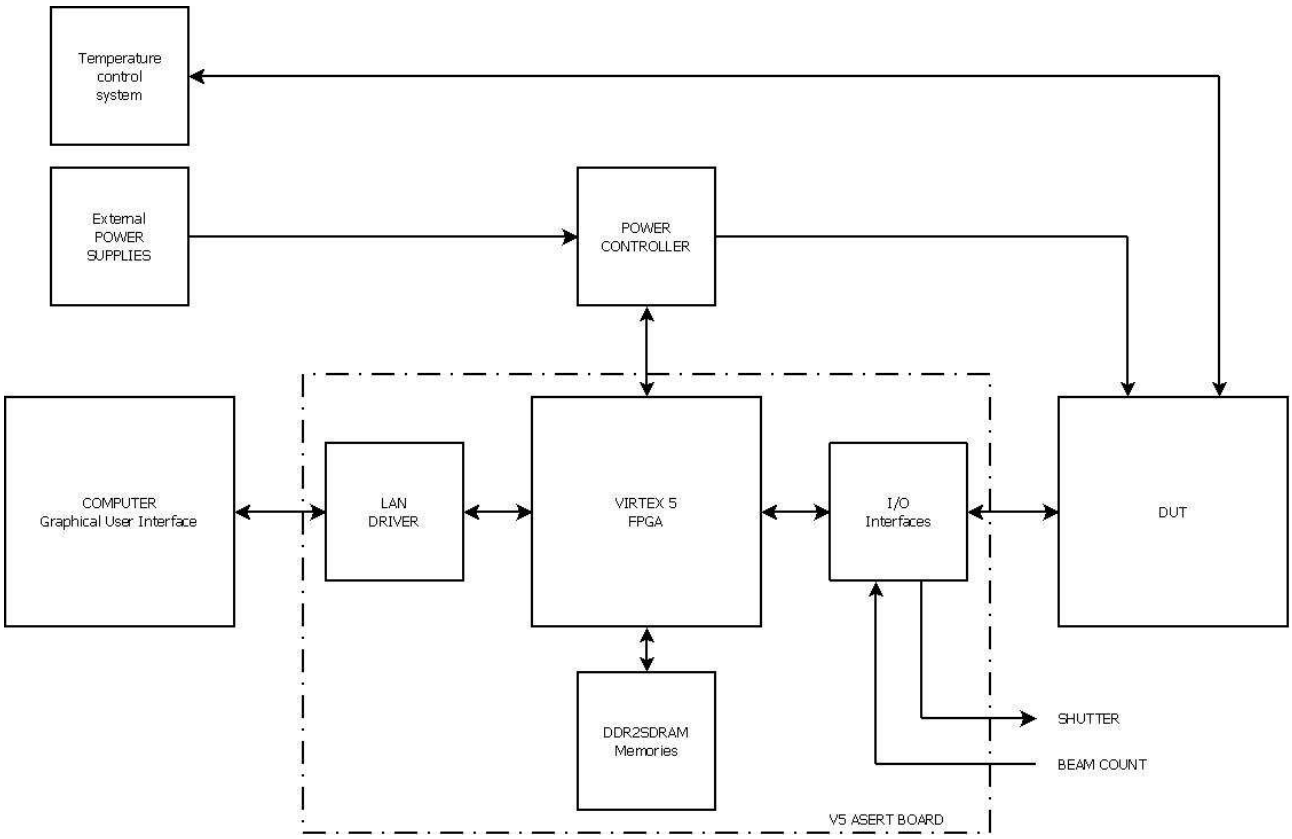
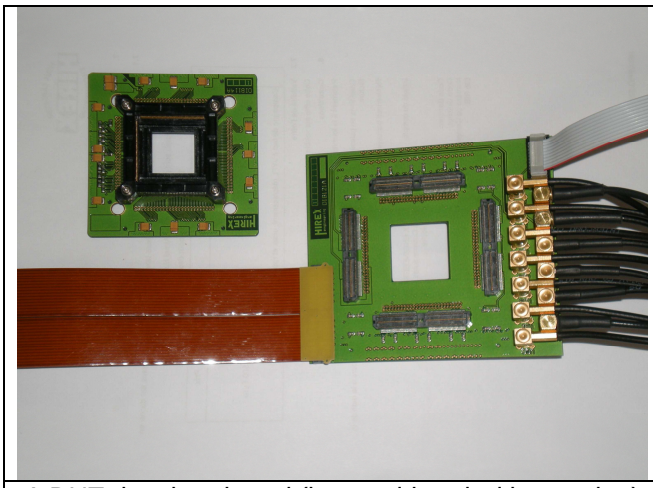
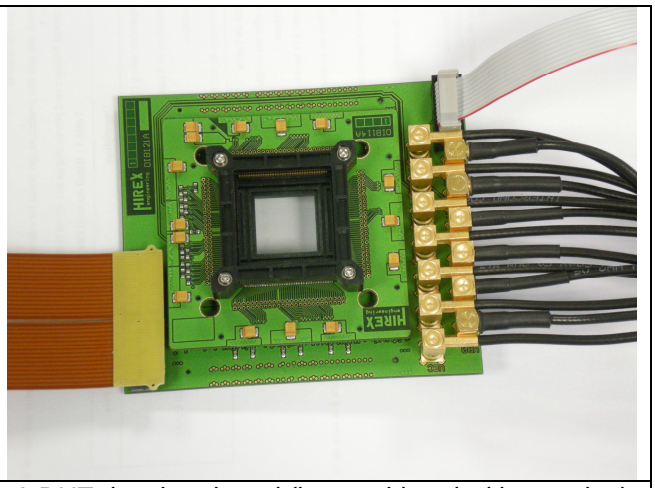


Figure 18: Heavy Ion test set-up

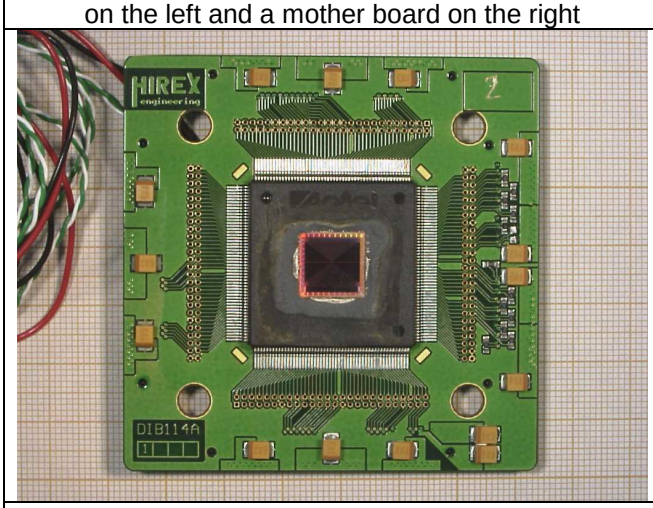
The DUT side of the tester is composed of a set of 2 boards as shown on the Figure 19. A mother board connecting directly on the tester implementing voltage level translators, power supply connectors, LVDS connectors and the ISP connector. It received on top the connection system to plug the daughter board. The daughter board received a sample (or socket) directly soldered in the middle as well as decoupling capacitor and terminal resistors. All samples were soldered on a daughter board. Two daughter boards received a socket instead of a device. An access area was realized below the DUT footprint on both boards to allow the heating system and temperature sensor to take place in close contact to the bottom of device‘s package. Both test vehicles used the same hardware (also the same samples).



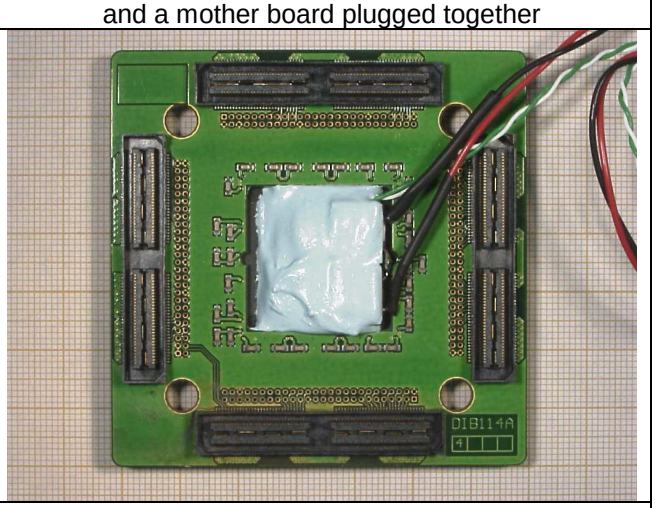
A DUT daughter board (here soldered with a socket) on the left and a mother board on the right



A DUT daughter board (here soldered with a socket) and a mother board plugged together



A DUT daughter board (top) - SN 2



A DUT daughter board (bottom) with heating system and temperature sensor mounted

Figure 19: DUT board set

8.1 Power supply

The following 13 channels were defined to monitor the DUT power supplies. They were independently monitored using for each channel a set of selectable parameters (start and stop delay, current threshold, inhibit time…) and were globally controlled.

- ✓ 1 core supply
- ✓ 8 bank supplies
- ✓ 2 PLL supplies
- ✓ 1 charge pump supply
- ✓ 1 JTAG supply

The Table 8 details the voltage range admissible for each channel previously defined.

		FUNCTIONING			PROGRAMMING		
NAME	**DESCRIPTION**	**Min (V)**	**Nominal (V)**	**Max (V)**	**Min (V)**	**Nominal (V)**	**Max (V)**
Vcc	Core supply voltage	1.35	1.5	1.65	1.35	1.5	1.65
Vccbx	I/O Bank Supply voltage	2.25 | 3.0	2.5 | 3.3	2.75 | 3.6	2.25 | 3.0	2.5 | 3.3	2.75 | 3.6
Vccplx	PLL supply voltage	1.35	1.5	1.65	1.35	1.5	1.65
Vjtag	JTAG supply voltage	0	0	0	3	3.3	3.6
Vpump	Charge Pump supply voltage	0	0	0	3	3.3	3.6

Table 8: Power supplies conditions

The device belonging to the ProASIC3L family (L meaning low power) is working with the core voltage (V_{cc}) down to 1.2 Volts. However the device was not properly functioning when increasing the working frequency. For this reason the core voltage was kept at 1.5 V.

Unused power supplies (like JTAG and charge pump power supplies while the device is not in configuration mode), and unused I/Os were kept at the reference voltage (0 V).

The Table 9 summarizes the applied test conditions on the current thresholds of the DUT power supplies.

Target - Mode	Core current threshold (mA)	Banks current thresholds (mA)	PLL current thresholds (mA)	JTAG and PUMP current thresholds (mA)
TV1 - Dynamic	950	600	100	NA
TV1 - Static	950	250	100	NA
TV1 - Flash Freeze	950	250	100	NA
TV2 - Dynamic	950	600	NA	NA
Programming	950	600	100	100

Table 9: Power supplies - Current thresholds

8.2 Shift registers

The basic shift registers test sequence used was:

Initialization
Loop
  Exposition
  Check & Fill
End loop

The initialization step was needed to initialize the shift registers with a selected pattern. The check & fill step was made to read and verify the content of all channels while they were filled with another (or the same) pattern.

The used patterns were the standard checker board and complemented checker board, static 0 and static 1. The shift register clock frequency (selectable from the GUI) was set to 2, 50, 100, 150 and 200 MHz for the first TV while it was set to 2, 37.5, 50 and 70 MHz for the second TV.

Dynamic tests were performed. One additional run was performed in a static mode using the Hirex shutter system.

SEFI and SEU are treated on a post-treatment process. This classification process allowed the detection of SEFI, SBU and MBU.

8.3 SRAM

The TV1 uses 100 % of the device's embedded SRAM. It was made of 112 blocks of 512 words of 9 bits. To access all memory blocks, all blocks were cascaded and the outputs were multiplexed.

The SRAM fill and the SRAM check algorithms (Figure 20 and Figure 21) were both designed to highlight different types of errors (write error, read error, upset, stuck bits…) of basic memory cells. Each memory cell on a block can be sequentially or interleaved manner tested with different combinations of both algorithms.

To be tested the selected memory block has first to be filled using the fill algorithm. Then the same memory block can be:

- ✓ Checked entirely then filled again entirely making the test sequential.
- ✓ Checked and filled memory address per memory address making the test interleaved.

The SRAM fill and check algorithms report each 4 types of error here listed on the Table 10:

Error type	FILL algorithm	CHECK algorithm	Error source
No-error	No error from 1 write / read	No error from 1 read	NA
Type 1	1 error from 2 write / read	1 error from 2 reads	Write / Read error
Type 2	NA	2 errors from 3 reads / 1 write	Upset
Type 3	2 errors from 4 write / read	3 errors from 4 reads / 2 writes	Snap back
Type 4	3 errors from 4 write / read	4 errors from 4 reads / 2 writes	Stuck bit / Big problem

Table 10: SRAM - Error types definitions

The used patterns were checker board and complemented checker board, static 0 and static 1. The SRAM clock frequency (selectable from the GUI) was set to 20 MHz.

Mostly dynamic tests were performed. Few additional runs were performed in a static mode using the Hirex shutter system and one additional run was performed in the flash freeze mode.

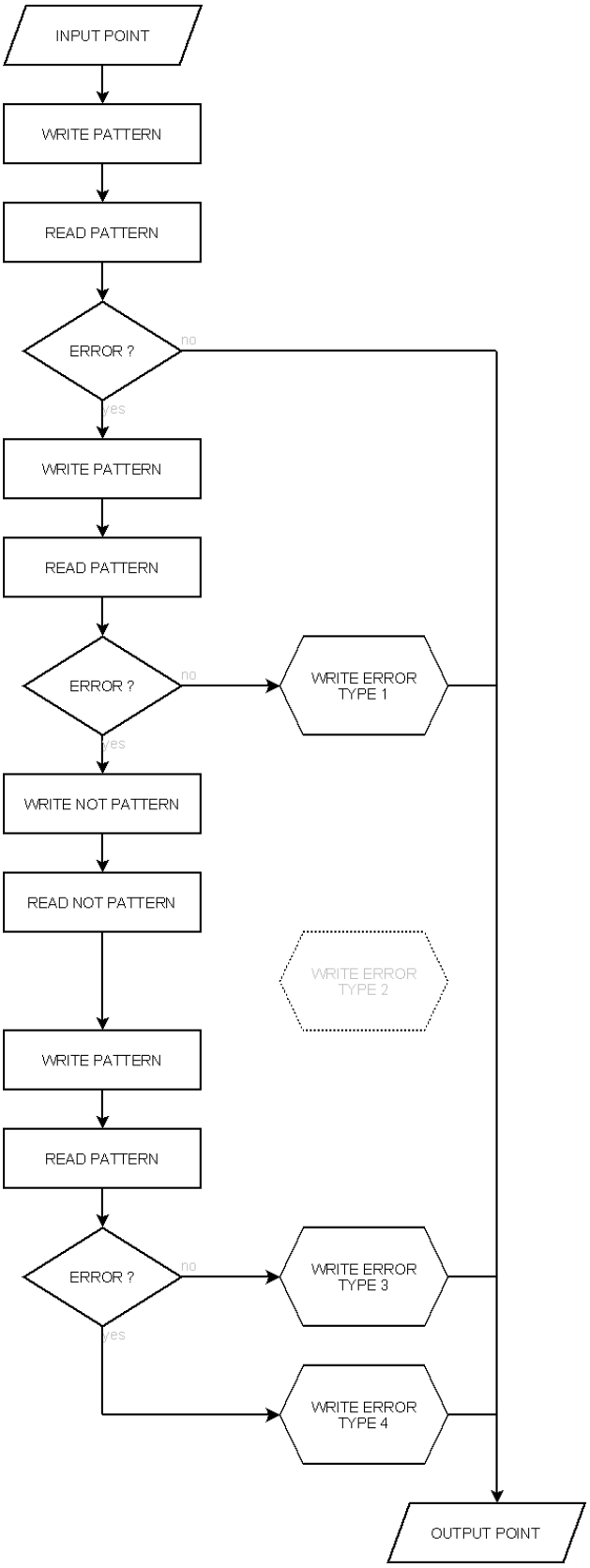


Figure 20: SRAM Fill algorithm

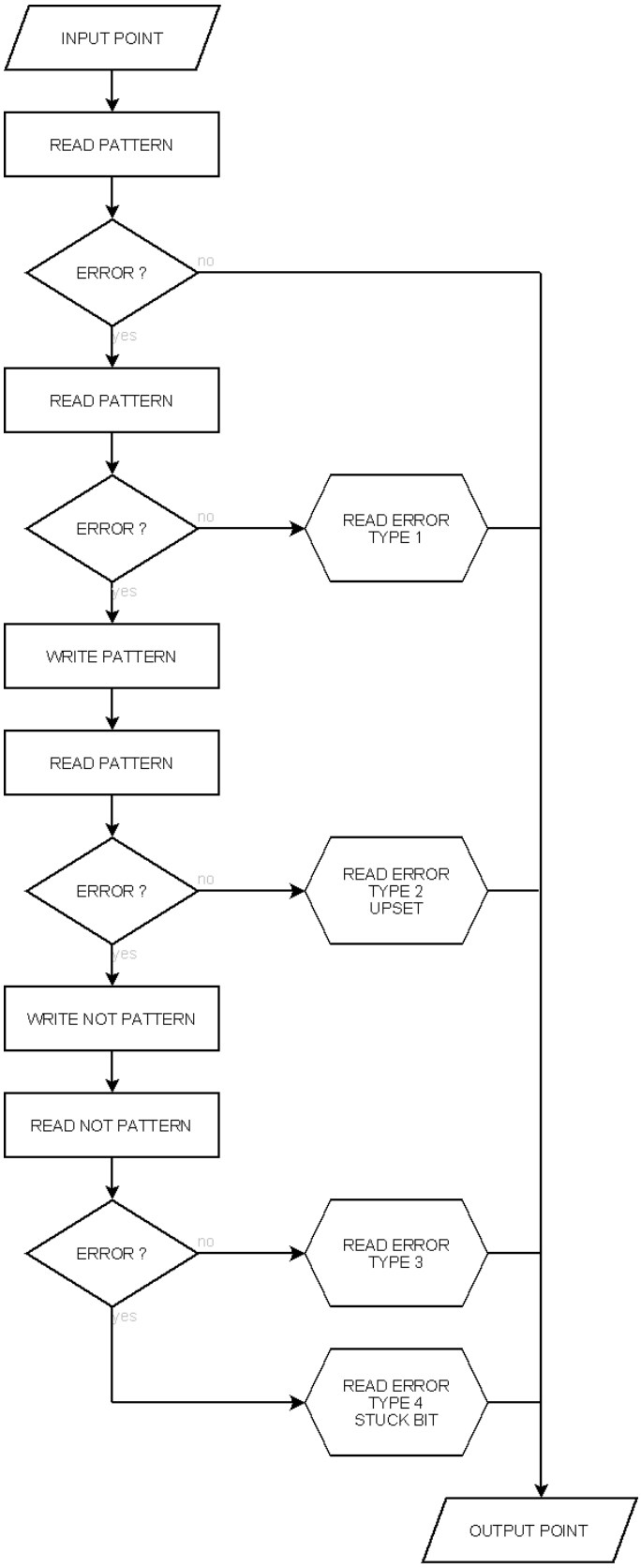


Figure 21: SRAM Check algorithm

8.4 UFROM

The TV1 uses 100 % of the device's embedded UFROM made of 128 words of 8 bits.

The UFROM algorithm detailed on the Figure 22 is based on 3 reads of each memory address sequentially tested. The memory address is increased to the next when the state of the current address is stated. The result of the memory content is estimated as the majority of the read results. By this way, 3 error types are defined as detailed on the Table 11:

Error type	Algorithm steps	Error source
No error	0 error from 2 reads	NA
Type 1	1 error from 3 reads	Read error
Type 2	2 errors from 3 reads	Read error or Upset
Type 3	2 errors from 2 reads	Upset

Table 11: UFROM - Error types definitions

To fasten the test of the memory, the 3rd read is "cancelled" if the 2 previous results are similar.

For example, if 2 successive reads are realized without any error then the 3rd read is cancelled and the "No-error" type is stated (reporting nothing), this increasing the speed of the test. The behavior is similar if 2 successive reads result in error cancelling the 3rd read, stating and reporting the error type 3.

The flash memory content was configured with checker board interleaved with checker board complemented patterns. The UFROM clock frequency (selectable from the GUI) was set to10 MHz.

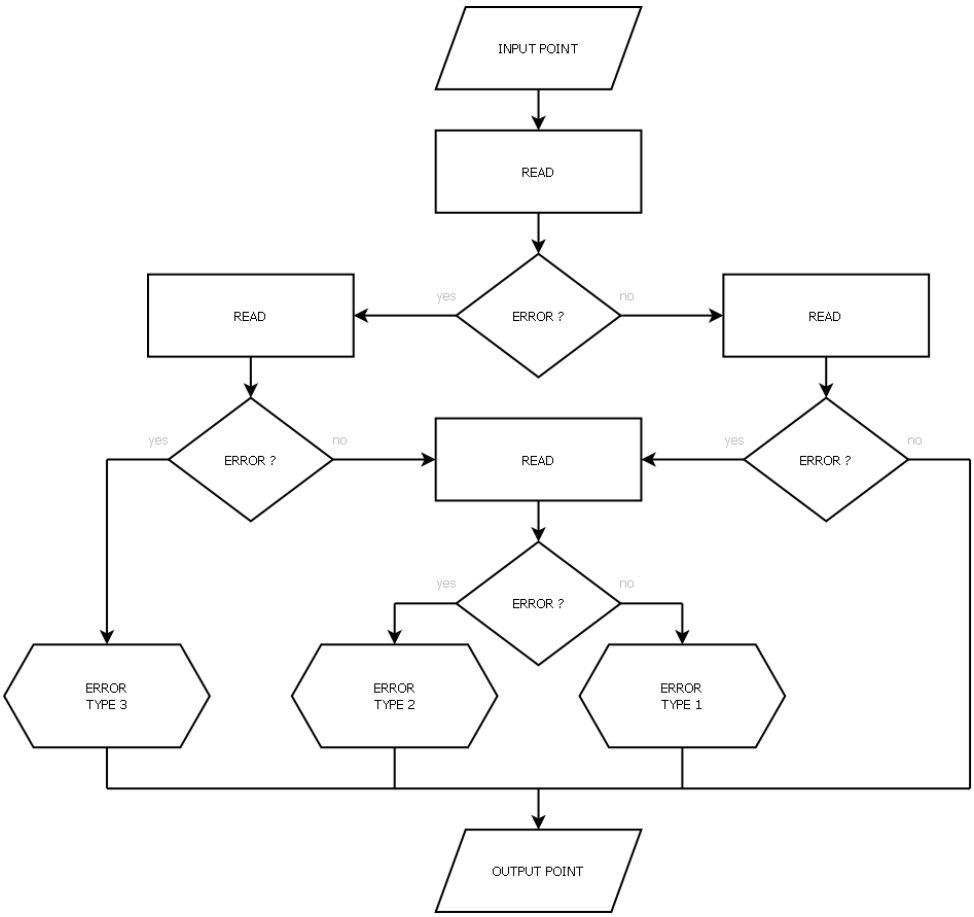


Figure 22: UFROM Check algorithm

8.5 CCC/PLL

On the TV1, one Clock Conditioning Circuit (CCC) with a Phase-Locked Loop (PLL) was configured in a static mode (single frequency) set on 200 MHz.

The SEE sensitivity of the CCC/PLL is evaluated first by interpreting clock error signature on the shift registers clocked by the CCC/PLL output. In the mean time the PLL lock signal is verified and recorded when toggling state.

The CCC/PLL input clock was the common shift register input clock. The PLL was verified functional with an input clock frequency from 200 MHz (the nominal point) and down to lower than 100 MHz. The SEE sensitivity of the PLL was so characterized from 200 MHz down to 100 MHz (200 MHz being the nominal point).

8.6 Configuration Flash, charge pump and ISP

The configuration flash was tested by checking the functionality of the device during and after each exposition. Additional runs were performed while the device was running the configuration process to evaluate the SEE sensitivities of the configuration flash, charge pump and ISP. The standard configuration sequence is:

- ✓ Erase
- ✓ Program
- ✓ Verify

The erase, program and verify processes were run all together and one at a time, exposed to the beam. The result of the entire configuration process was then stated by verifying the:

- ✓ Success of the operation (pass/fail)
- ✓ Design functionality
- ✓ Re-configurability of the device

The configuration process was run with ACTEL specific tools.

9 HEAVY ION - TEST RESULTS

9.1 POWER SUPPLY

No SEL has been observed up to a LET of 55 MeV.cm²/mg ($^{131}Xe^{35+}$), a cumulative fluence of 1E7 p/cm², a temperature up to 125 °C, a bias voltage of 1.65 V for the core voltage and 3.6 V for the input/output voltage.

The run N°159 from June 2010 campaign at RADEF was one test run performed in SEL tests condition. It was performed on the device sample SN 5 configured with the TV1 exposed to Xenon ion, a total fluence of 5E6 p/cm² and a temperature of 125 °C. The chronograms of banks, PLL and core power supplies are plotted on following figures from Figure 23 to Figure 33 where no SEL appears.

It can be seen on those figures 3 plots versus time:

- ✓ The flux of the beam in black color.
- ✓ The voltage of the channel in blue color.
- ✓ The current of the channel in red color.

Remarks:

i. The flux of the RUN 159 shows 2 cuts attended to 2 stops of the beam line.
ii. The second bank current chronogram shows large steps of current. This is due to the very short scale used (because consumption is very light on this bank). So small variations are largely spread into the full scale.
iii. The PLL F was not used on the device but still powered.
iv. The JTAG and charge pump voltage were kept at 0 V while tested in nominal mode (not configuring the device).
v. The device was not tested with SEL test condition in configuration mode. So no SEL test condition was performed with the JTAG and charge pump power supplies on.

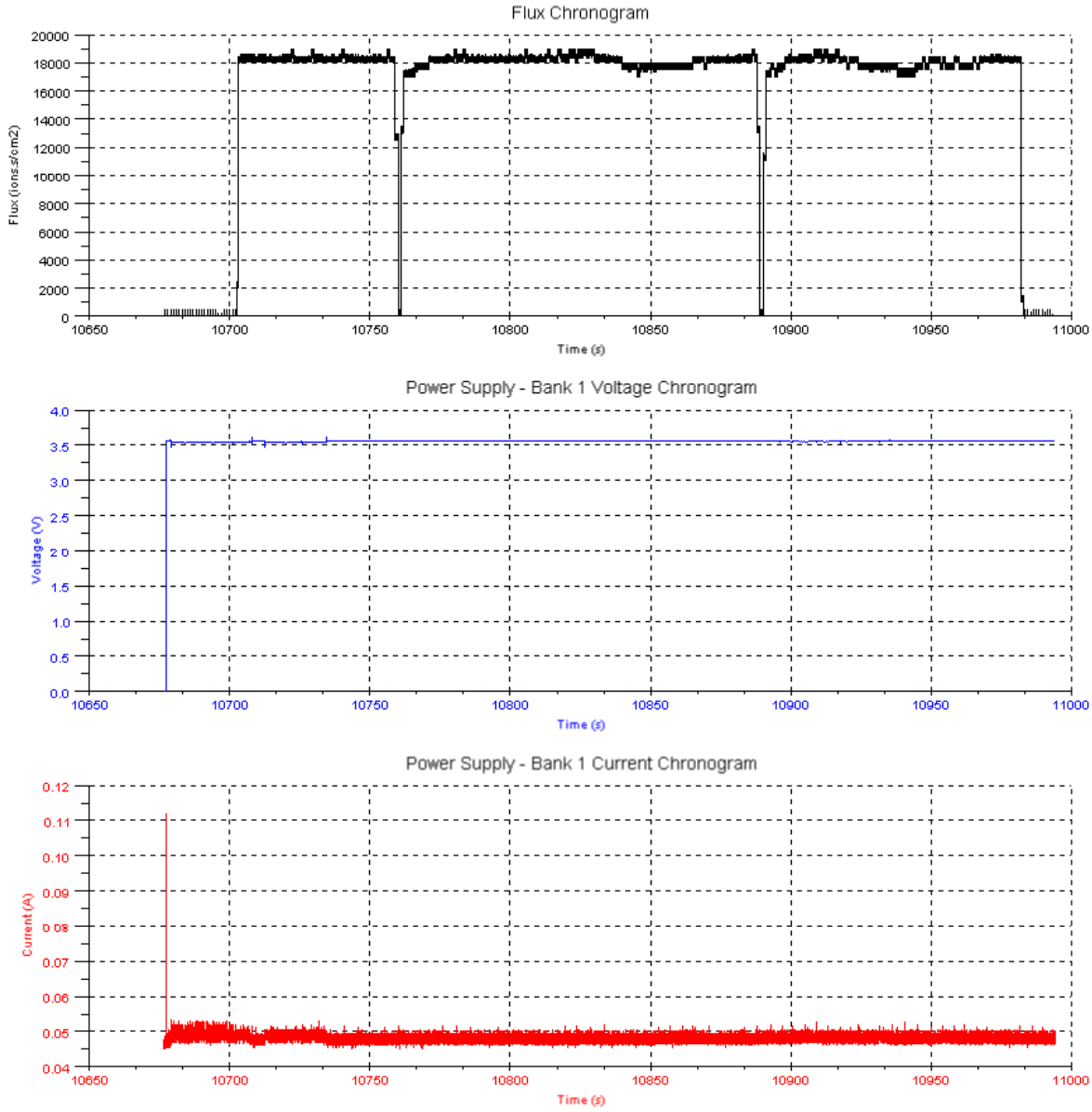


Figure 23: RADEF June 2010 - RUN 159 - Bank 1 power supply

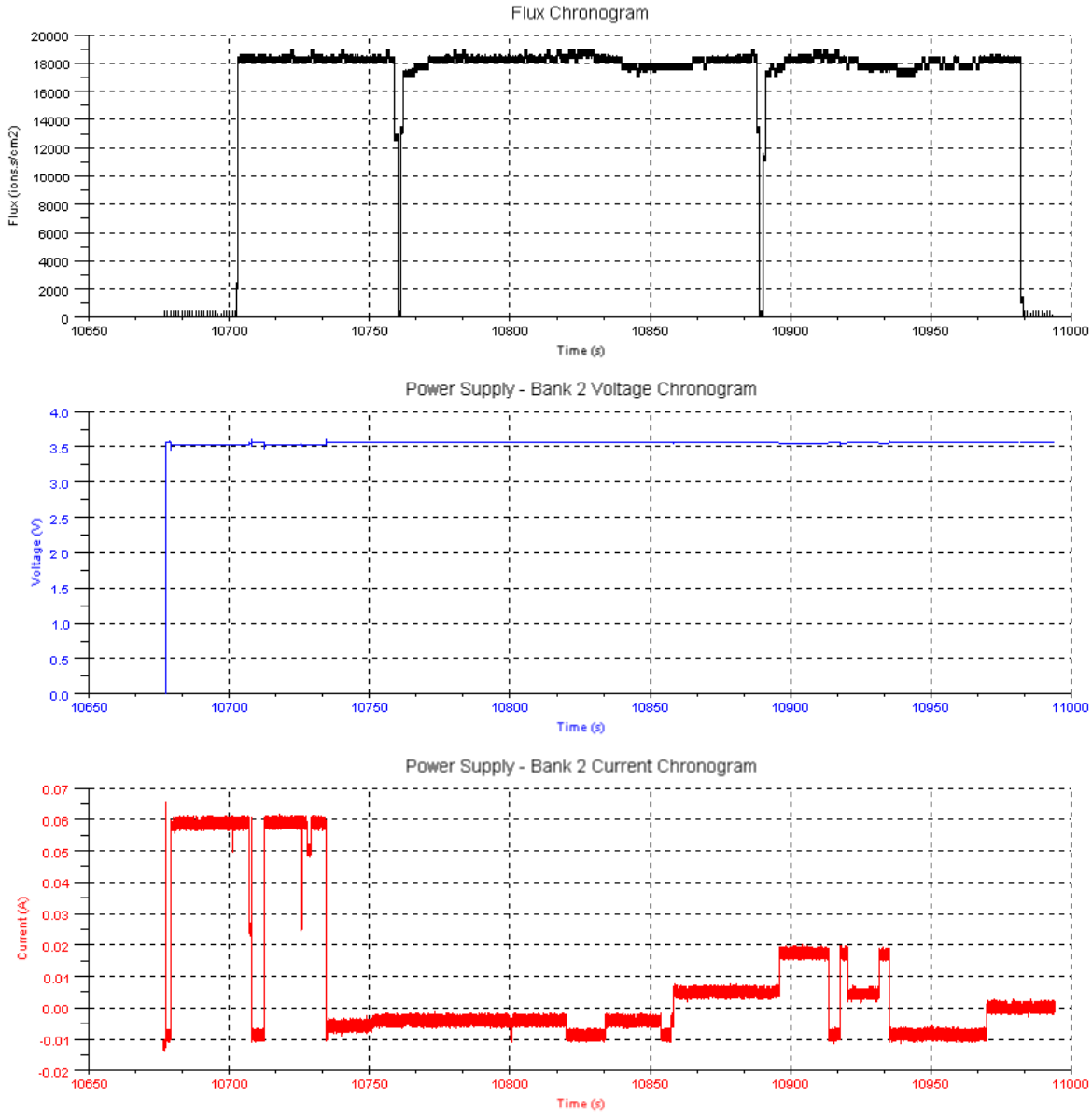


Figure 24: RADEF June 2010 - RUN 159 - Bank 2 power supply

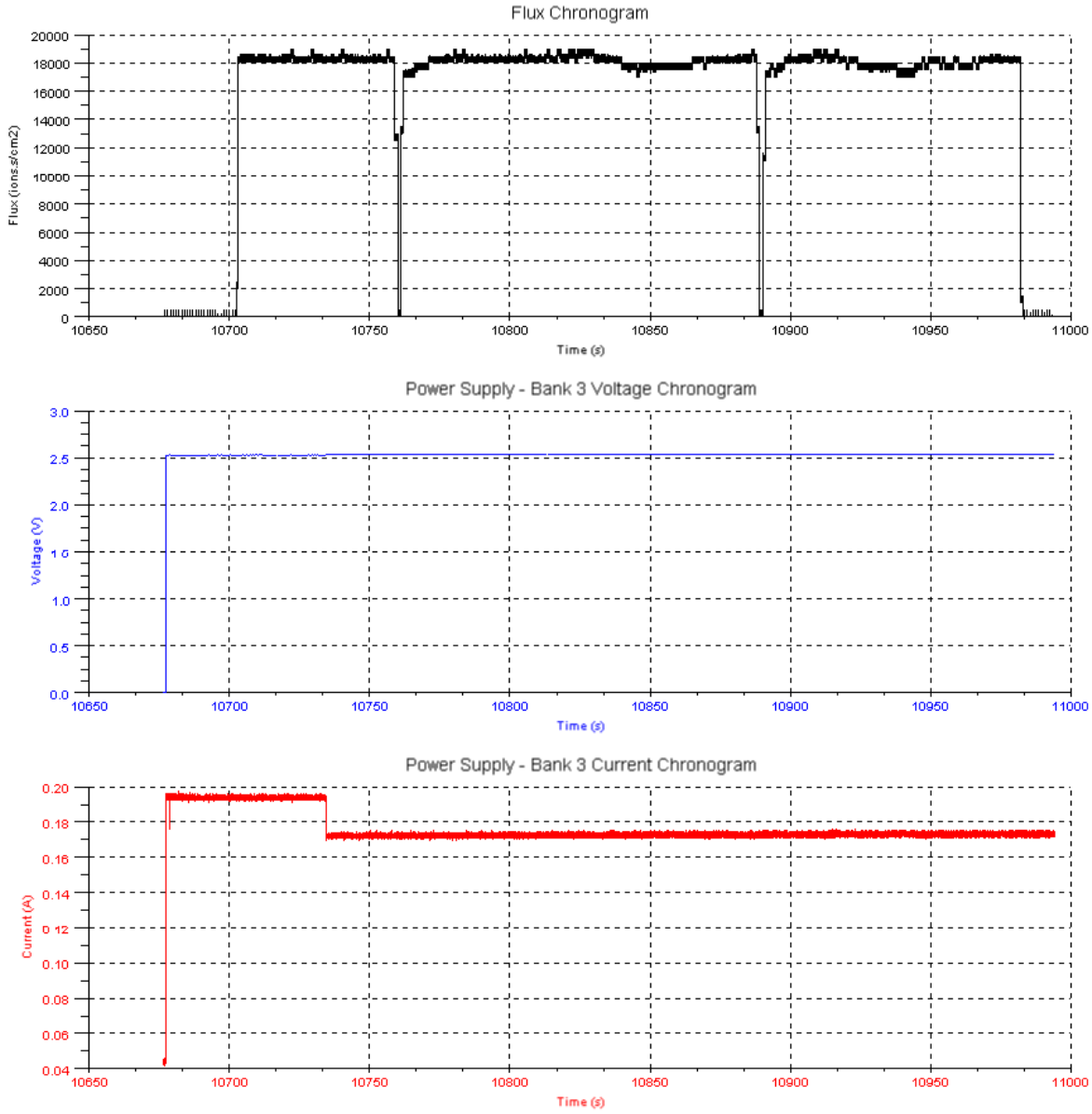


Figure 25: RADEF June 2010 - RUN 159 - Bank 3 power supply

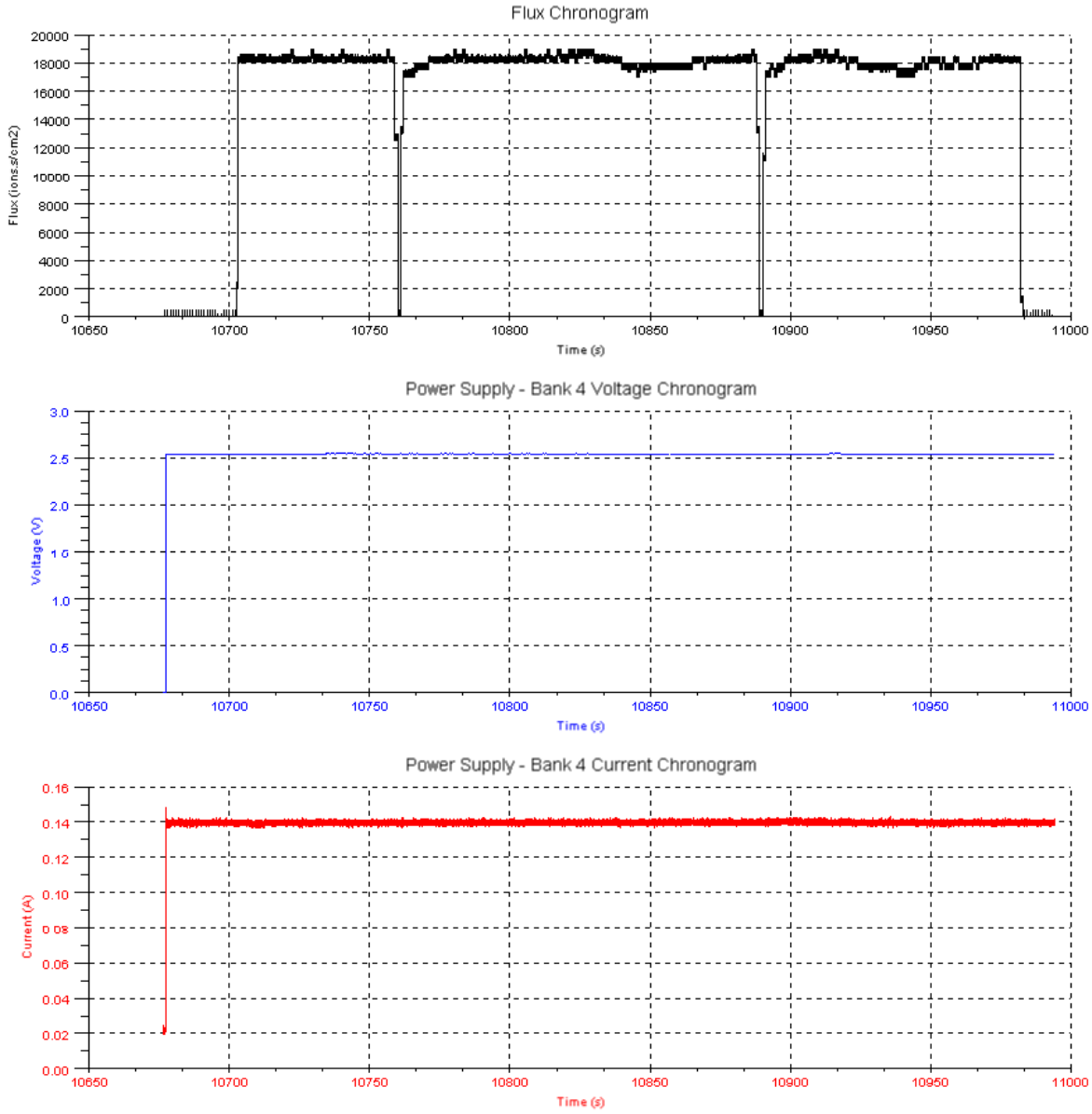


Figure 26: RADEF June 2010 - RUN 159 - Bank 4 power supply

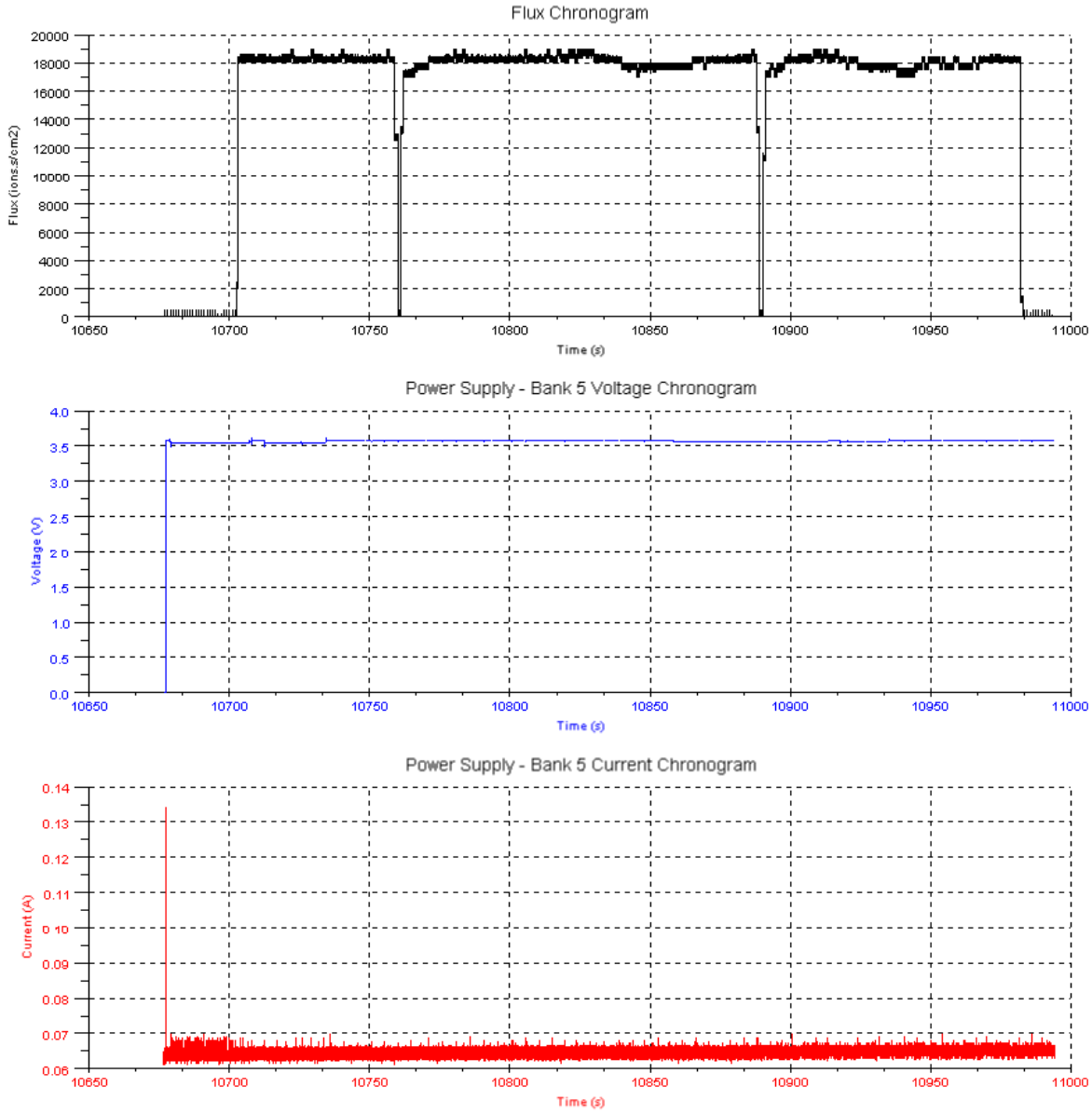


Figure 27: RADEF June 2010 - RUN 159 - Bank 5 power supply

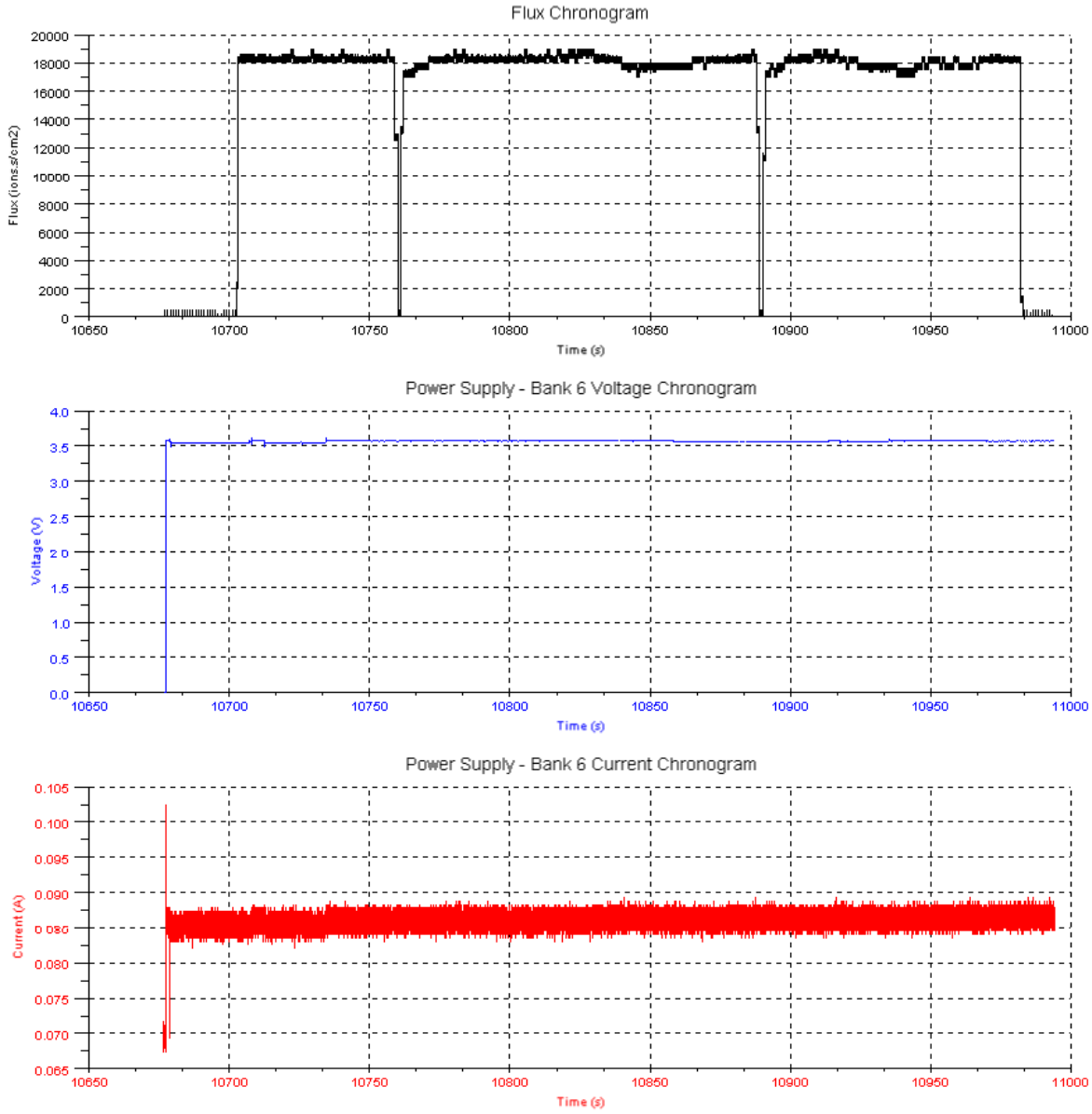


Figure 28: RADEF June 2010 - RUN 159 - Bank 6 power supply

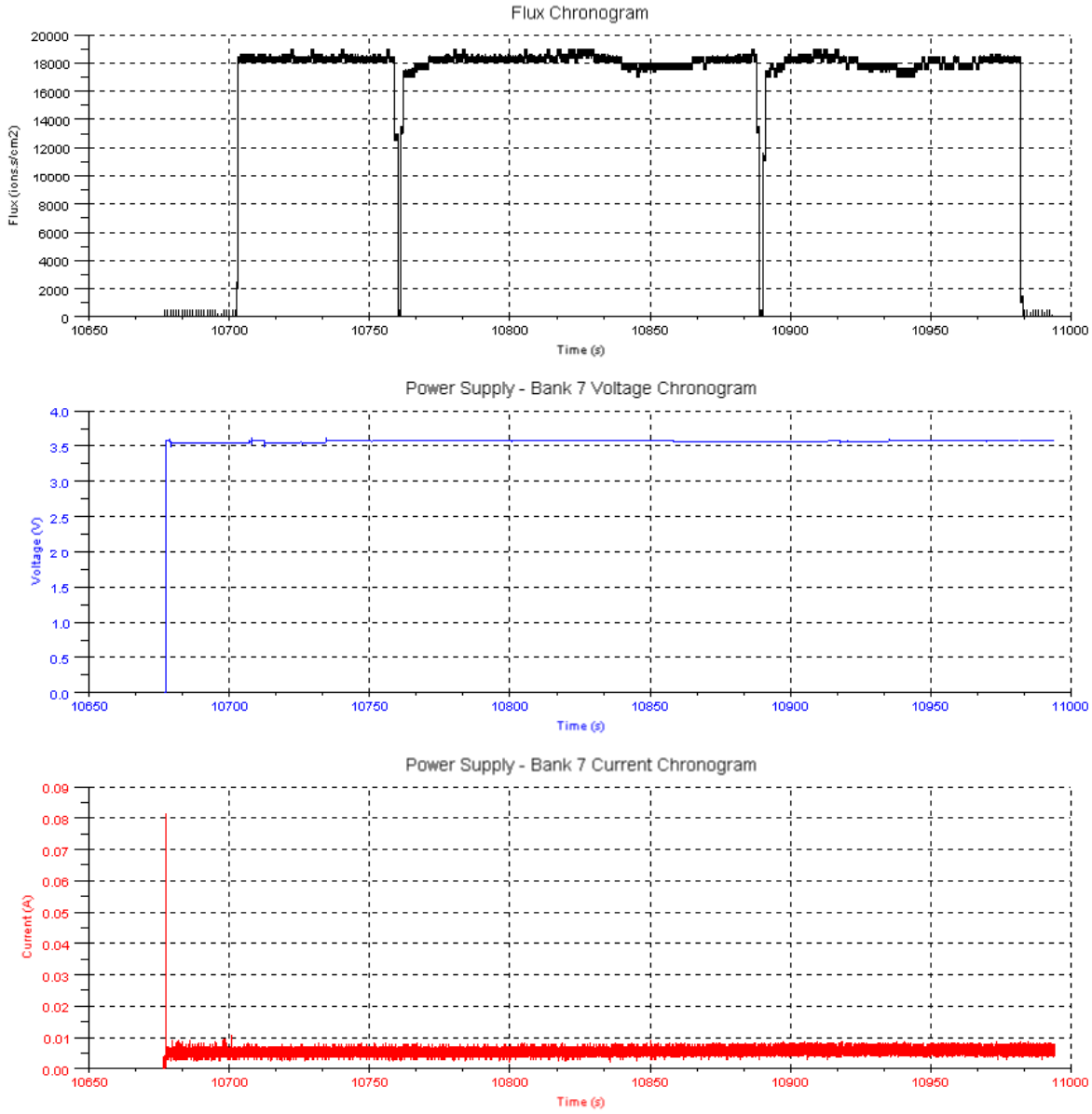


Figure 29: RADEF June 2010 - RUN 159 - Bank 7 power supply

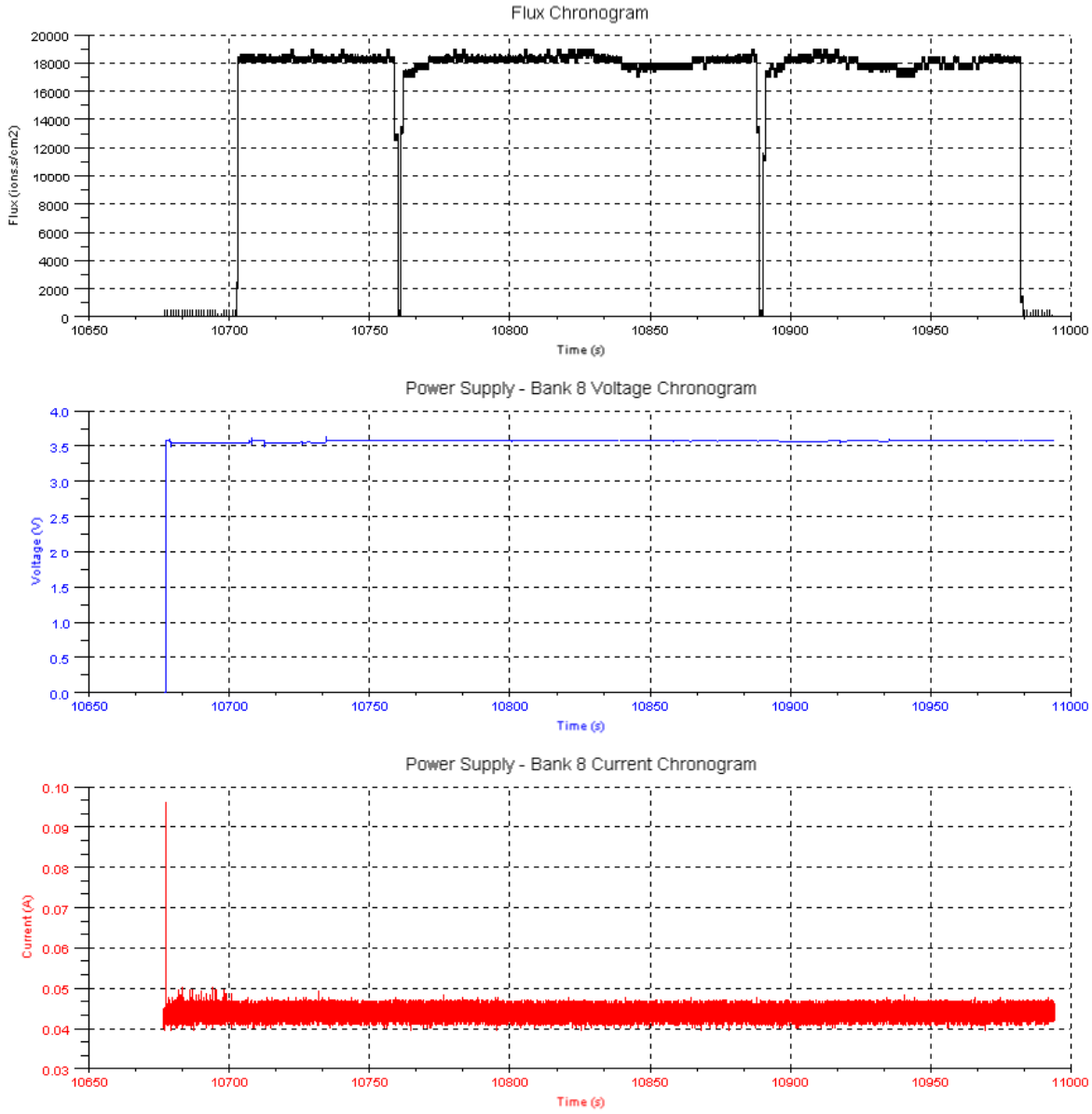


Figure 30: RADEF June 2010 - RUN 159 - Bank 8 power supply

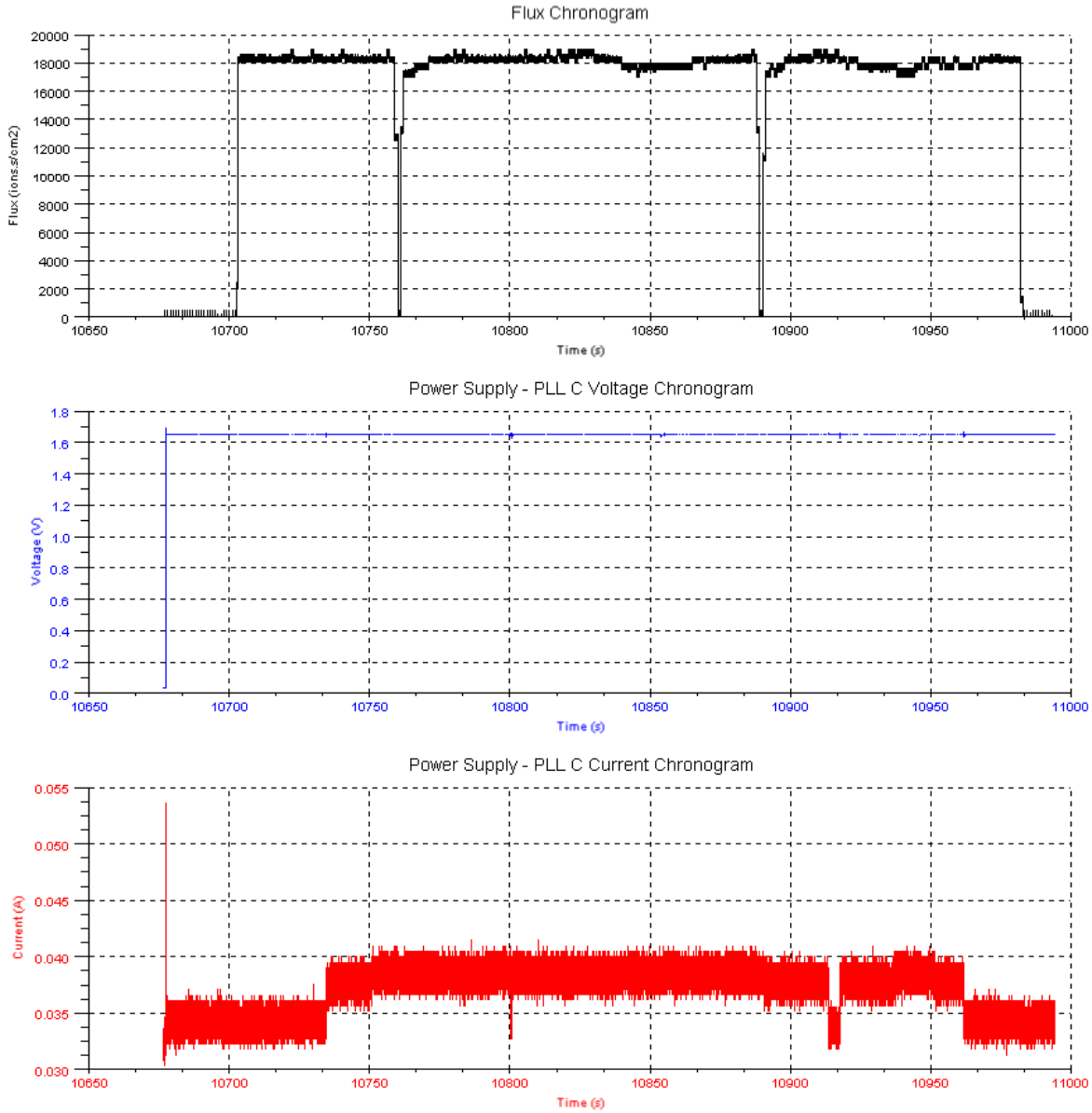


Figure 31: RADEF June 2010 - RUN 159 - PLL C power supply

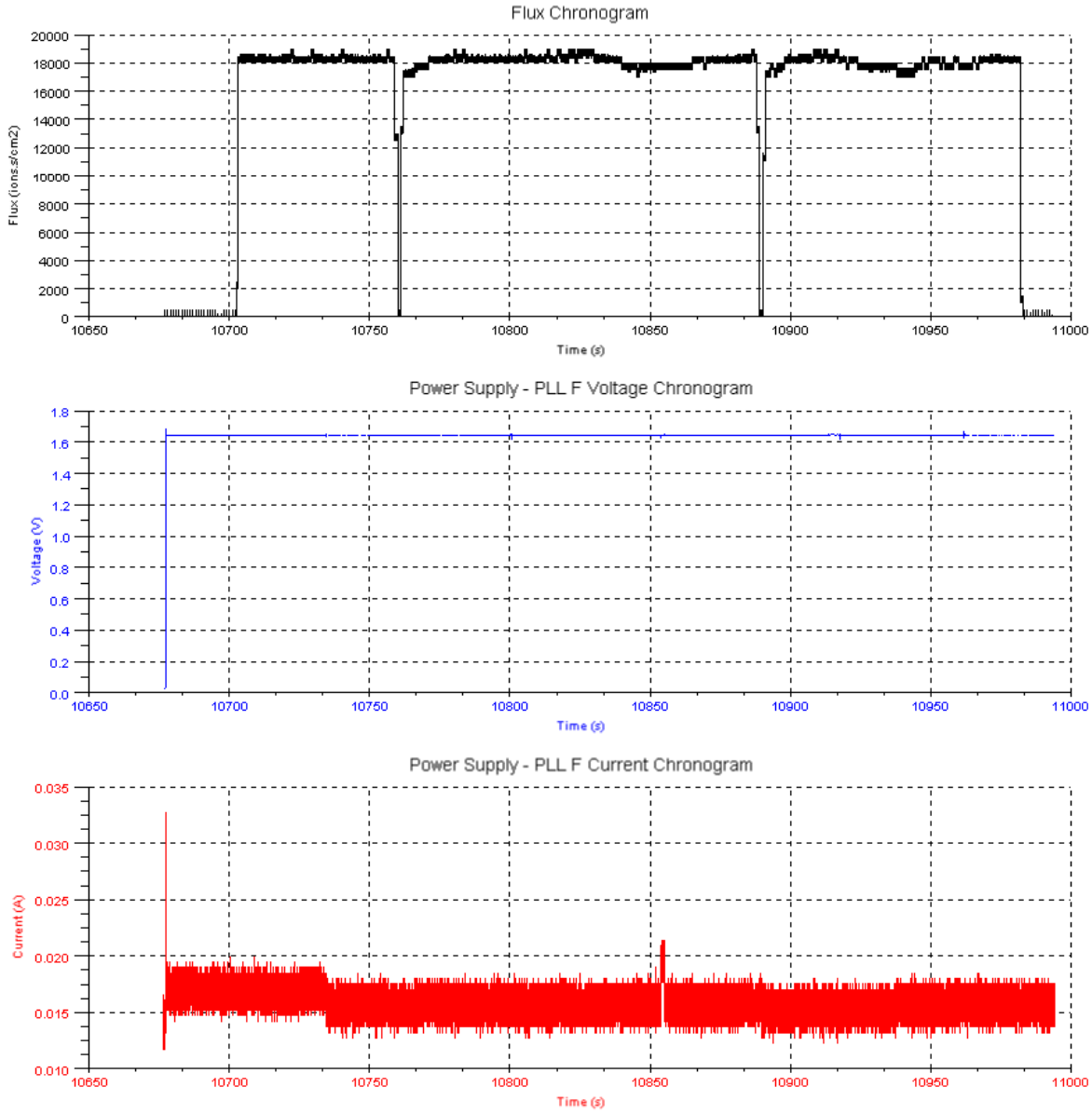


Figure 32: RADEF June 2010 - RUN 159 - PLL F power supply

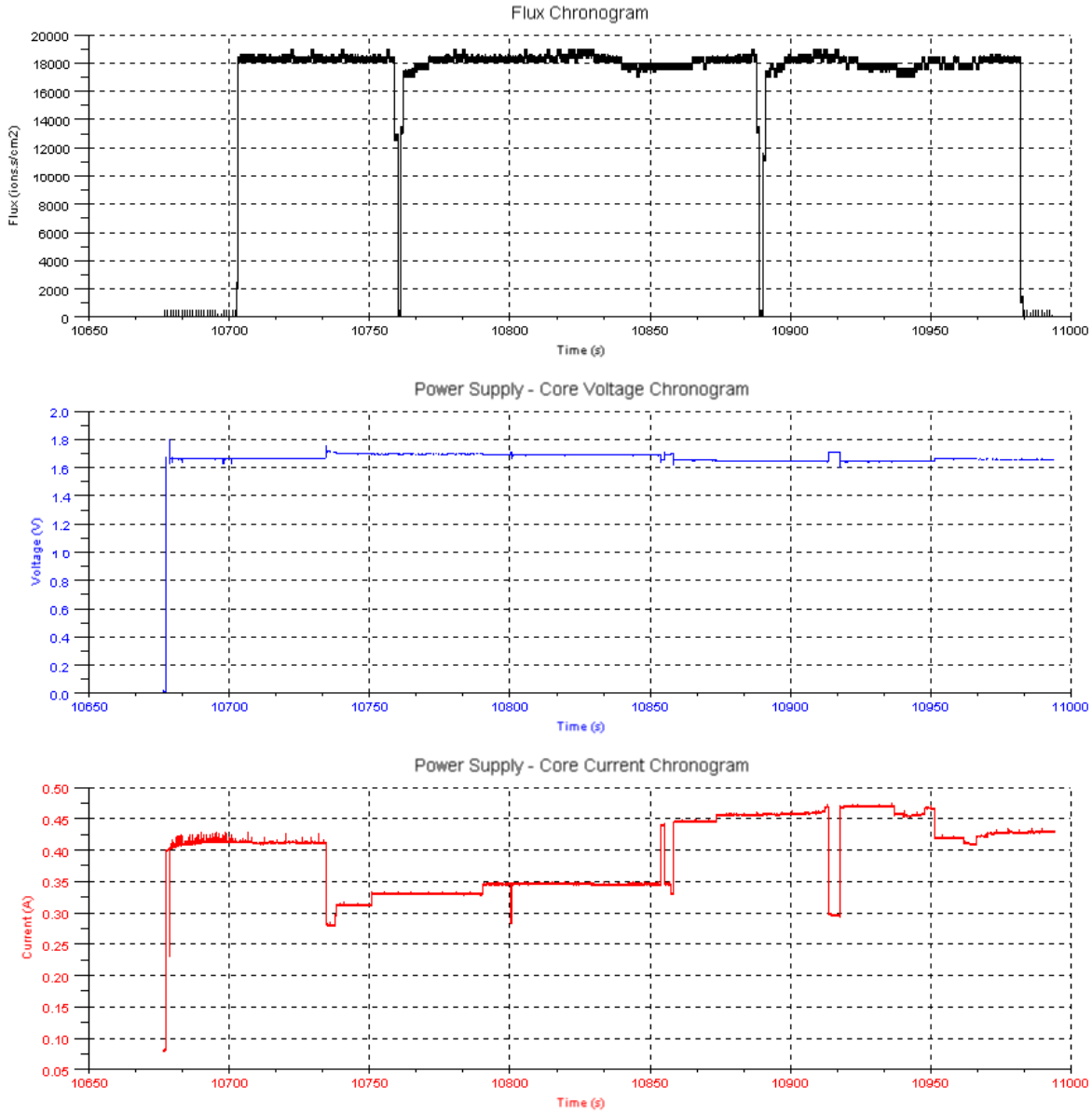


Figure 33: RADEF June 2010 - RUN 159 - Core power supply

9.2 TV1 - SHIFT REGISTER

9.2.1 TV1 - SR1

The Figure 34 displays the SEU cross-sectional area per bit of the TV1 SR1. This SEU cross-section per bit is characterized with an asymptotic cross-section (saturation cross-section) below 3E-7 cm² and a LET threshold around 1.8 MeV.cm²/mg.

On the plot, one Weibull fit curve was estimated from the points and added to the graph. The estimated Weibull fit curve is calculated from the following equation of the cumulative distribution function:

$$\sigma = CSsat\left(1 - e^{-(x/\lambda)K}\right)$$

With the following parameters values:

K = 1
λ = 80
X_0 = 1.8 Mev.cm²/mg
CSsat = 3E-7 cm²

This same Weibull fit curve is then used as reference Weibull curve on all the SEU cross-sectional area plots.

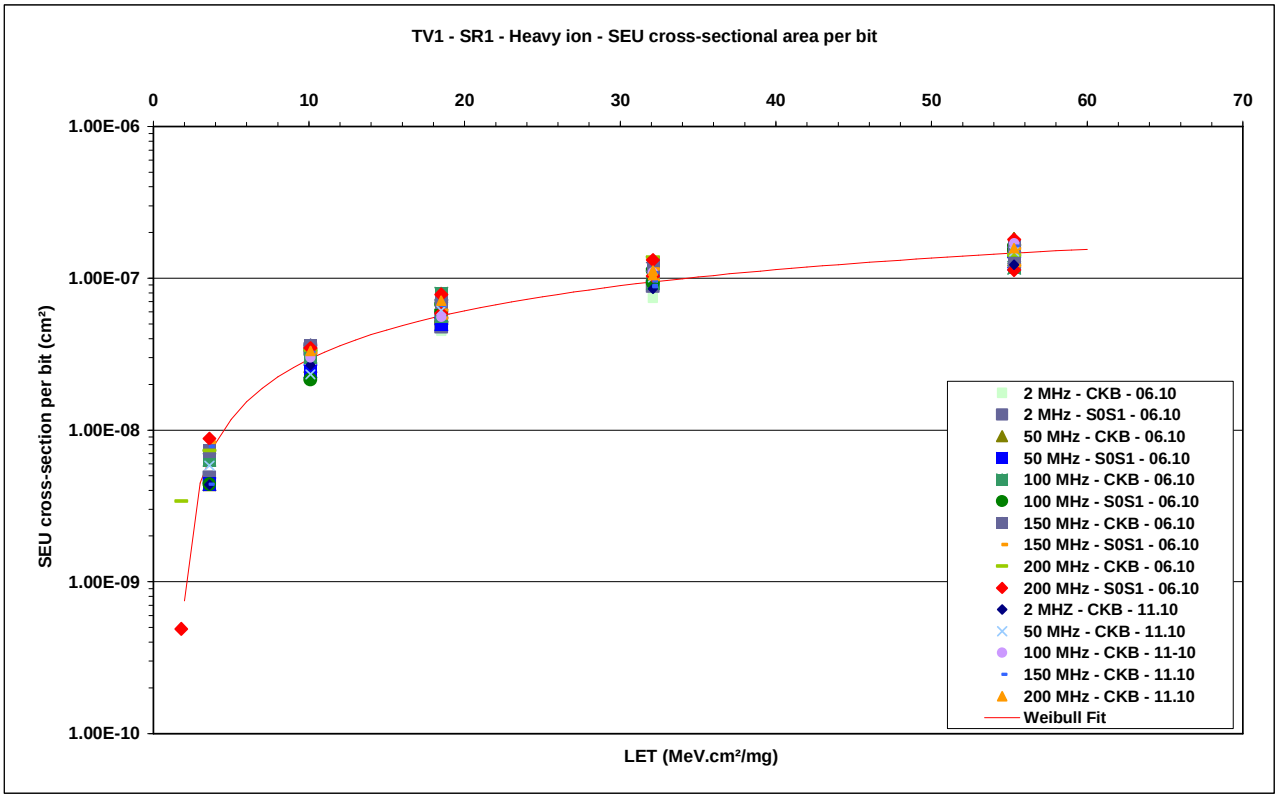


Figure 34: TV1 - SR1 - SEU cross-sectional area per bit

An extremely light influence of the working frequency can be seen on the SEU cross-section of the TV1 SR1 as highlighted on the Figure 35. In addition to the reference Weibull curve, 2 other Weibull curves were estimated and plotted: one fitting the 2 MHz points and one fitting the 200 MHz points. The 3 Weibull curves have the same parameters: K, Xo and CSsat. The λ parameter is as in Table 12:

Weibull curve	λ parameter value
Weibull reference	80
Weibull fit - 2 MHz	100
Weibull fit - 200MHz	60

Table 12: TV1 - SR1 - λ parameter values

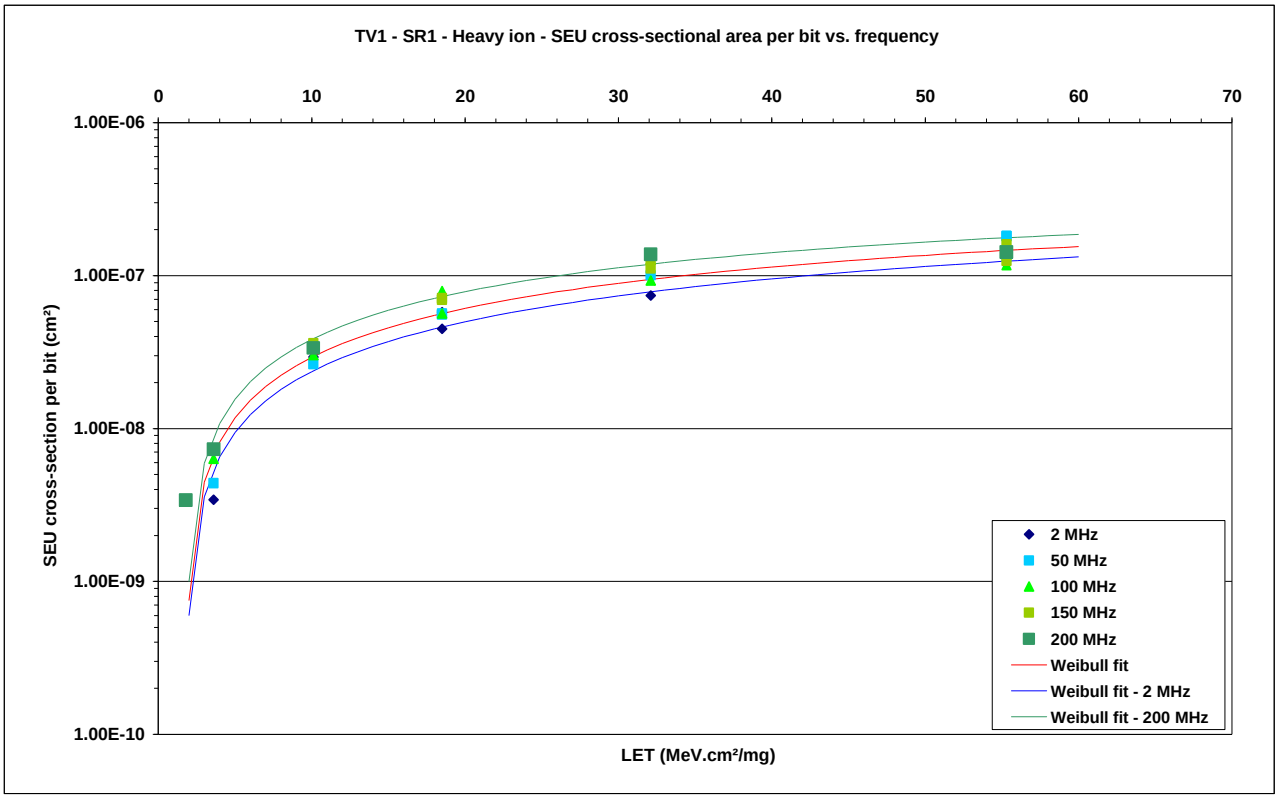


Figure 35: TV1 - SR1 - SEU cross-sectional area per bit vs. frequency

The Figure 36 plots the distribution of the SEU. Most errors are SBU where almost 2/3 of those errors are due to clear transition (also called reset transition: transition from '1' to '0'). The other 1/3 is made of set transition (transition from '0' to '1'). Some MBUs can be counted as well. The MBUs are made of:

- ✓ A large majority of arbitrary numbers of consecutive reset bits which look like a local perturbation, more or less spread, on the global reset signal.
- ✓ Few 2 consecutive bits toggled: most probably due to 2 adjacent registers impacted by the same ion hit.
- ✓ Mixes of errors

This same SEU distribution plot is used as reference for all the other SEU distribution graphs.

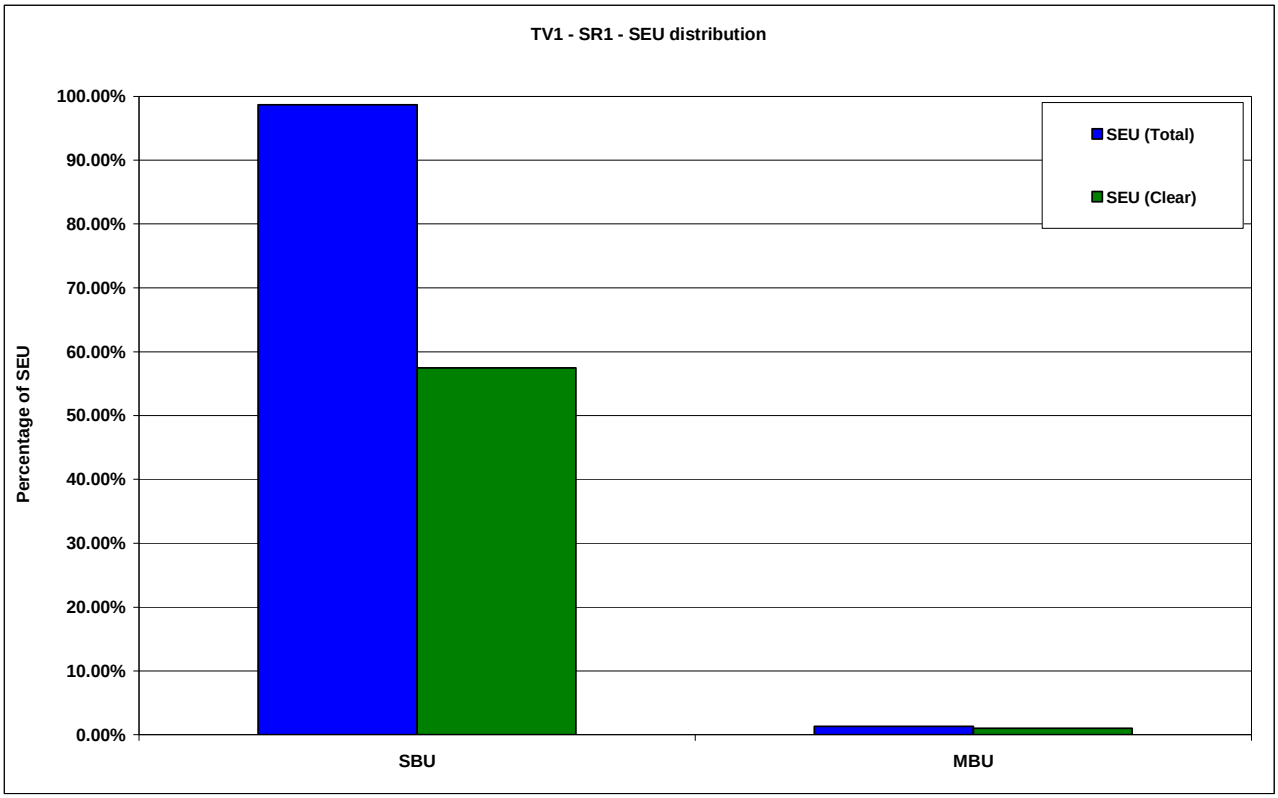


Figure 36: TV1 - SR1 - SEU distribution

9.2.2 TV1 - SR2

The TV1 SR2 channel implemented combinational cells on the global enable signal path.

The SEU cross-sectional area per bit of this channel is plotted on the Figure 37. It is characterized with an asymptotic cross-section (saturation cross-section) below 3E-7 cm² per bit and a LET threshold around 1.8 MeV.cm²/mg. No difference between this channel and the reference is visible on the plot of the cross-section: the reference Weibull curve fits well the measured points of this channel.

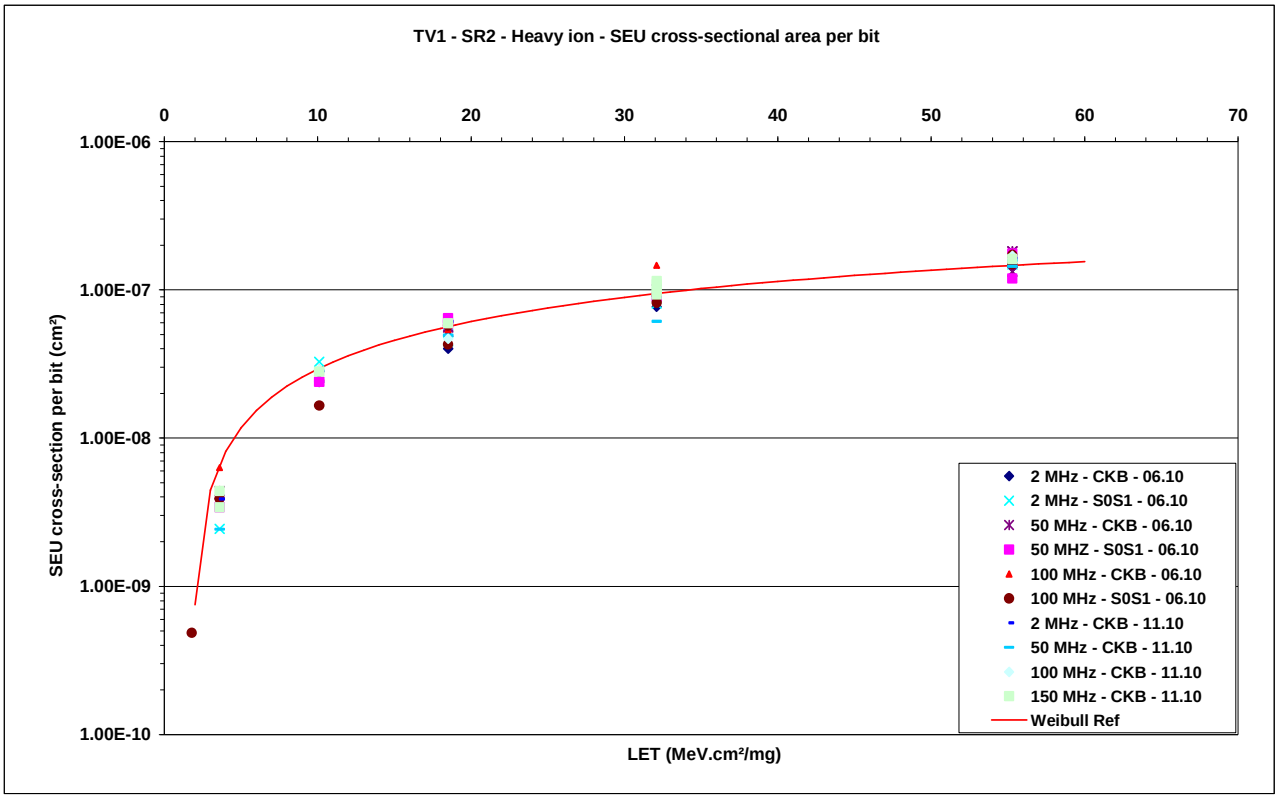


Figure 37: TV1 - SR2 - SEU cross-sectional area per bit

The frequency does not appear to influence the SEU cross-section or so lightly than it is not clearly visible. The SEU cross-section area per bit vs. the frequency is visible on the Figure 38.

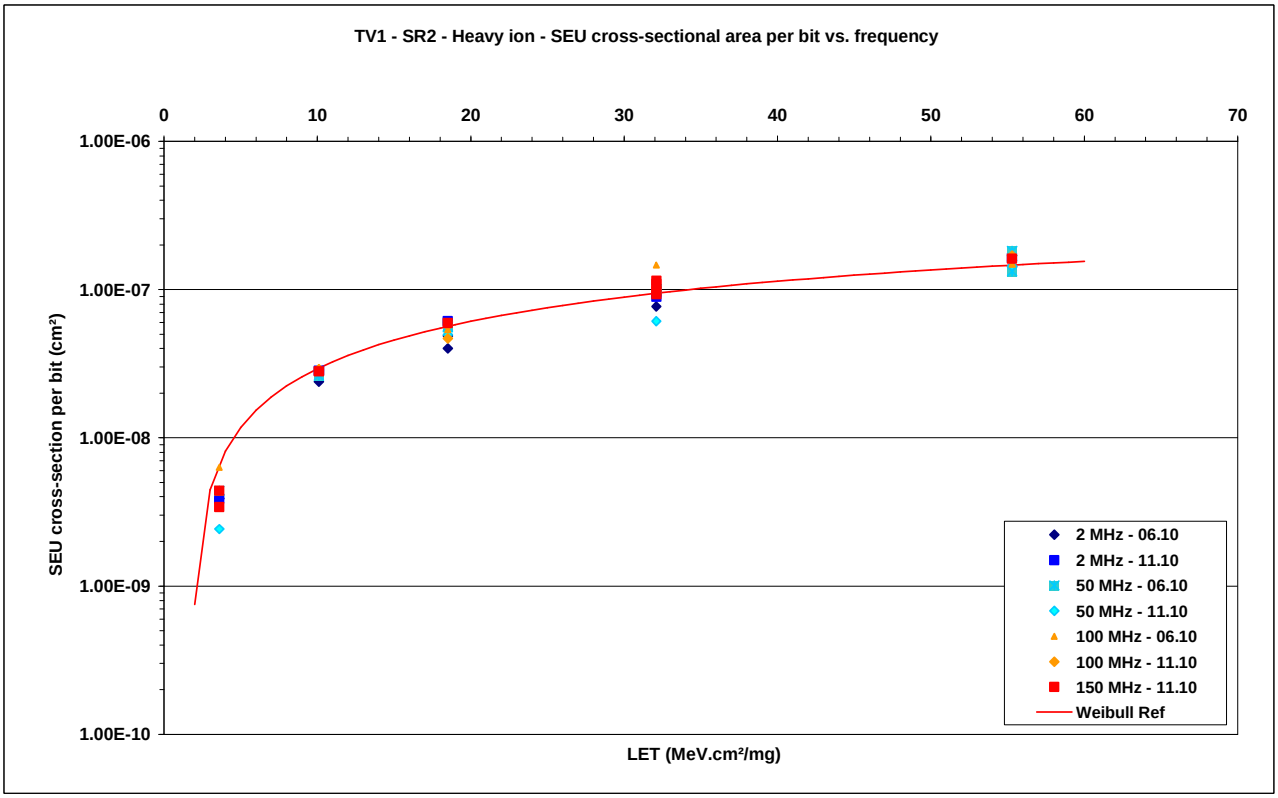


Figure 38: TV1 - SR2 - SEU Cross-sectional area per bit vs. frequency

The Figure 39 plots the SEU distribution. Like the reference channel, most errors are SBUs with more than half of those due to clear transition. MBUs percentages and signatures are like the reference channel. However another signature of MBU appears. This signature shows an un-shifted quartet caused by an SET on the local enable signal caught at the active edge of the clock: data are held from shifting. Very few SETs on the enable signal were caught that way.

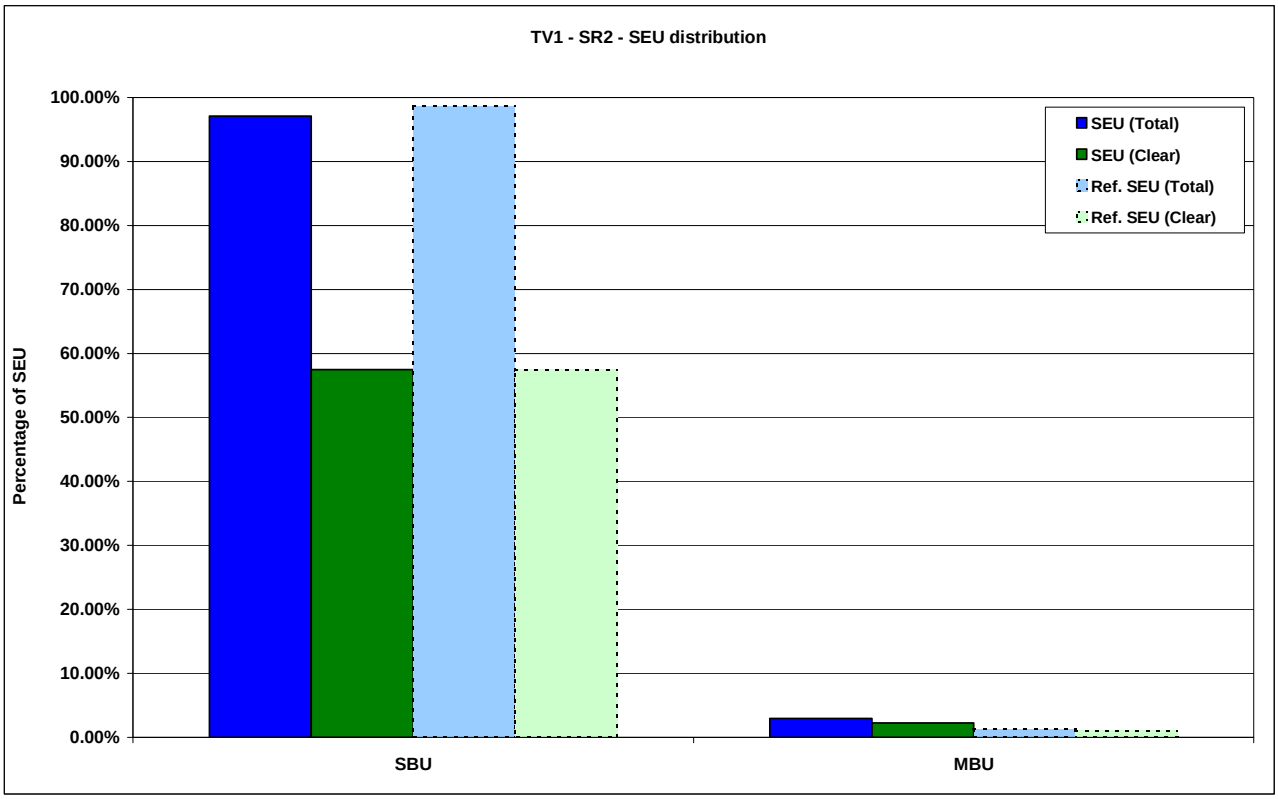


Figure 39: TV1 - SR2 - SEU distribution

9.2.3 TV1 - SR3

The TV1 SR3 channel implemented combinational cells on the global reset signal path.

The SEU cross-sectional area per bit of this channel is plotted on the Figure 40. It is characterized with an asymptotic cross-section (saturation cross-section) below 1E-6 cm² per bit and a LET threshold around 1.8 MeV.cm²/mg. This SEU cross-section is higher than the reference also added to the plot. A Weibull curve was estimated from the points and added to the graph. The TV1 SR3 Weibull fit curve has the following parameters:

K = 1
λ = 200
Xo = 1.8 MeV.cm²/mg
CSsat = 1E-6 cm²

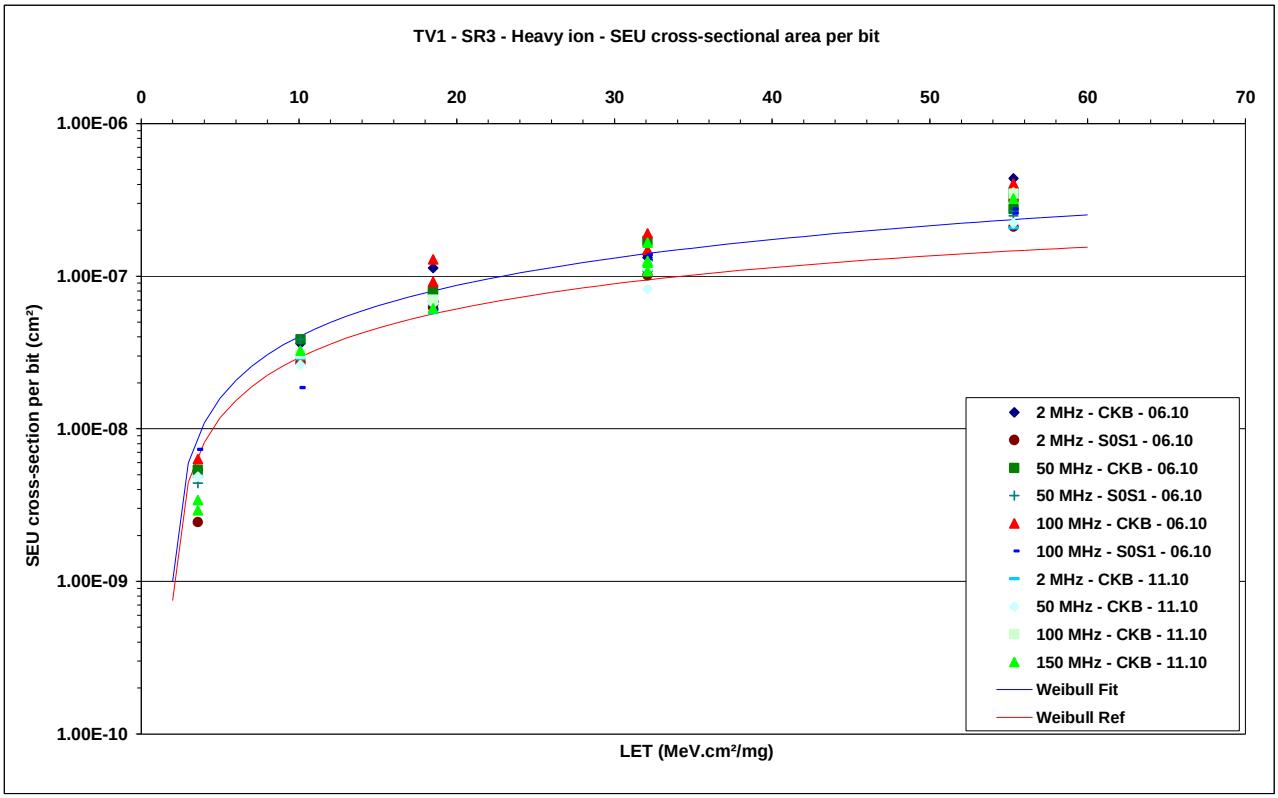


Figure 40: TV1 - SR3 - SEU cross-sectional area per bit

Because the reset signal is an asynchronous signal each time its value steps into the bounces of the active level for a time longer or equal to the asynchronous clear minimum pulse width (Twclr # 0.3 ns), the register is cleared. As a consequence SEU and SET on the global (or local) reset signal longer than Twclr clear the register.

The Figure 41 plots the SEU distribution. Almost 80% of SEUs are SBUs and 70% of those are due to clear transition. There is a high count of MBU compared to the reference channel and almost all of the MBUs are due to arbitrary number of reset bits (clear bit).

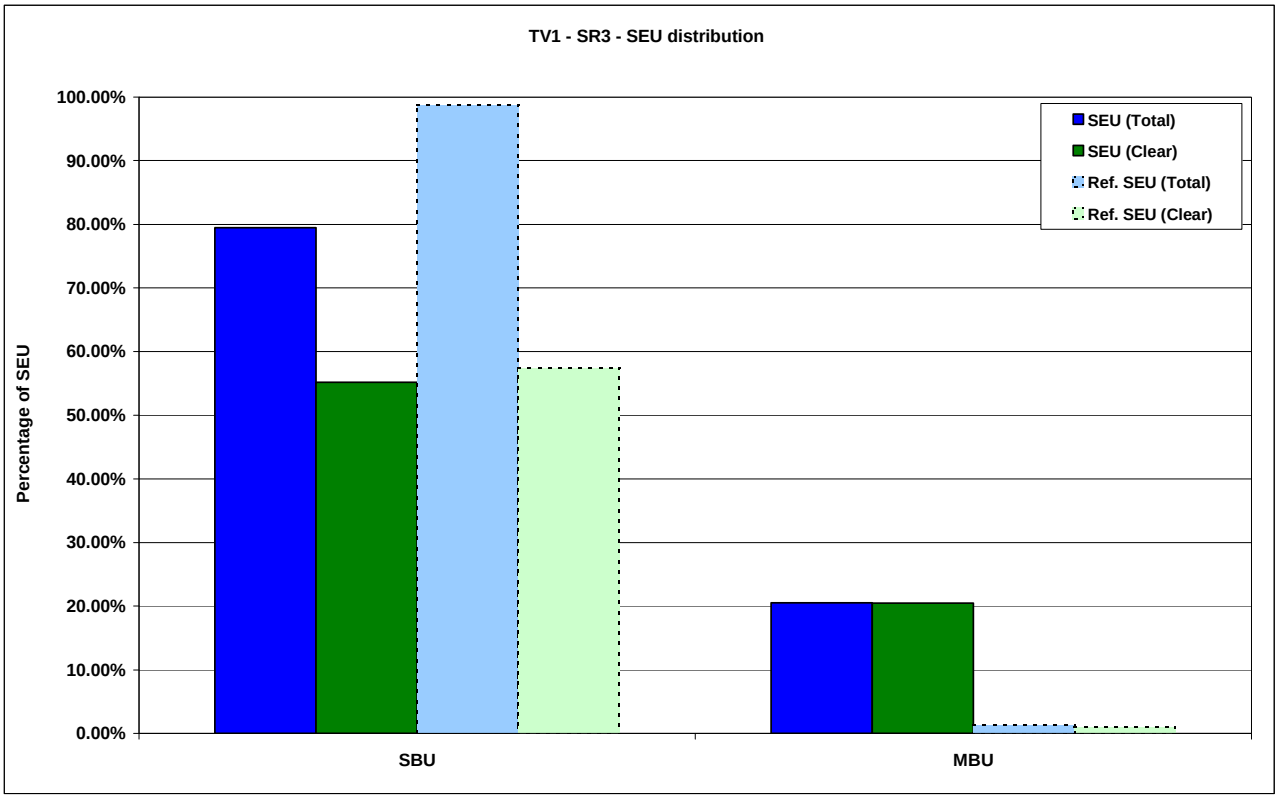


Figure 41: TV1 - SR3 - SEU distribution

9.2.4 TV1 - SR4

The TV1 SR4 channel implemented combinational cells in-between each register.

The SEU cross-sectional area per bit is equivalent to the reference channel as compared on the Figure 42. It is characterized with an asymptotic cross-section (saturation cross-section) below 3E-7 cm² per bit and a LET threshold around 1.8 MeV.cm²/mg.

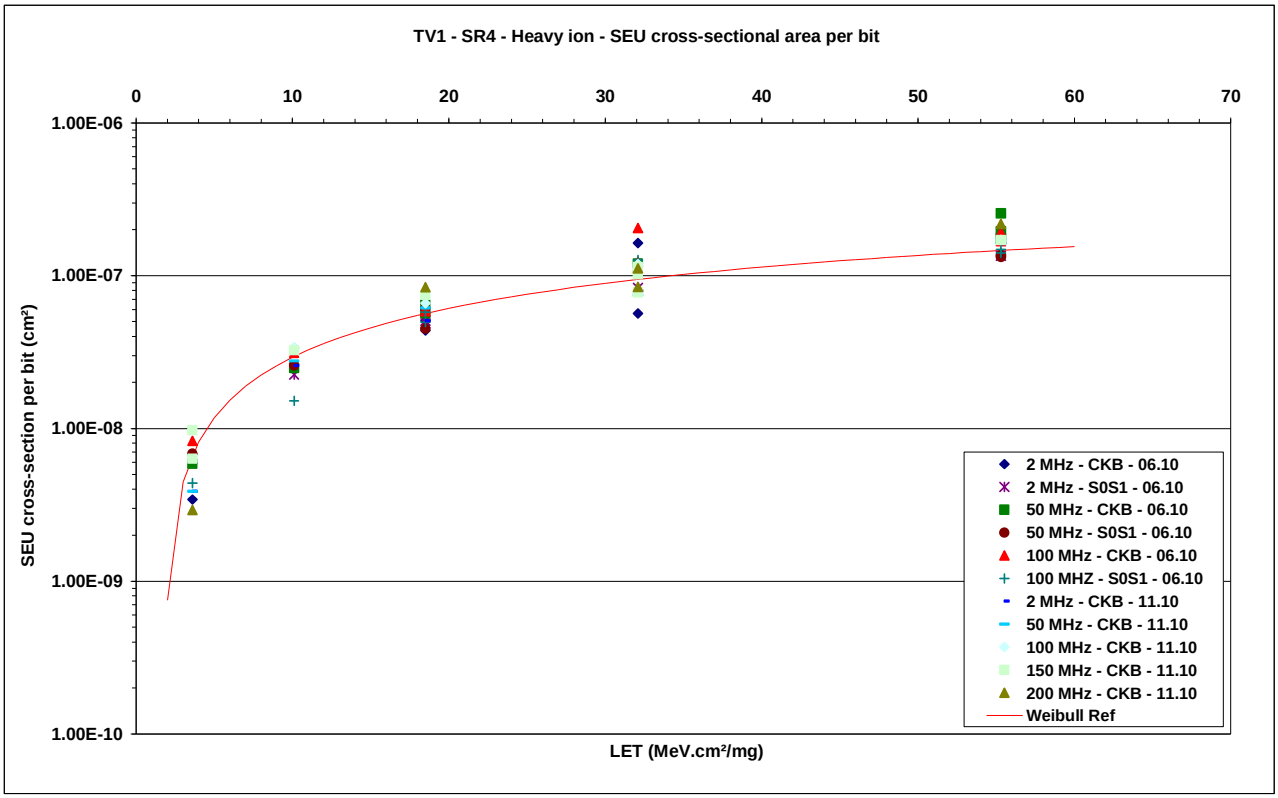


Figure 42: TV1 - SR4 - SEU cross-sectional area per bit

The influence of the frequency plotted on the Figure 43 is not highly visible on the SEU cross-section. The 3 reference Weibull curves of the reference channel were also added to the plot for comparison purpose.

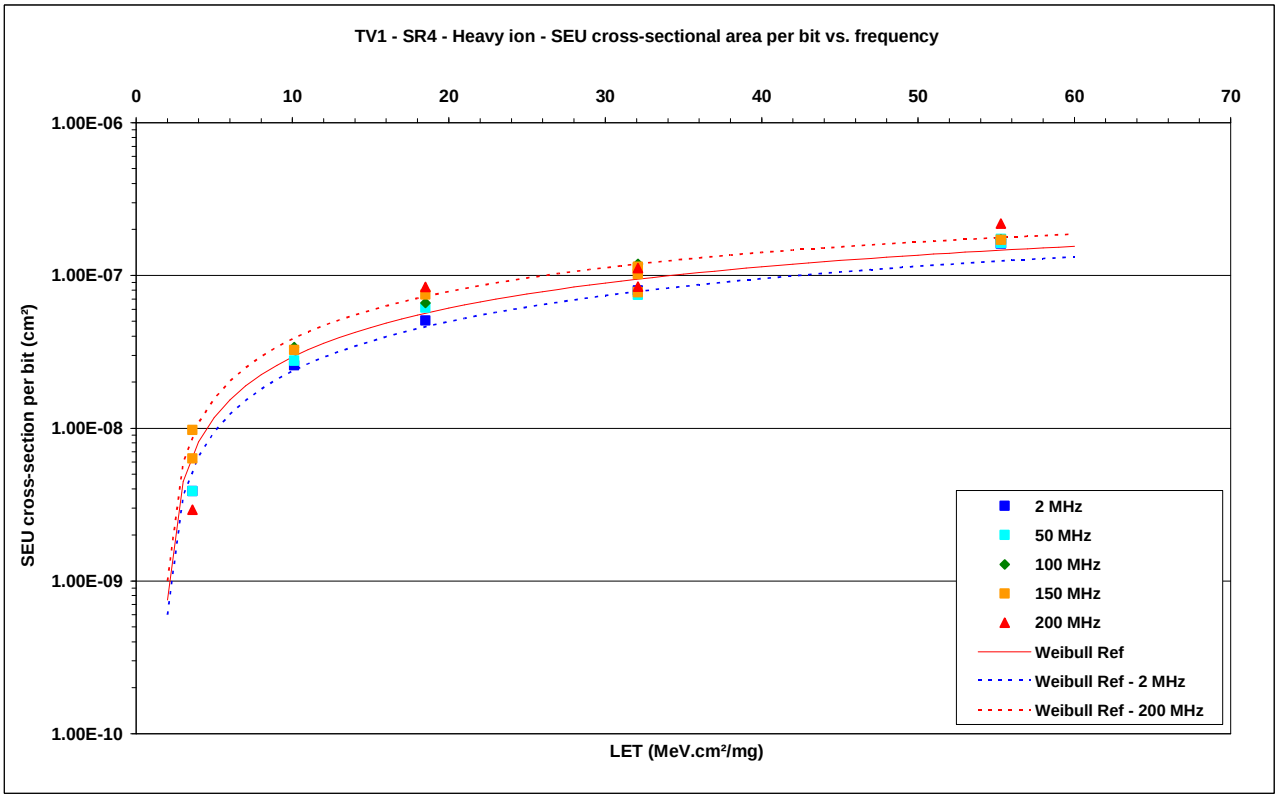


Figure 43: TV1 - SR4 - SEU cross-sectional area per bit vs. frequency

The Figure 44 plots the SEU distribution. Like the reference channel, most SEUs are SBUs and 2/3 of those are due to clear transition. Comparing SEU cross-section and signatures, this channel is very similar to the reference one.

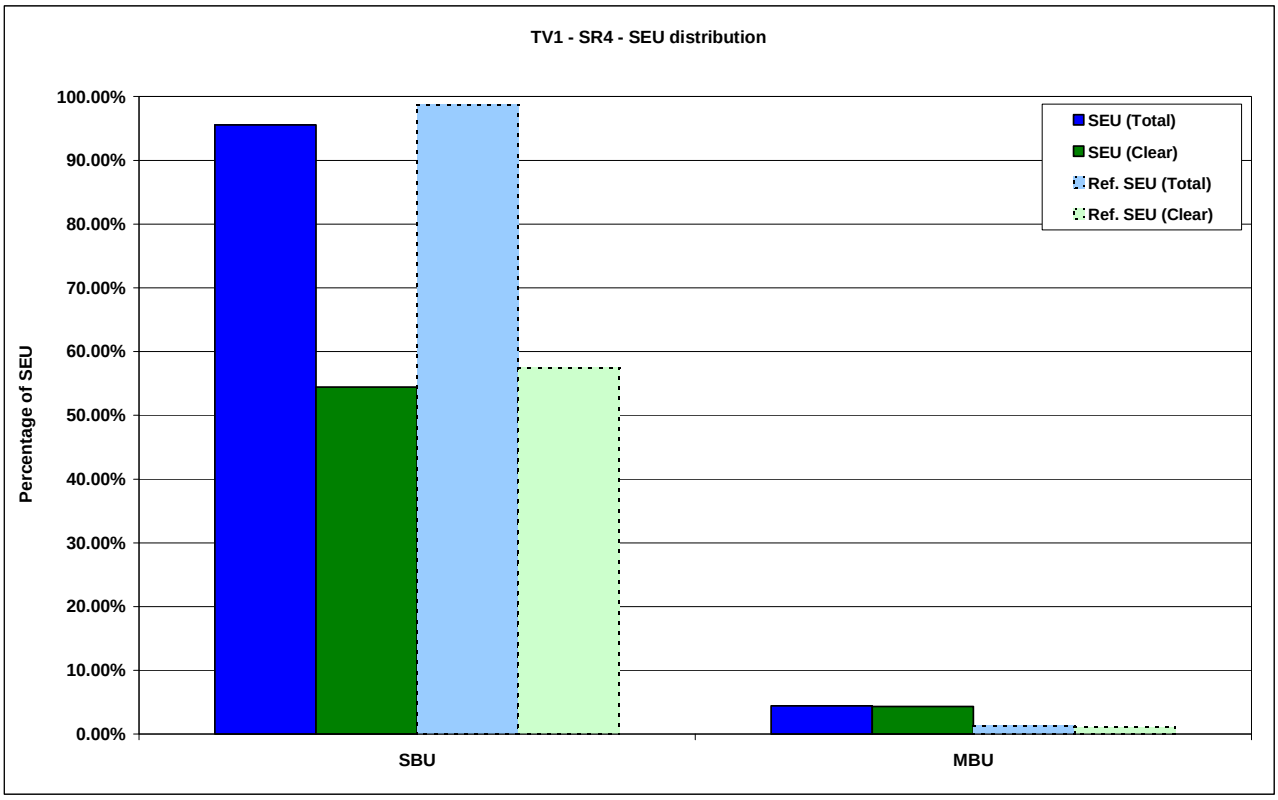


Figure 44: TV1 - SR4 - SEU distribution

9.2.5 TV1 - SR5, 6, 7 and 8

The TV1 SR5, 6, 7 and 8 channels implemented Double Data Rate (DDR) registers at the input/output stages.

The SEU cross-section area per bit of those channels is very similar to the reference channel as it can be seen on the Figure 45. It is characterized with an asymptotic cross-section (saturation cross-section) below 3E-7 cm^2 per bit and a LET threshold around 1.8 $MeV.cm^2/mg$.

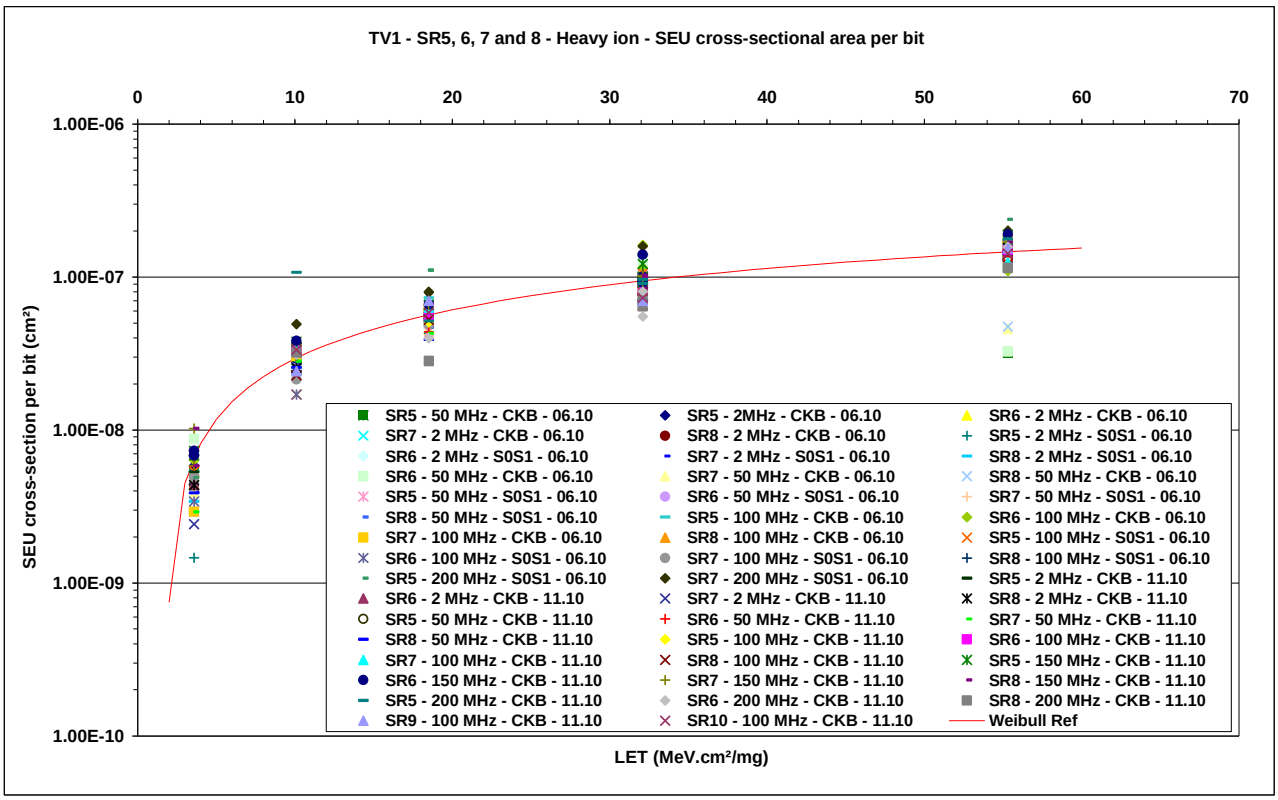


Figure 45: TV1 - SR5, 6, 7 and 8 - SEU cross-sectional area per bit

The Figure 46 plots the SEU distribution. Like the reference channel, most SEUs are SBUs with more than the half of those due to clear transition. MBUs signatures are very similar to the reference channel.

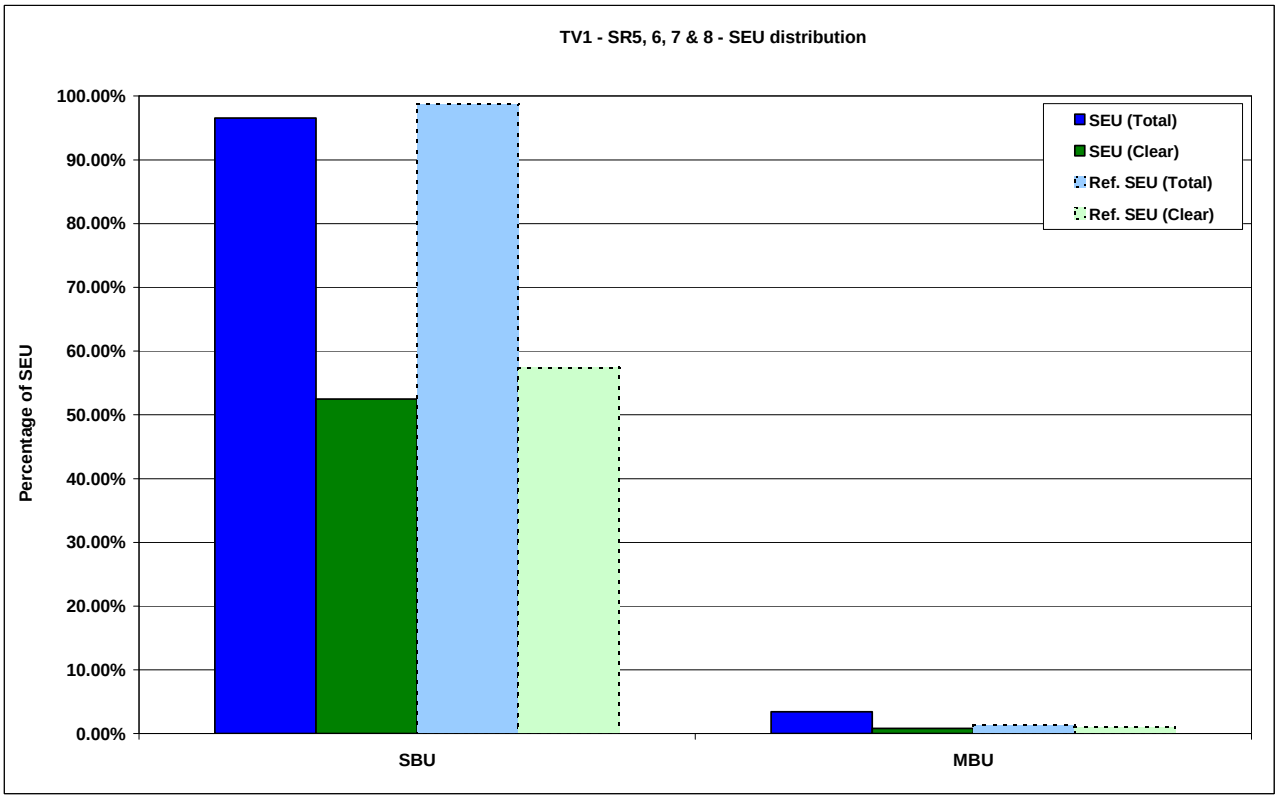


Figure 46: TV1 - SR5, 6, 7 and 8 - SEU distribution

9.2.6 TV1 - SR9 and 10

The TV1 SR9 and 10 channels implemented LVDS buffers at the input/output stages.

The SEU cross-sectional area per bit is very similar to the reference channel. It is plotted on the Figure 47. It is characterized with an asymptotic cross-section (saturation cross-section) below 3E-7 cm² per bit and a LET threshold around 1.8 MeV.cm²/mg.

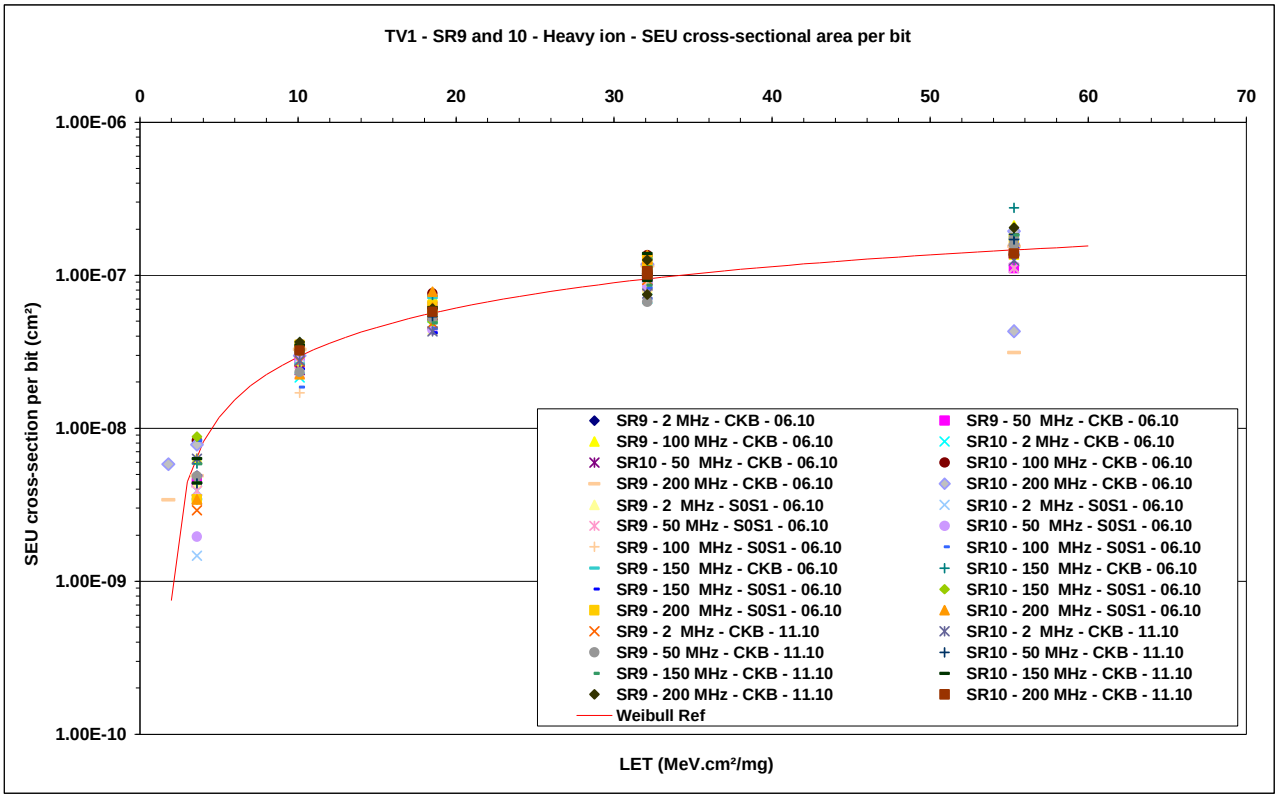


Figure 47: TV1 - SR9 and 10 - SEU cross-sectional area per bit

The Figure 48 plots the SEU distribution. Like the reference channel, most SEUs are SBUs with almost 2/3 of those errors attended to clear transition. The very few MBUs are composed of the same signatures than the reference channel.

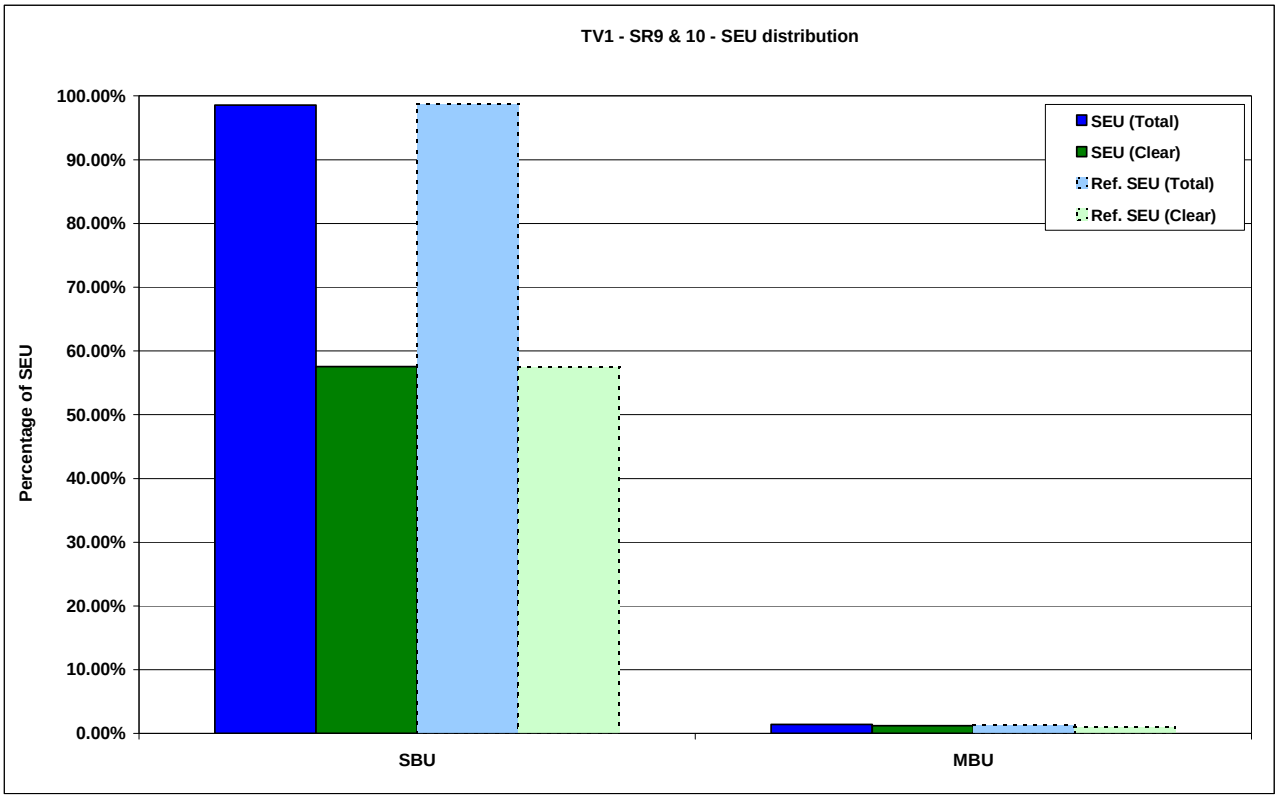


Figure 48: TV1 - SR9 and 10 - SEU distribution

9.2.7 TV1 - SR11, 12, 13 and 14

The TV1 SR11, 12, 13 and 14 channels were clocked by the PLL output clock.

The SEU cross-sectional area per bit is similar to the reference channel. It is plotted on the Figure 49. It is characterized with an asymptotic cross-section (saturation cross-section) below 3E-7 cm² per bit and a LET threshold around 1.8 MeV.cm²/mg.

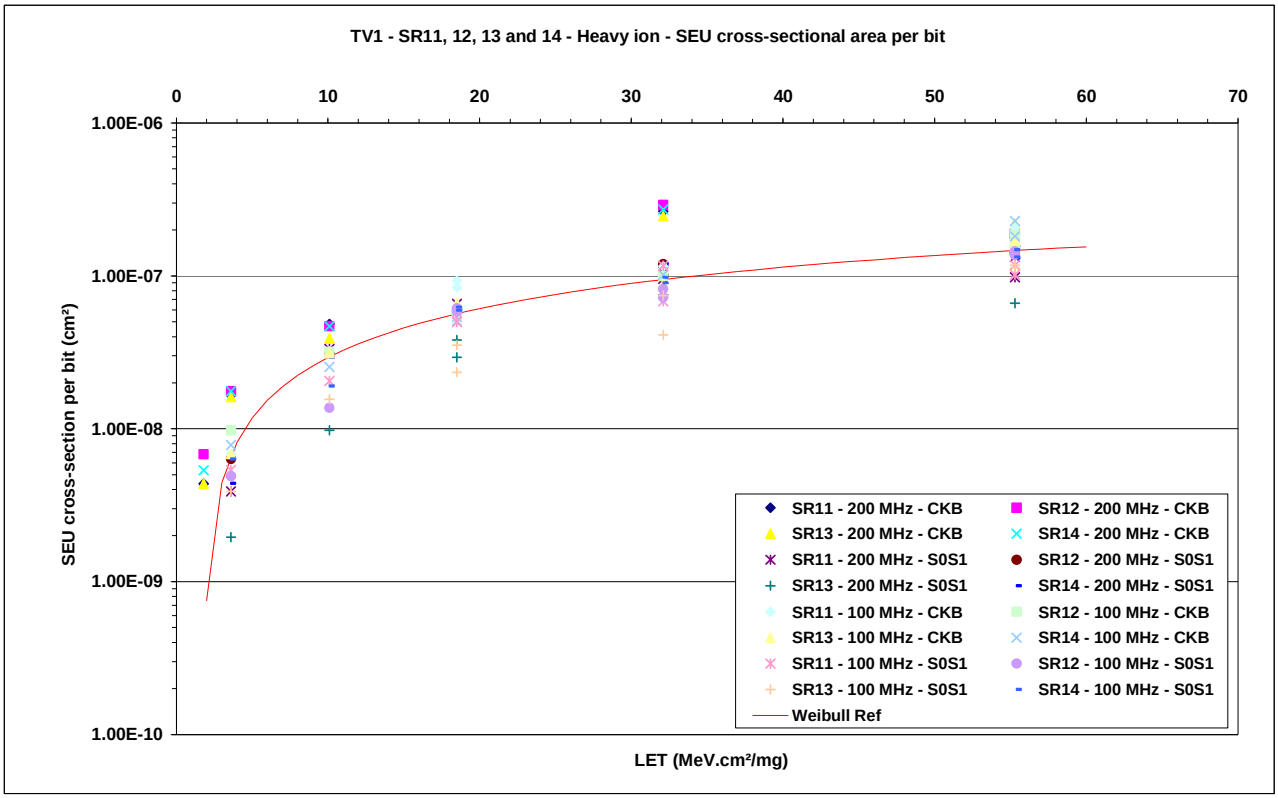


Figure 49: TV1 - SR11, 12, 13 and 14 - SEU cross-sectional area per bit

The Figure 50 plots the SEU distribution. Like the reference channel, most SEUs are SBUs with more than half coming from clear transition. MBUs signatures are the same as the reference channel: it was not seen a total flip or stuck bit of the channel that could lead to a total or partial stop of the PLL output clock.

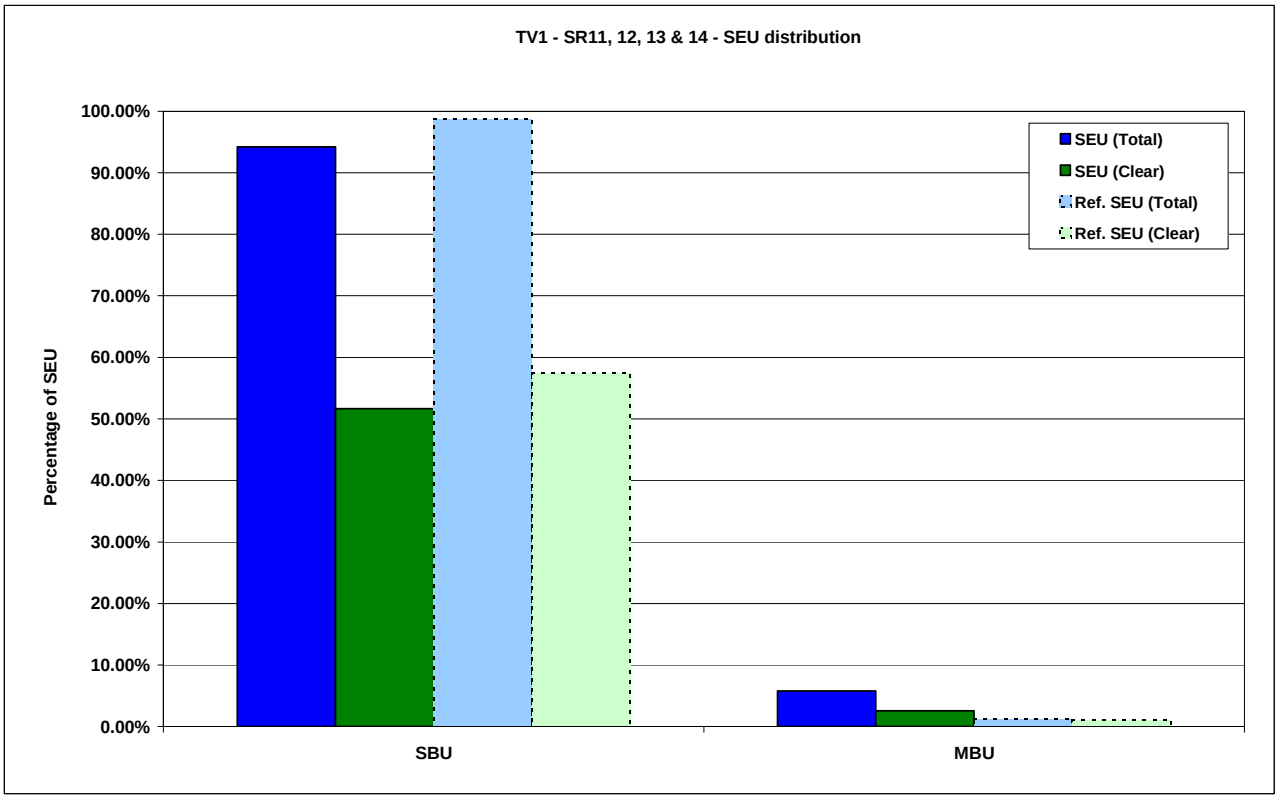


Figure 50: TV1 - SR11, 12, 13 and 14 - SEU distribution

9.3 TV2 - SHIFT REGISTER

One SEFI was detected and recorded during the campaign at RADEF on November 2010 on the RUN 112 with an effective LET of 55 MeV.cm²/mg. The device was configured with the TV2 and all shift registers were tested with a working frequency of 2 MHz. From the Iteration N° 257 (a fluence of 3.69E5 p/cm²) up to the end of the run (a fluence of 5E5 p/cm²) all the read data from the device were read at the low state (“0”). The device did not recover from the SEFI state by itself. The recovery took place after a power cycle of the device allowing the next run with the exact same conditions to be performed without any more SEFI detected.

9.3.1 TV2 - SR1

The TV2 SR1 implemented sequential cell triplication as SEU mitigation.

The Figure 51 displays the SEU cross-sectional area per bit of this channel. It is based on a poor statistic attended to the small number of errors. The reference Weibull curve was added to the graph for comparison purpose. It can be seen a large difference (around 2 decades) on both SEU cross-sections. The SEU cross-section is characterized with an asymptotic cross-section (saturation cross-section) below 2E-9 cm² per bit. The Weibull fit curve with the following parameters values was estimated from the points and added to the plot:

K = 1
λ = 80
Xo = 1.8 MeV.cm²/mg
CSsat = 2E-9 cm²

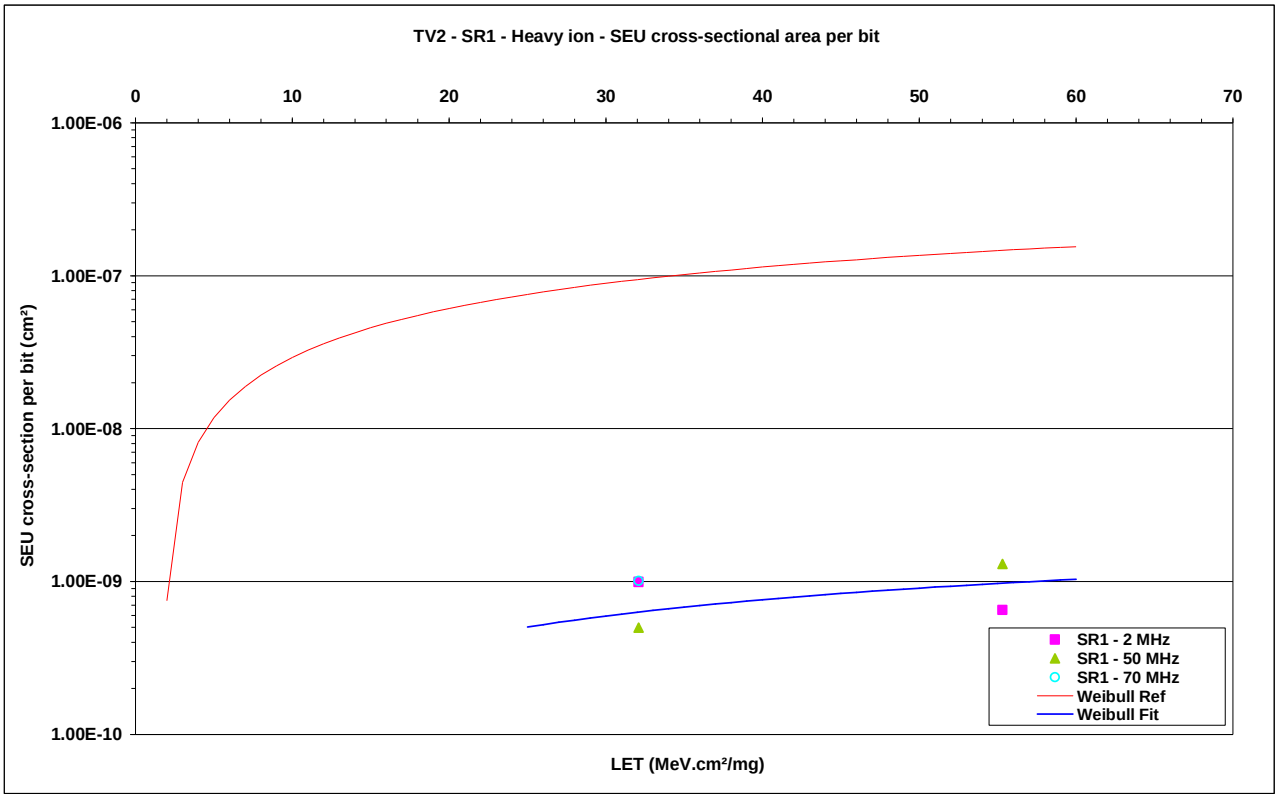


Figure 51: TV2 - SR1 - SEU cross-sectional area per bit

The Figure 52 plots the SEU distribution. More than 70 % of SEUs are SBUs and all of those are due to clear transition (transition from ‘1’ to ‘0’). The high percentage of MBUs (almost 30 %) compare to the reference channel is entirely made of arbitrary numbers of reset bits.

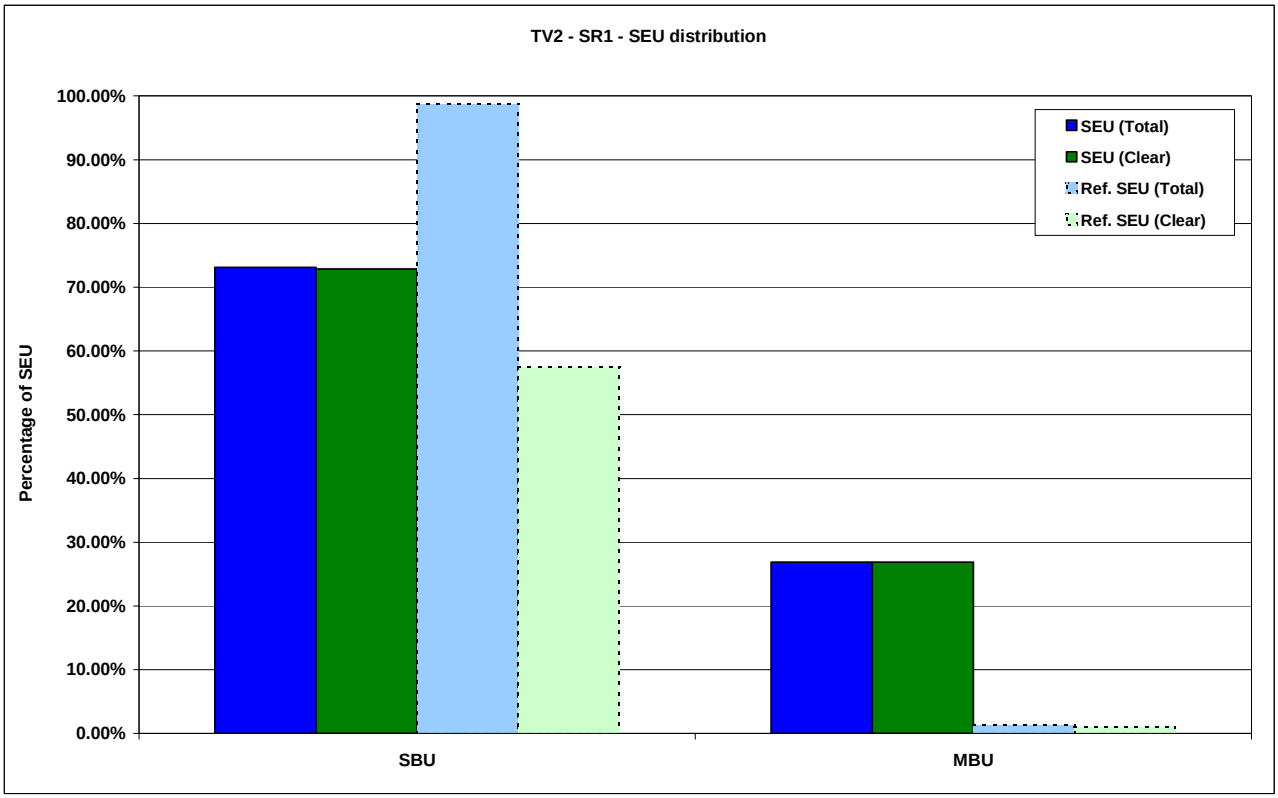


Figure 52: TV2 - SR1 - SEU distribution

The sequential cell triplication SEU mitigation seriously decreases the total amount of SEU and changes the SBU vs. MBU ratio. All events appearing on the only asynchronous global (or local) reset signal shared between all registers induced all recorded SEU without any available correction from the voter.

9.3.2 TV2 - SR2

The TV2 SR2 implemented sequential cell and I/O block triplication as SEU and SET mitigation.

The Figure 53 displays the SEU cross-sectional area per bit of this channel. The reference Weibull curve is added to the SEU cross-section graph for comparison purpose. It can be seen a small difference (less than a decade) between the channel and the reference. The SEU cross-section is characterized with an asymptotic cross-section (saturation cross-section) below 2E-7 cm² per bit and a LET threshold below 10 MeV.cm²/mg. A Weibull fit curve was estimated from the measured points and added to the cross-section graph. The Weibull fit parameters values are:

K = 1
λ = 80
Xo = 1.8 MeV.cm²/mg
CSsat = 1E-7 cm²

This SEU cross-section is high compared to the SEU cross-section of the channel using only sequential cell triplication (TV2 SR1). Because both channels use the same sequential cell triplication as SEU mitigation, a smaller (or in the worst case an equivalent) cross-section was expected on the SR2 channel. No explanation has been found yet to explain the result on this channel.

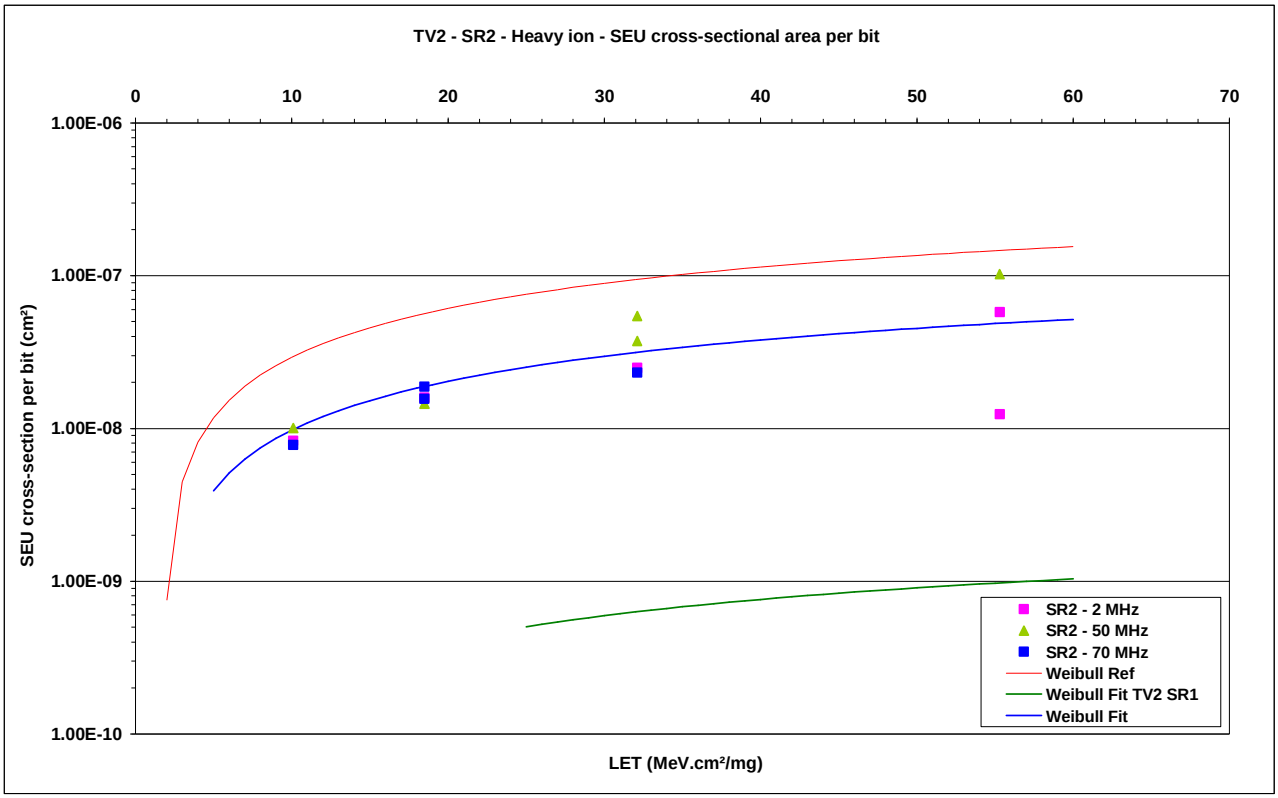


Figure 53: TV2 - SR2 - SEU cross-sectional area per bit

The Figure 54 plots the SEU distribution. 87 % of SEUs are SBUs and 83 % of those are due to clear transition. The 13 % of MBUs are made of arbitrary numbers of reset bits.

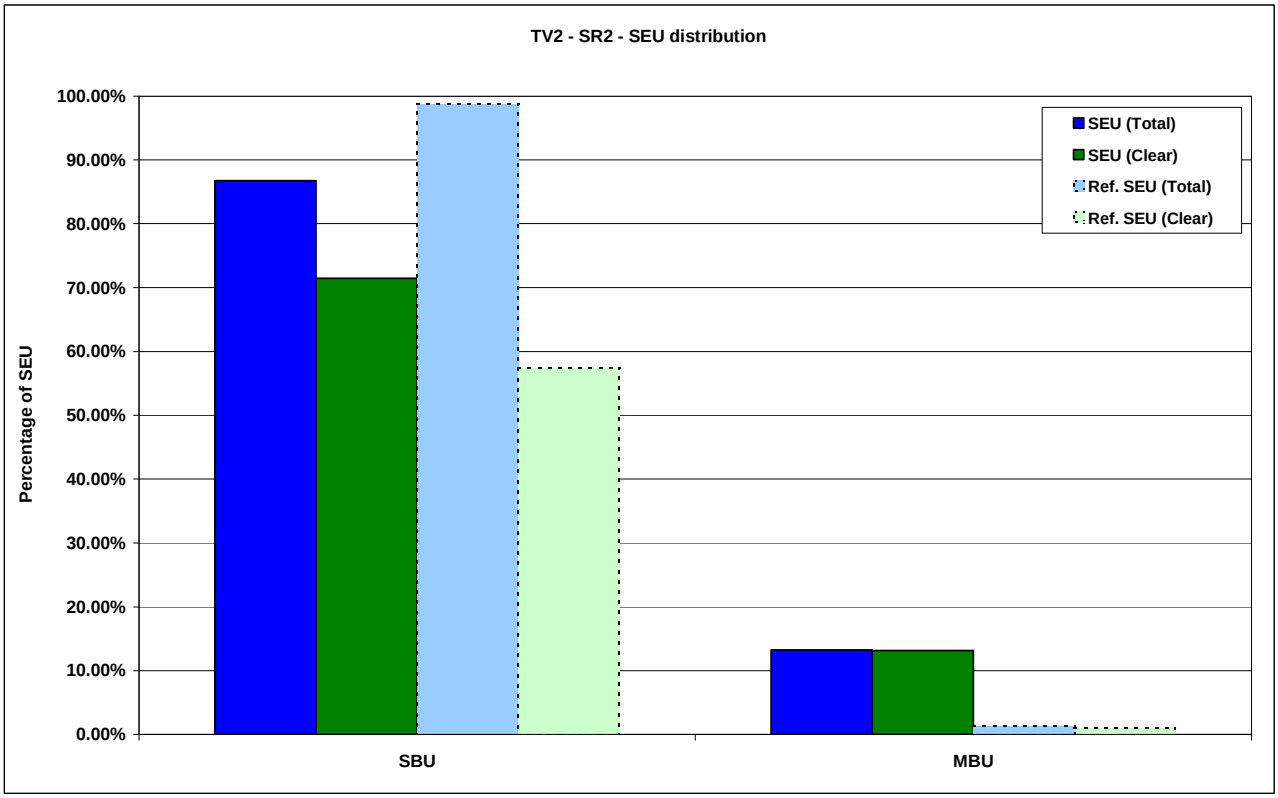


Figure 54: TV2 - SR2 - SEU distribution

9.3.3 TV2 - SR3

The TV2 SR3 implemented SET filtering with a delay of 2 ns as SET mitigation.

The Figure 55 displays the SEU cross-section of this channel. It is characterized with an asymptotic cross-section (saturation cross-section) below 3E-7 cm² per bit and a LET threshold around 1.8 MeV.cm²/mg. The reference Weibull curve was added to the graph for comparison purpose and it can be seen than the reference Weibull curve fits well the measured points of this channel.

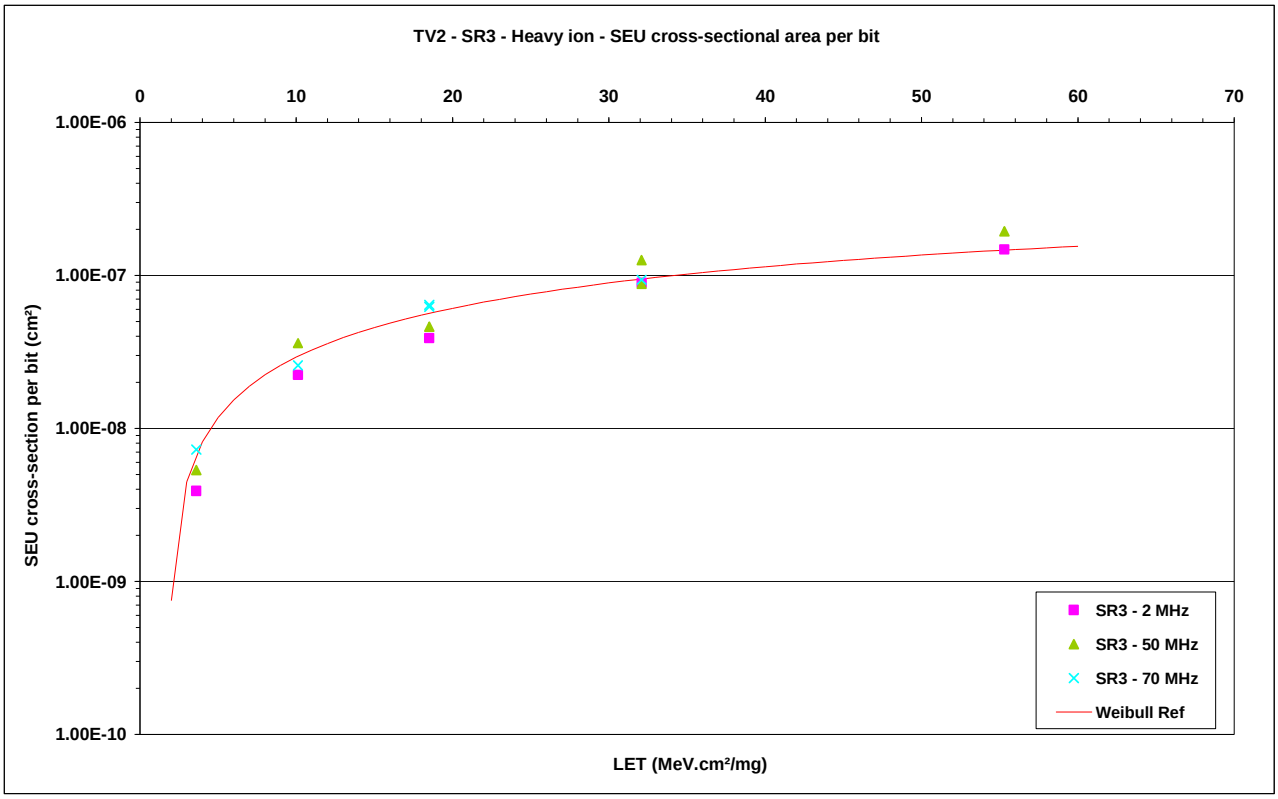


Figure 55: TV2 - SR3 - SEU cross-sectional area per bit

The Figure 56 plots the SEU distribution. Like the reference channel, most SEUs are SBUs with a little more than the half due to clear transition. MBUs counts and signatures are very similar to the reference.

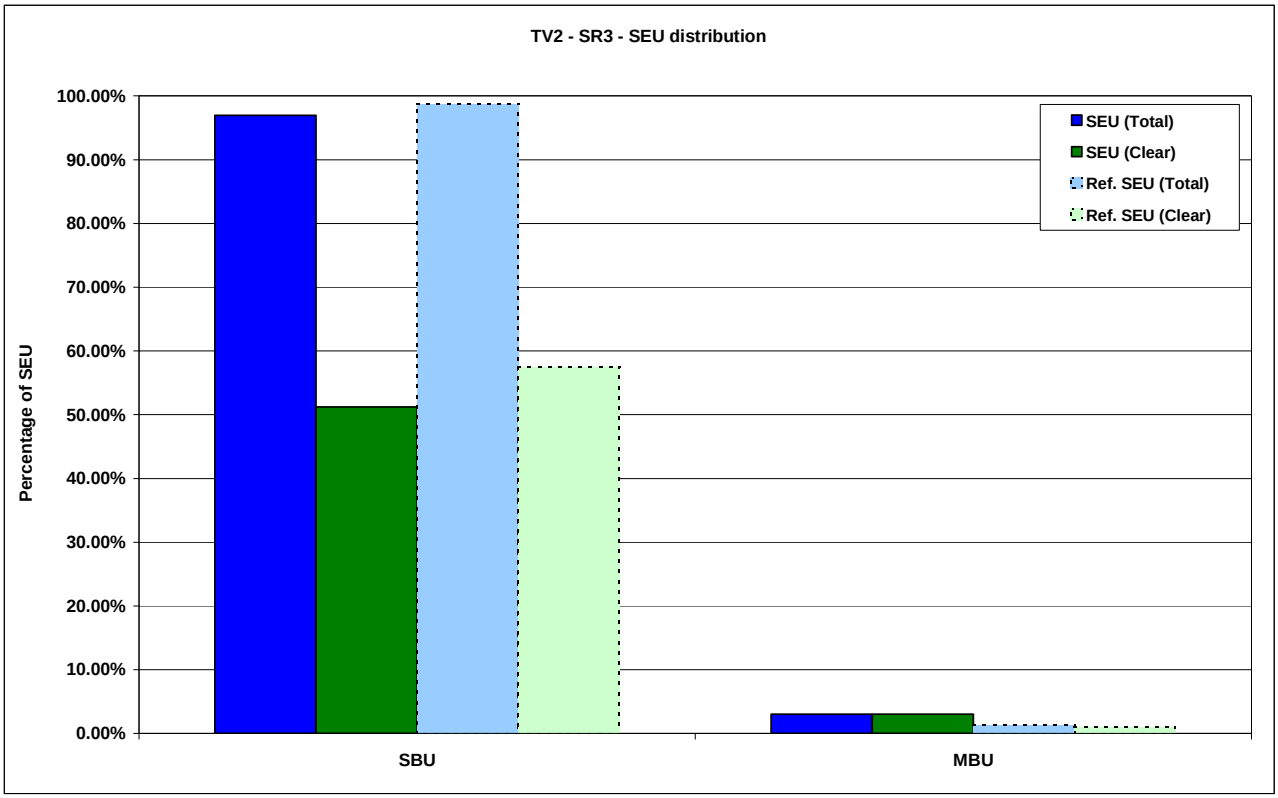


Figure 56: TV2 - SR3 - SEU distribution

9.3.4 TV2 - SR4

The TV2 SR4 implemented sequential cell and I/O block triplication as SEU mitigation and SET filtering with a delay of 3 ns as SET mitigation.

No SEE was recorded on this channel up to a LET of 55 MeV.cm²/mg and a cumulated fluence of 2E6 p/cm².

9.3.5 TV2 - SR5

The TV2 SR5 implemented sequential cell and I/O block triplication as SEU mitigation and logic duplication as SET mitigation.

No SEE was recorded on this channel up to a LET of 55 MeV.cm²/mg and a cumulated fluence of 2E6 p/cm².

9.3.6 TV2 - SR6

The TV2 SR6 implemented sequential cell and I/O block triplication as SEU mitigation and combinational cell triplication as SET mitigation. This mitigation technique is also called [full] Triple Modular Redundancy (TMR).

The Figure 57 plots the SEU cross-sectional area per bit of this channel. It is based on an extremely poor statistic because only 2 SEUs were recorded. The reference and the TV2 SR1 Weibull curves were added to the graph for comparison purpose.

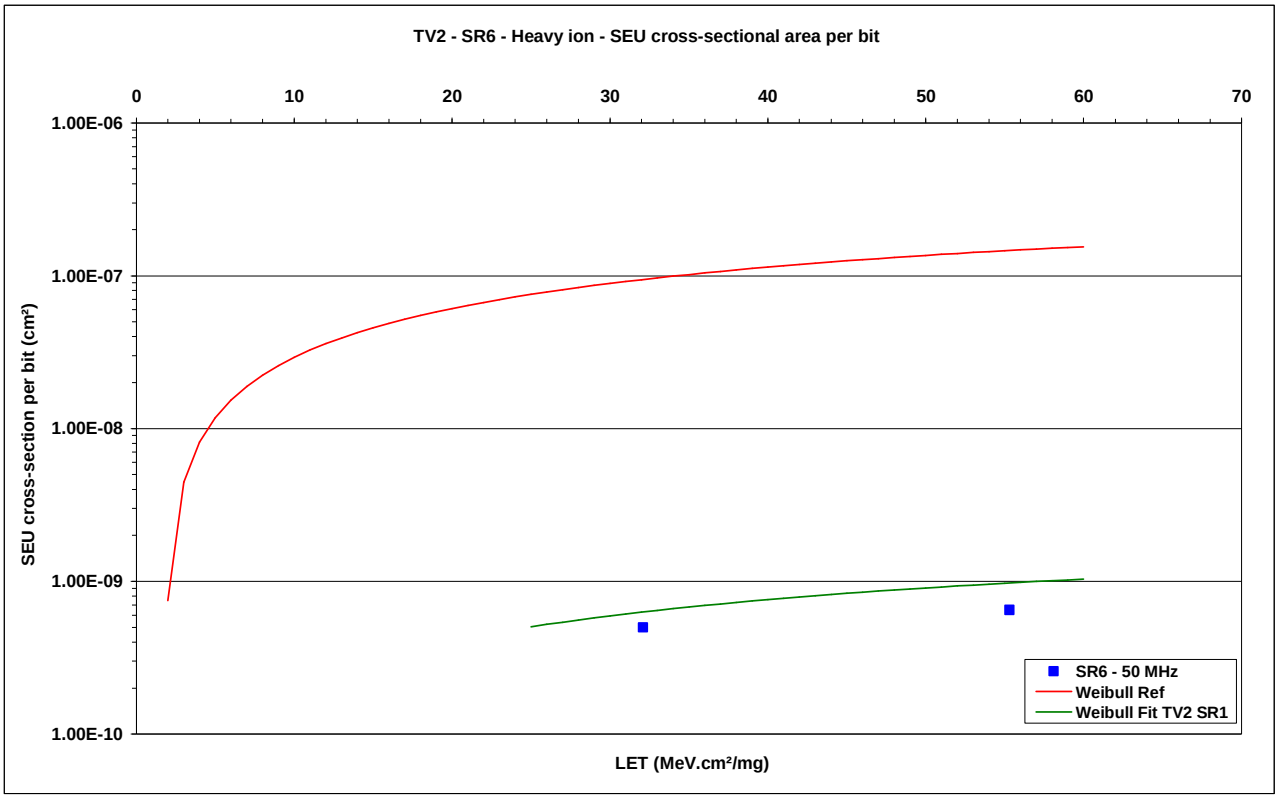


Figure 57: TV2 - SR6 - Heavy ion - SEU cross-sectional area per bit

The recorded SEUs were 2 SBUs due to clear transition.

9.4 SRAM

The SRAM SEU cross-sectional area per bit is plotted on the Figure 58. It is characterized with an asymptotic cross-section around 4E-8 cm² per bit and a LET threshold below 1.8 MeV.cm²/mg. A Weibull fit curve was estimated from the measured points and added to the graph. The Weibull fit parameters values are:

K = 1
λ = 22.5
Xo = 0.2 MeV.cm²/mg
CSsat = 4E-8 cm²

As a remark, all test conditions (dynamic, static and Flash Freeze) fit well to the estimated SEU cross-section.

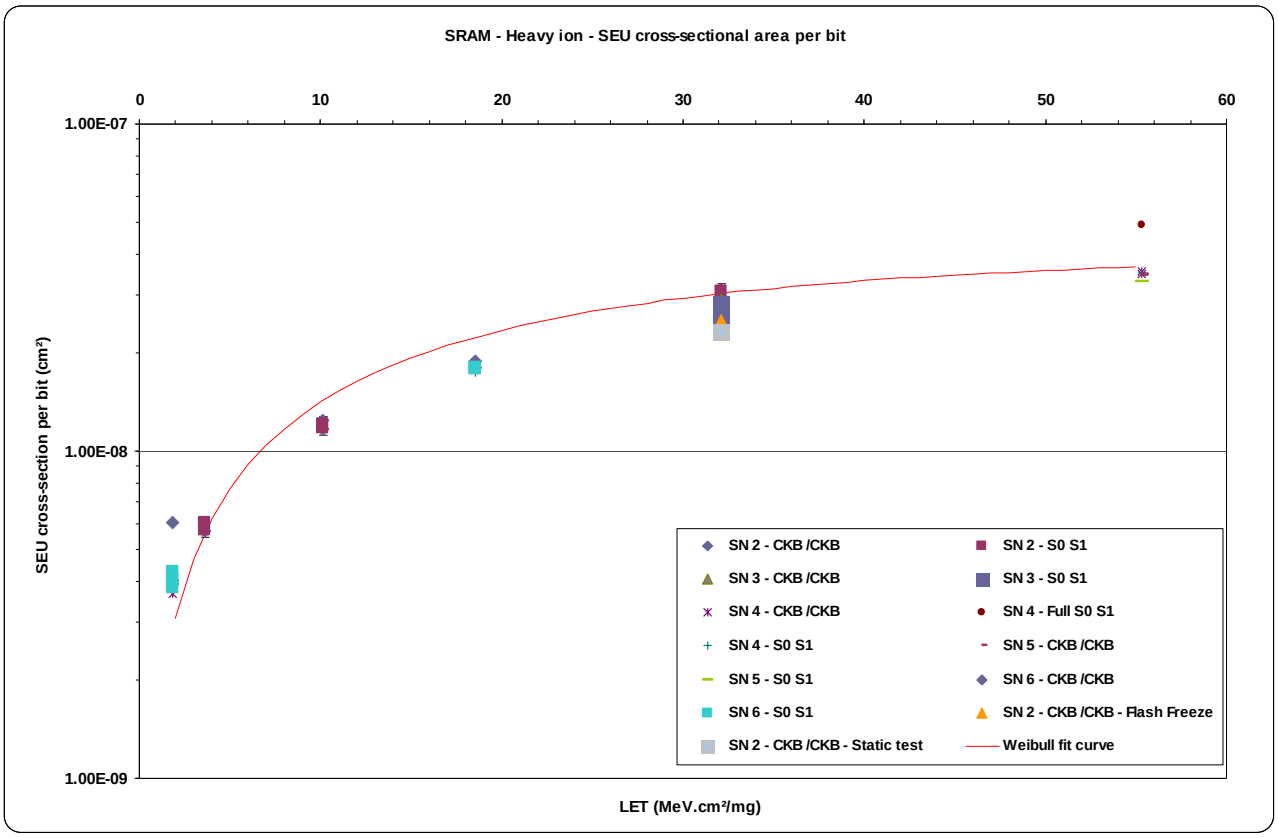


Figure 58: SRAM - SEU cross-sectional area per bit

As highlighted on the Figure 59 all SRAM errors are SEUs (checking type 2 - upset while checking process). The Table 10 summarizes the available error types (see paragraph 8.3 for further details). The Figure 60 shows the very large majority of errors are SBU. The Figure 61 displays the very well balanced distribution of SEU vs. the erroneous bit position inside the word. By averaging the data of all bits it can be stated than:

- ✓ 47 % of SEU errors are set bit while 53 % are reset bit (clear bit) (see Figure 62).
- ✓ 47 % of SEU errors are located on the north side while 53 % are on the south side (see Figure 63).

The north side and south side error counts are close. The small difference between the counts can also be originated from the variation of the homogeneity of the beam on the large distance between the opposite sides of the die.

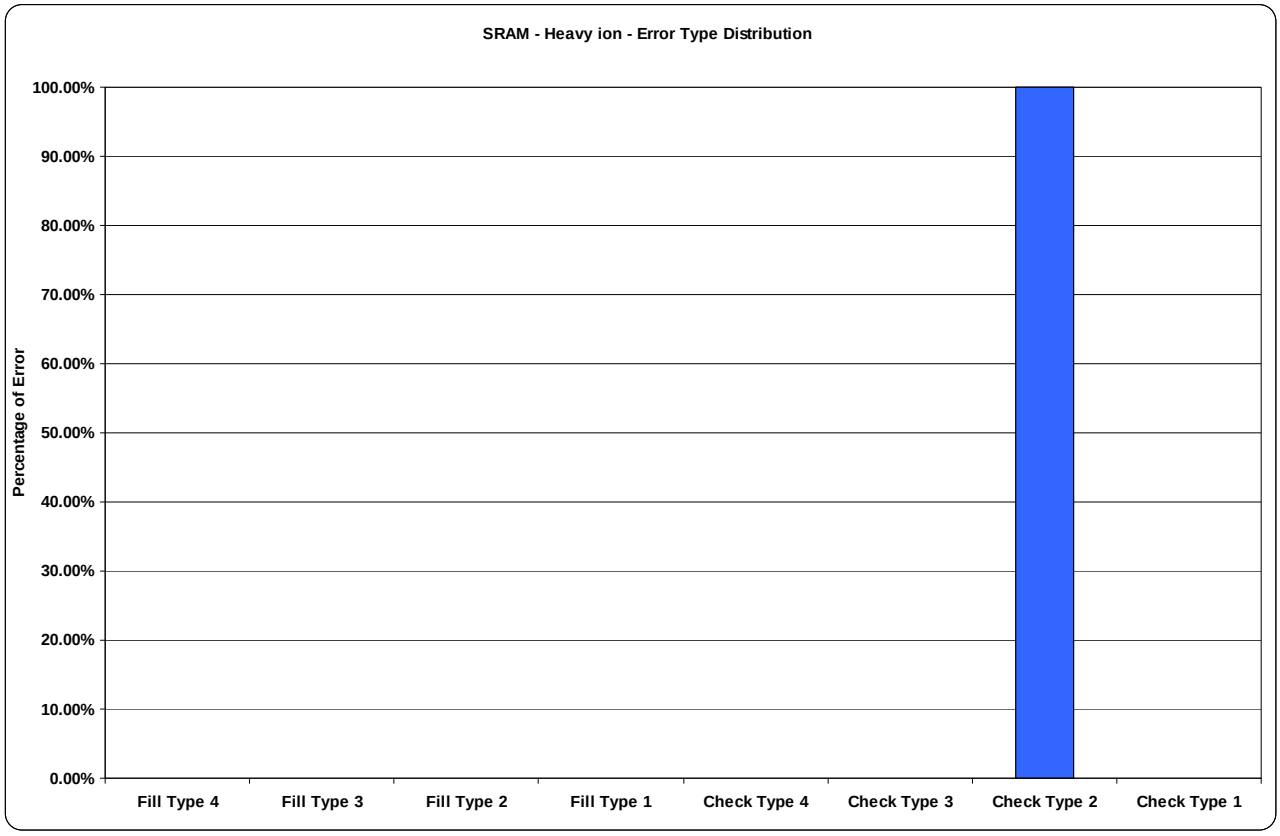


Figure 59: SRAM - Error type distribution

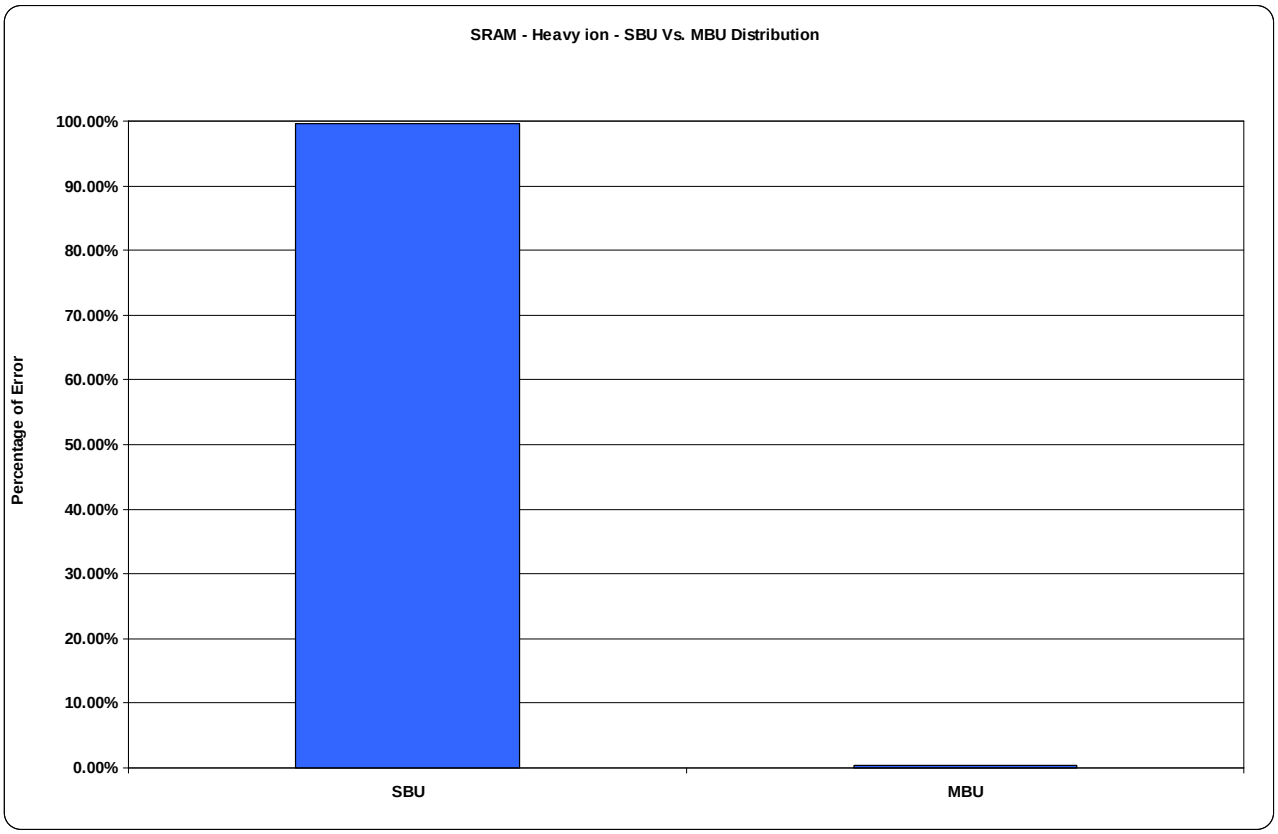


Figure 60: SRAM - SBU vs. MBU distribution

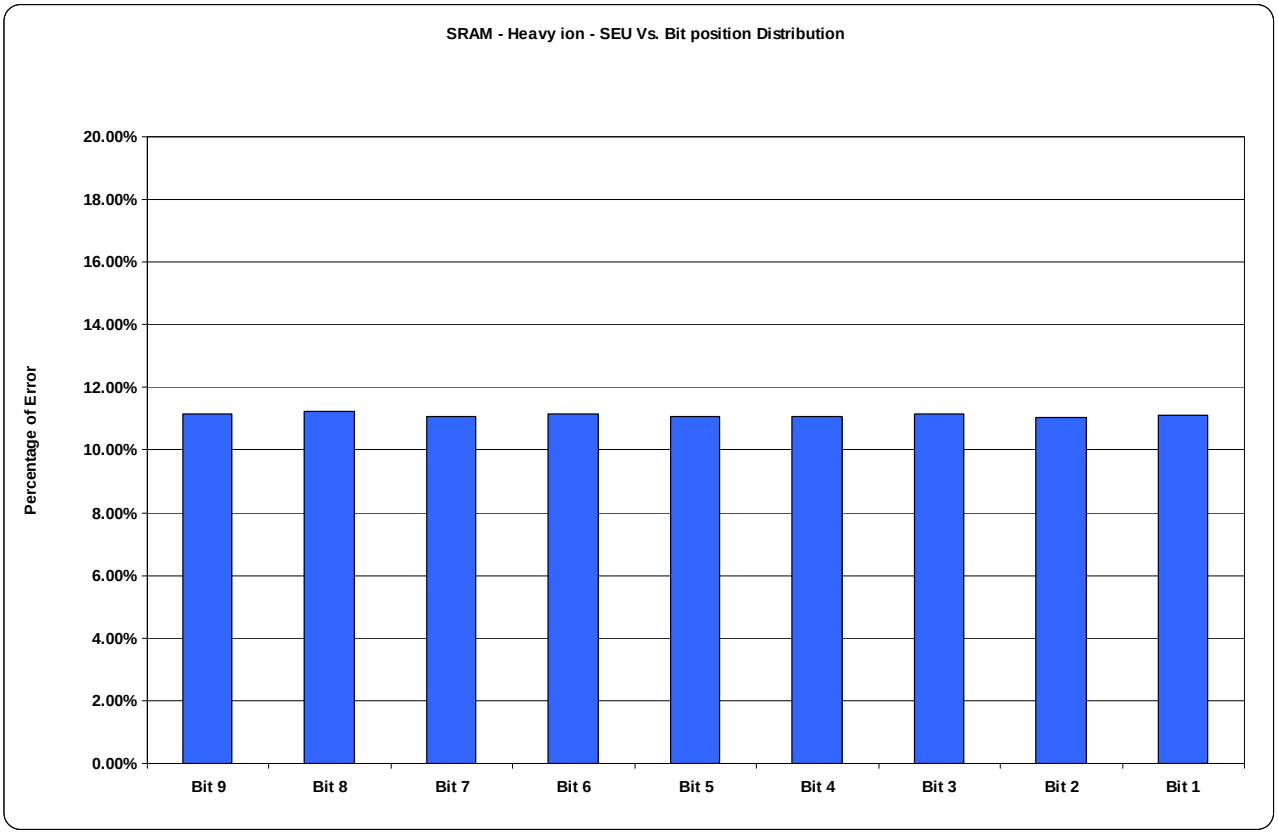


Figure 61: SRAM - SEU vs. Bit position distribution

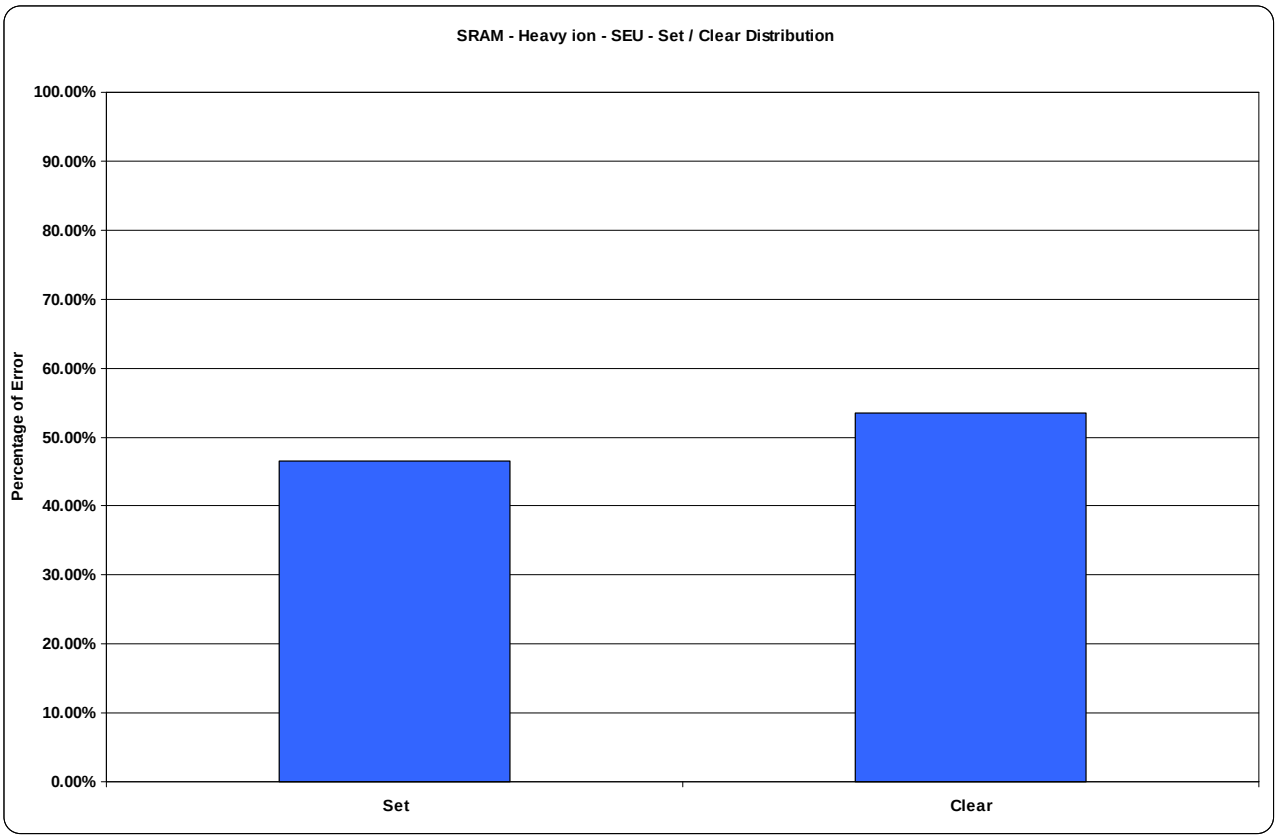


Figure 62: SRAM - SEU - Set / Clear distribution

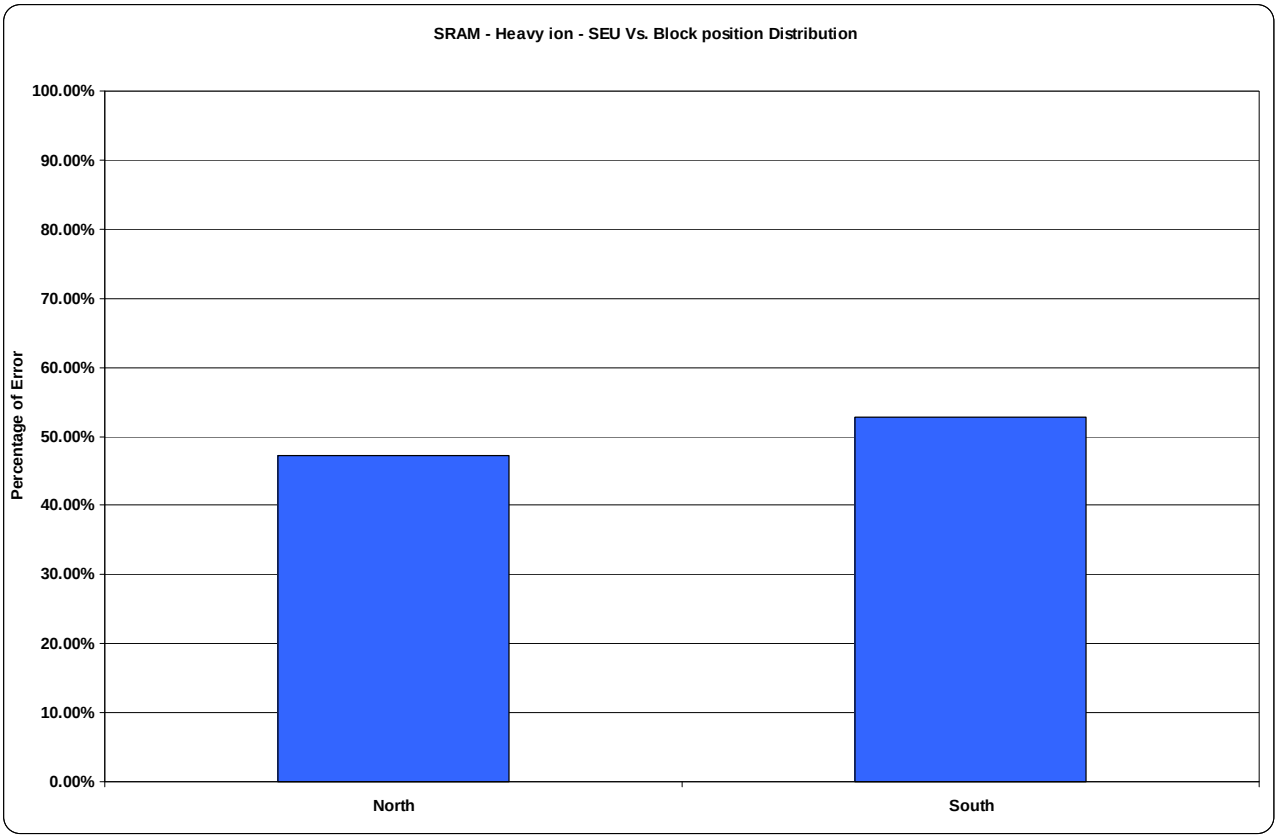


Figure 63: SRAM - SEU vs. Block position distribution

9.5 UFROM

No error was observed (neither recorded) on the UFROM up to a LET of 55 MeV.cm²/mg ($^{131}Xe^{35+}$) and a total cumulated fluence of 1.36E7 p/cm².

9.6 CCC/PLL

Like the reference channel, most SEUs on the shift register channels clocked by the PLL output clock are SBUs with more than half coming from clear transition. MBUs signatures are the same as the reference channel. It was not seen a total flip or stuck bit of the channels' outputs that could lead to a total or partial stop of the PLL output clock: the PLL output clock never stopped.

The PLL lock signal however is sensitive to Large Error (here below called PLL lock signal SEFI) and to SET. One PLL lock signal SEFI event was counted each time an error appeared on the PLL lock signal and the PLL did not recover by itself. The recovering process was made using a power cycle. On the other way, the error was counted as an SET each time the PLL recovered by itself.

4 PLL lock signal SEFIs were recorded on the PLL lock signal under the following conditions:

SEFI #	1	2	3	4
Frequency (MHz)	100	150	150	100
LET (MeV.cm²/mg)	32.1	32.1	18.5	18.5
Conditions	RADEF - June 2010 - RUN 22	RADEF - June 2010 - RUN 66	RADEF - June 2010 - RUN 101	RADEF - June 2010 - RUN 121
Fluence (p/cm²)	5E5	1E6	1E6	1E6

Table 13: CCC/PLL - PLL lock signal SEFI conditions

No PLL lock signal SEFI was recorded under the nominal condition.

The PLL lock signal SET cross-sectional area is plotted on the Figure 64. This SET cross-section is based on poor statistic attended to the small number of errors. Three Weibull fit curves from 3 different input frequencies (200, 150 and 100 MHz) were more or less well estimated from the measured points and added to the graph. It can be seen than the frequency influences the SET sensitivity. Because the PLL was set on a static mode to a nominal frequency of 200 MHz, increasing the gap between the nominal frequency and the working frequency increased the SET sensitivity. In nominal condition, the CCC/PLL lock signal SET cross-section is characterized with an asymptotic cross-section below 1E-5 cm² and a LET threshold around 1.8 MeV.cm²/mg. The nominal Weibull fit curve has the following parameters values:

K = 1
λ = 160
Xo = 1.8 MeV.cm²/mg
CSsat = 1E-5 cm²

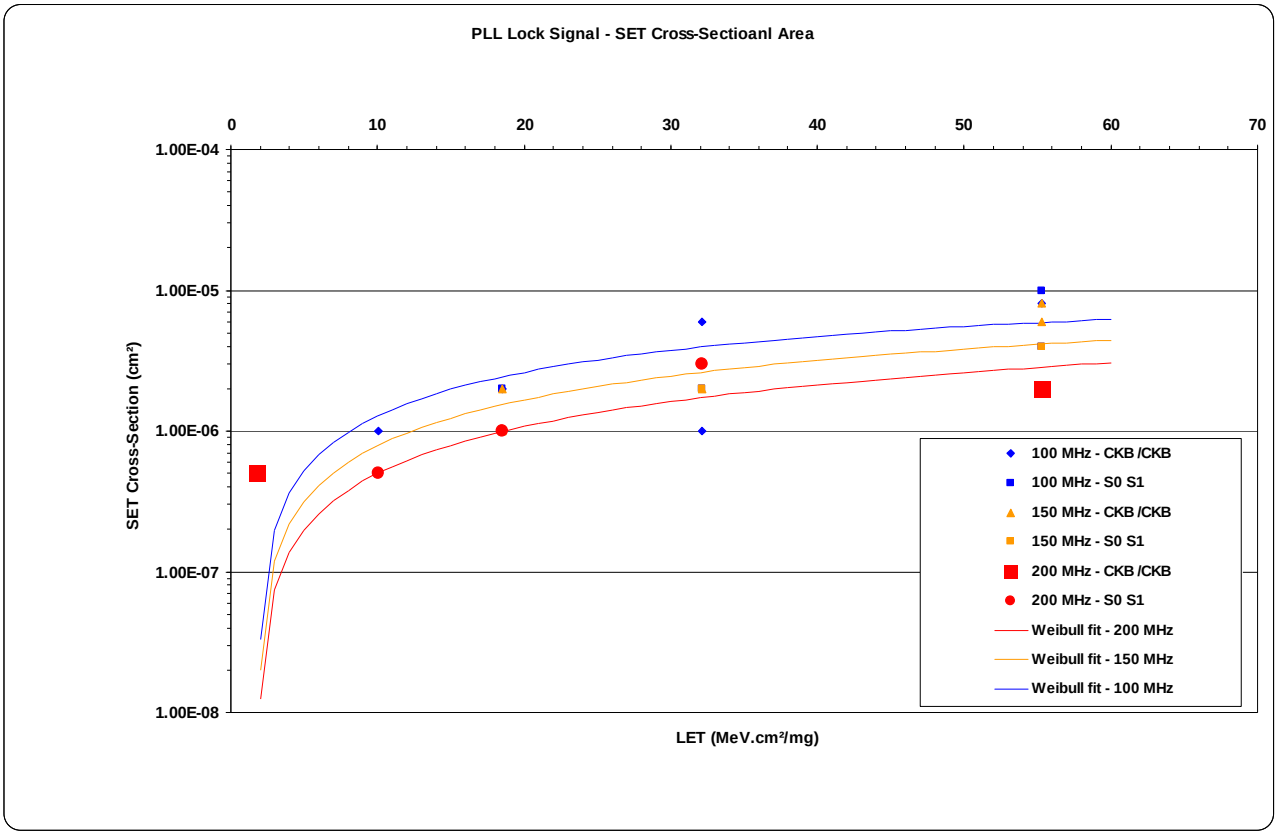


Figure 64: PLL Lock signal - SET cross-sectional area

9.7 CONFIGURATION FLASH, CHARGE PUMP & IN SYSTEM PROGRAMMING

The configuration flash is not sensitive to SEE. However the programming part of the configuration flash is sensitive to SEU, SHE and to the cumulated dose deposited by the cumulated fluence.

The following processes of the device configuration were run under beam exposition to check the sensitivity and can be stated to be sensitive to SEE.

- ✓ Erasing
- ✓ Programming
- ✓ Verifying

The processes were tested all together and separately on the beam. The success of the process, the functionality of the design and the re-configurability of such configured devices was then verified (once or twice) off beam.

The following Table 14 summarizes the status of the samples.

Few remarks have to be made on the Table 14:

i. All status are stated from functionality of the design and the re-configurability of the sample. The failing of the re-configuration was generally verified by repeating the operation.
ii. The dose (the status) after configuration test is the dose (the status) of the sample at the end of the last configuration test run performed under the beam. Additional runs (to test other parts of the device) can be performed on the same sample after the last configuration test run.
iii. The status after SEE test is the status of the sample at the end of the test campaign.
iv. The final dose is the total dose received by the sample.
v. The final status is the status of the sample stated at the end of all tests. All samples were checked in August 2011 (5 months after the last campaign).

From this Table 14, it can be seen than:

- Over the 6 samples tested in configuration mode:
  - ✓ All were the source of SEUs inducing failures in the programming process. An off beam re-configuration was then successfully completed and the functionality of the design successfully verified.
  - ✓ 2 samples (SN 3 and SN 16) were the source of SHE during the configuration of the sample and were so destructed.
  - ✓ 1 sample (SN 5) was stated as fail (not configurable anymore) at the end of the heavy ion test (November 2010). It received a cumulated dose of 21 KRad. The same sample was then stated as pass (fully functional and re-configurable) at the end of all tests (August 2011).
- The influence of the cumulated dose deposited by the cumulated fluence can also be seen on the sample SN 4. This sample was not used to test the configuration process, but the cumulated dose of this sample (29 KRad) at the end of the heavy ion test (November 2010) damaged its configuration system. The sample did not recover and was still failing (design functional but sample not re-configurable) at the end of all tests (August 2011).
- 3 samples (SN 8, 10 and 11) failed the re-configuration verification right after the heavy ion test. However they all passed (fully functional and re-configurable) the day after.

SN	Beam Nature	Configuration test	SEU	SHE	Dose (after configuration test) (Rad)	Status (after configuration test)	Status (after SEE test)	Status (after SEE test + 1 day)	Final Dose (Rad)	Final status
1	Heavy Ions				na	na	Pass	Pass	0.00E+00	Pass
2	Heavy Ions	X	X		1.43E+04	Pass	Pass	Pass	1.43E+04	Pass
3	Heavy Ions	X	X	X	6.57E+03	Fail	Fail	Fail	6.57E+03	Fail
4	Heavy Ions				na	na	not verified	Fail	2.89E+04	Fail
5	Heavy Ions	X	X		1.21E+04	Pass	Fail	Fail	2.09E+04	Pass
6	Heavy Ions	X	X		5.00E+03	Pass	Pass	Pass	5.00E+03	Pass
7	Heavy Ions				na	na	Pass	Pass	0.00E+00	Pass
8	Heavy Ions				na	na	Fail	Pass	2.84E+03	Pass
9	Heavy Ions				na	na	Pass	Pass	1.61E+02	Pass
10	Heavy Ions				na	na	Fail	Pass	1.92E+03	Pass
11	Heavy Ions				na	na	Fail	Pass	1.00E+04	Pass
12	Heavy Ions				na	na	Pass	Pass	0.00E+00	Pass
13	Heavy Ions				na	na	Pass	Pass	0.00E+00	Pass
14	Heavy Ions				na	na	Pass	Pass	0.00E+00	Pass
15	Heavy Ions				na	na	Pass	Pass	0.00E+00	Pass
16	Heavy Ions	X	X	X	3.20E+03	Fail	Fail	Fail	3.20E+03	Fail
17	Heavy Ions	X	X		1.05E+03	Pass	Pass	Pass	1.05E+03	Pass
18	Heavy Ions				na	na	Pass	Pass	0.00E+00	Pass
19	Proton				na	na	Pass	Pass	2.94E+04	Pass
20	Proton				na	na	Pass	Pass	1.65E+04	Pass
21	Proton				na	na	Pass	Pass	4.41E+03	Pass
22	Proton				na	na	Pass	Pass	0.00E+00	Pass
23	Proton				na	na	Pass	Pass	0.00E+00	Pass
24	Proton				na	na	Pass	Pass	0.00E+00	Pass

Table 14: Samples status

10 PROTON - TEST RESULTS

10.1 POWER SUPPLY

No SEL has been observed up to an energy of 230 MeV, a cumulative fluence of 6.36E11 p/cm², a room temperature, a bias voltage of 1.5 V for the core voltage and 3.3 V for the input/output voltage.

10.2 TV1 - SHIFT REGISTER

10.2.1 TV1 - SR1

Due to the low proton sensitivity of the D core flip-flop (register) a large fluence was needed and a large dose was so deposited on the samples at each run: this limiting the characterization. As a consequence, only 230 MeV energy was used. The SEU cross-section per bit plotted on the Figure 65 is below 1E-13 cm² at 230 MeV.

In the purpose to increase the proton SEU cross-section statistics, the total number of register composing the shift registers on the design could be increased. However this would have requested the usage of another design including a higher number of register inside each shift register or the modification of the requirements of the original test vehicle.

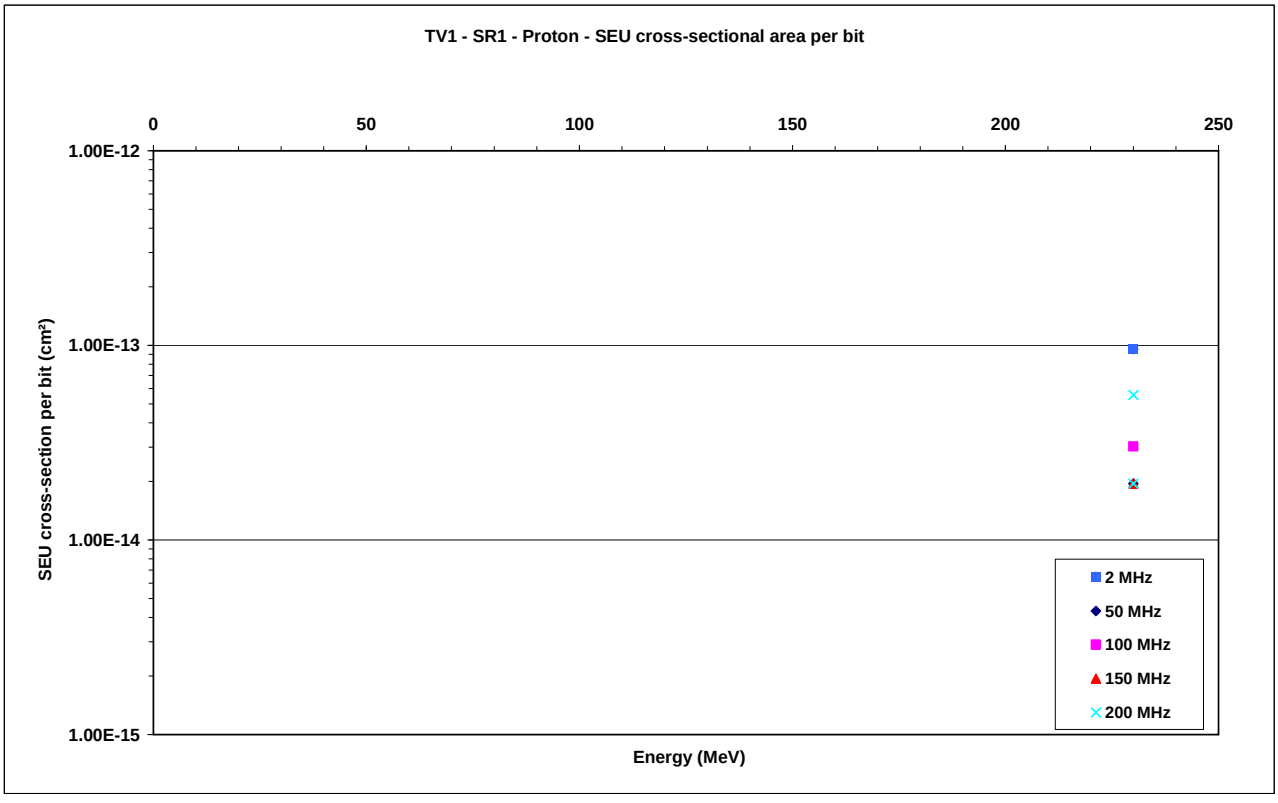


Figure 65: TV1 - SR1 - SEU cross-sectional area per bit

10.2.2 TV1 - SR2

The SEU cross-section per bit plotted on the Figure 66 is the same as the reference below 1E-13 cm² at 230 MeV.

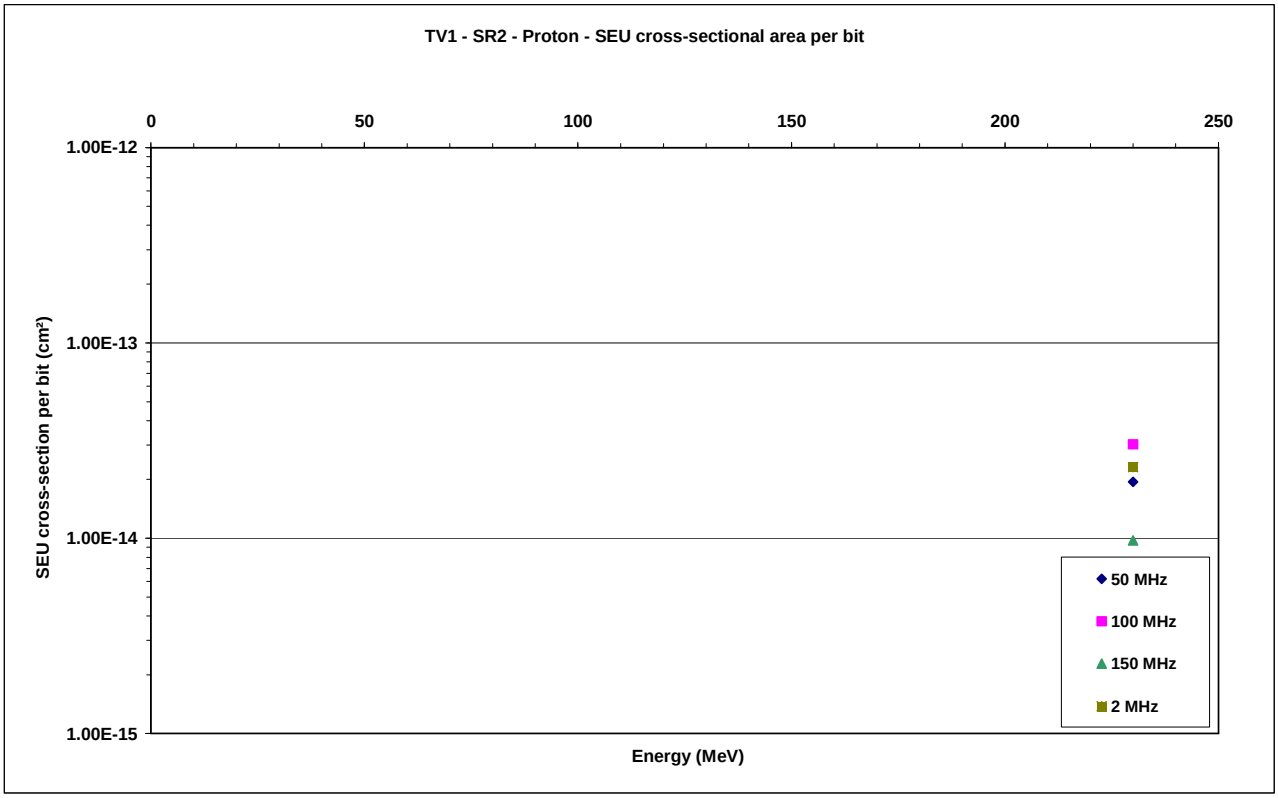


Figure 66: TV1 - SR2 - SEU cross-sectional area per bit

10.2.3 TV1 - SR3

The SEU cross-section per bit plotted on the Figure 67 is similar to the reference channel below 1E-13 cm² at 230 MeV.

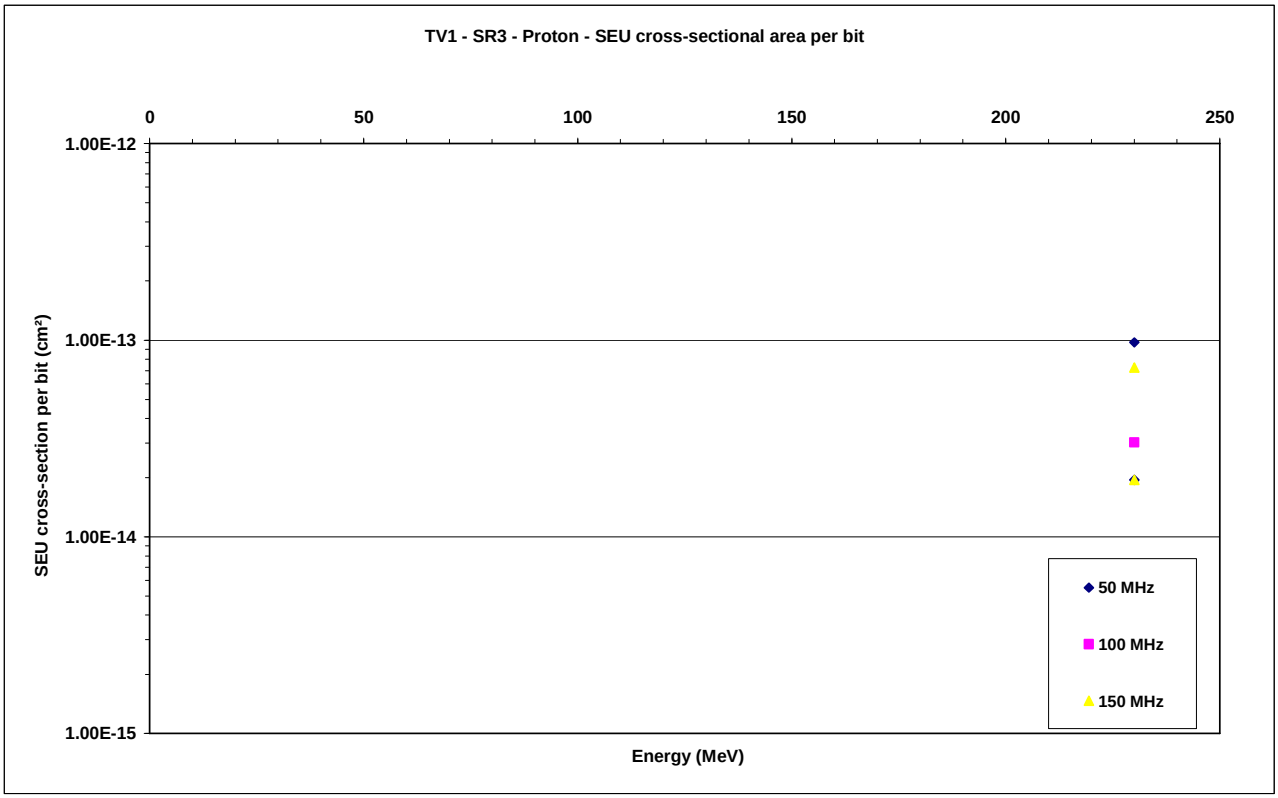


Figure 67: TV1 - SR3 - SEU cross-sectional area per bit

10.2.4 TV1 - SR4

The SEU cross-section per bit plotted on the Figure 68 is similar to the reference channel below 1E-13 cm² at 230 MeV.

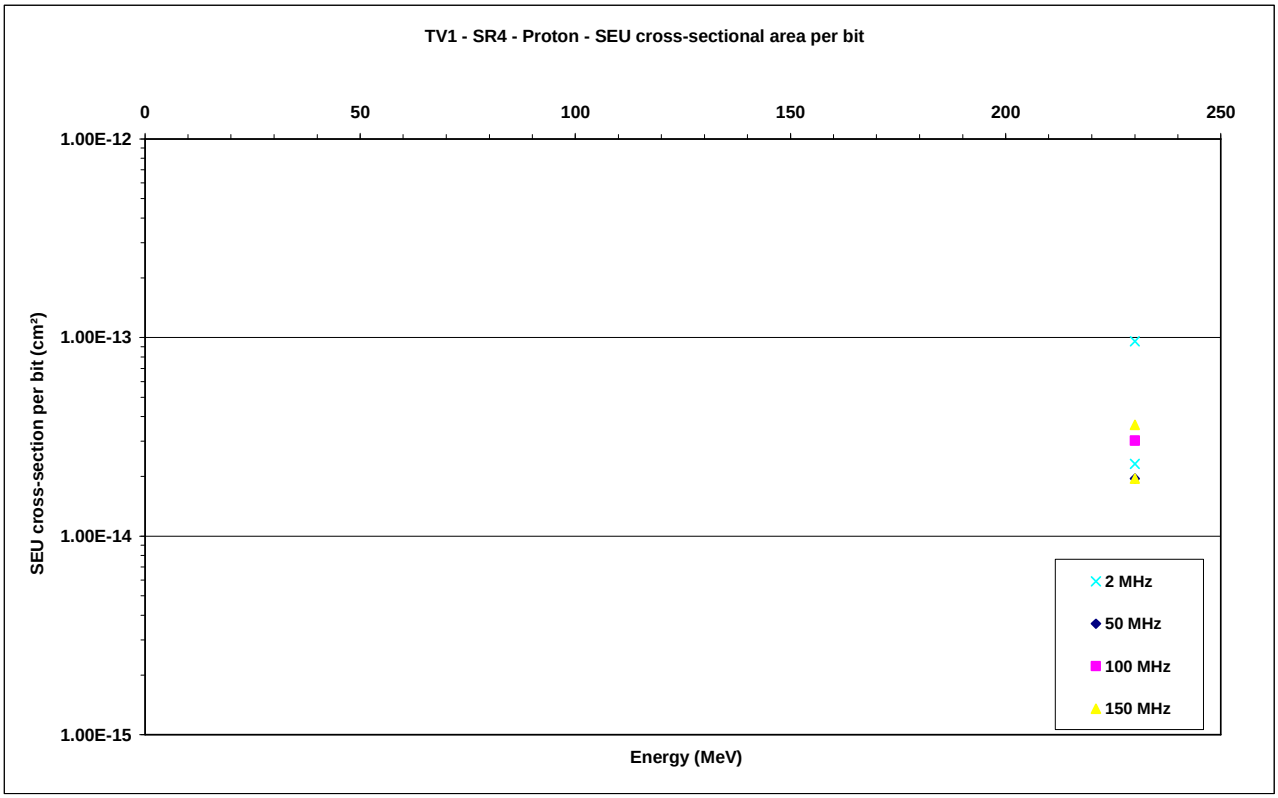


Figure 68: TV1 - SR4 - SEU cross-sectional area per bit

10.2.5 TV1 - SR5, 6, 7 and 8

The SEU cross-section per bit plotted on the Figure 69 is similar to the reference channel below 1E-13 cm² at 230 MeV.

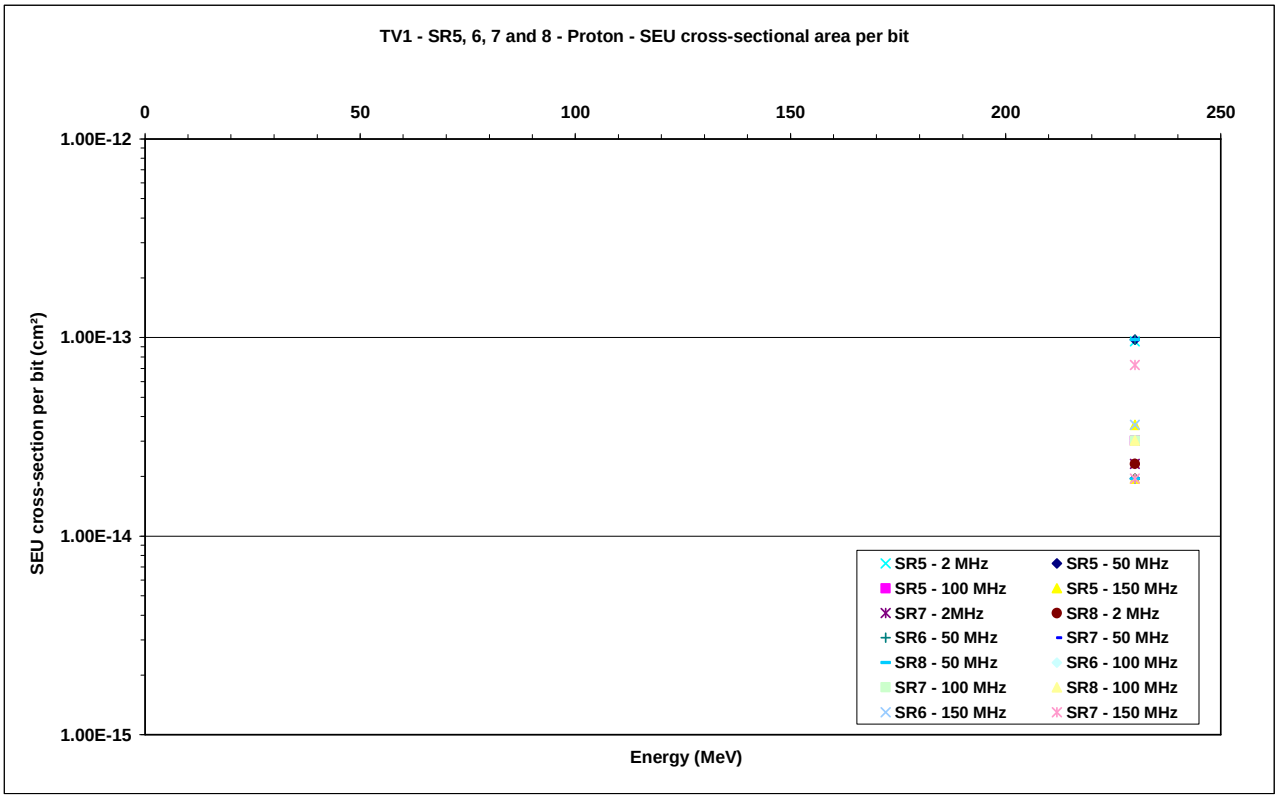


Figure 69: TV1 - SR5, 6, 7 and 8 - SEU cross-sectional area per bit

10.2.6 TV1 - SR9 and 10

The SEU cross-section per bit plotted on the Figure 70 is similar to the reference channel below 1E-13 cm² at 230 MeV.

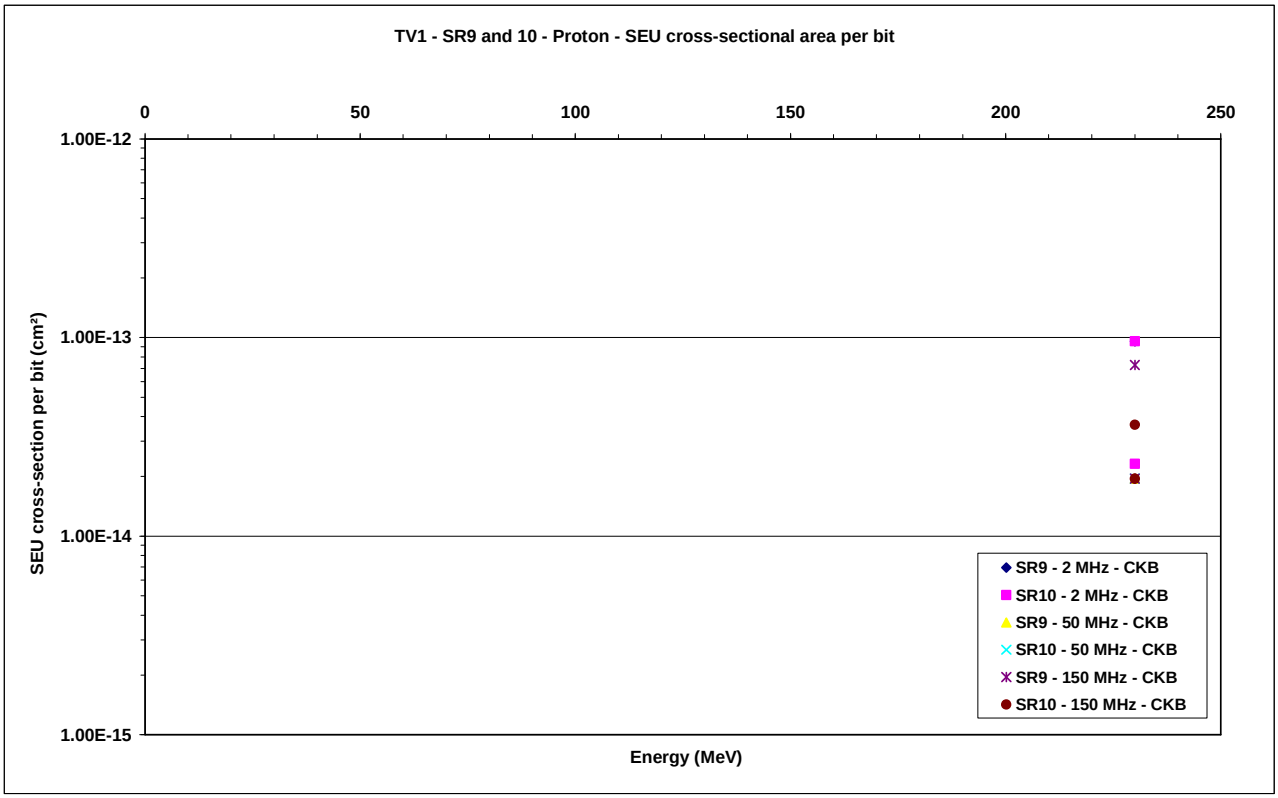


Figure 70: TV1 - SR9 and 10 - SEU cross-sectional area per bit

10.2.7 TV1 - SR11, 12, 13 and 14

Those channels were not tested to proton.

10.3 TV2 - SHIFT REGISTER

Due to the poor number of SEE recorded on the TV2 during heavy ion tests and the low proton sensitivity of registers of the TV1, the TV2 was not tested to proton.

10.4 SRAM

The SRAM SEU cross-sectional area per bit is plotted on the Figure 71. It is characterized with an asymptotic cross-section below 1E-13 cm² per bit and an energy threshold below 23.5 MeV.

One sample was used to fully characterize the SRAM at several energies while a second sample was used on 2 energies to verify. The 2 samples points are very likely.

Only the dynamic mode was used as test condition.

As highlighted on the Figure 72 all SRAM errors are SEUs (checking type 2 - upset while checking process). The Table 10 summarizes the available error types (see paragraph 8.3 for further details). The Figure 73 shows than the very large majority of errors are SBU. The Figure 74 displays the well balanced distribution of SEU vs. the erroneous bit position inside the word. By averaging data of all bits it can be stated than:

- ✓ 58 % of SEUs are set bit while 42 % are clear bit (reset bit) (see Figure 75).
- ✓ 50 % of SEUs are located on the north side while 50 % are on the south side (see Figure 76).

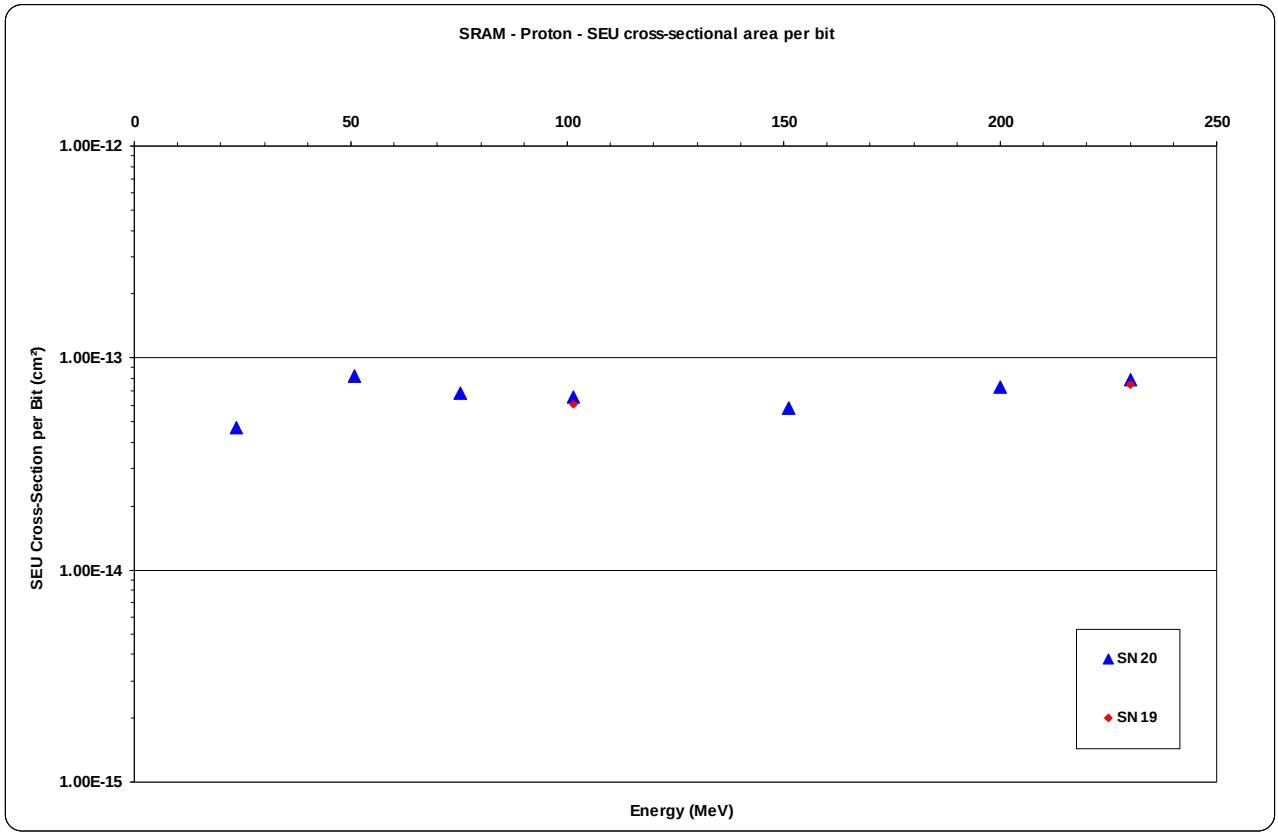


Figure 71: SRAM - SEU cross-sectional area per bit

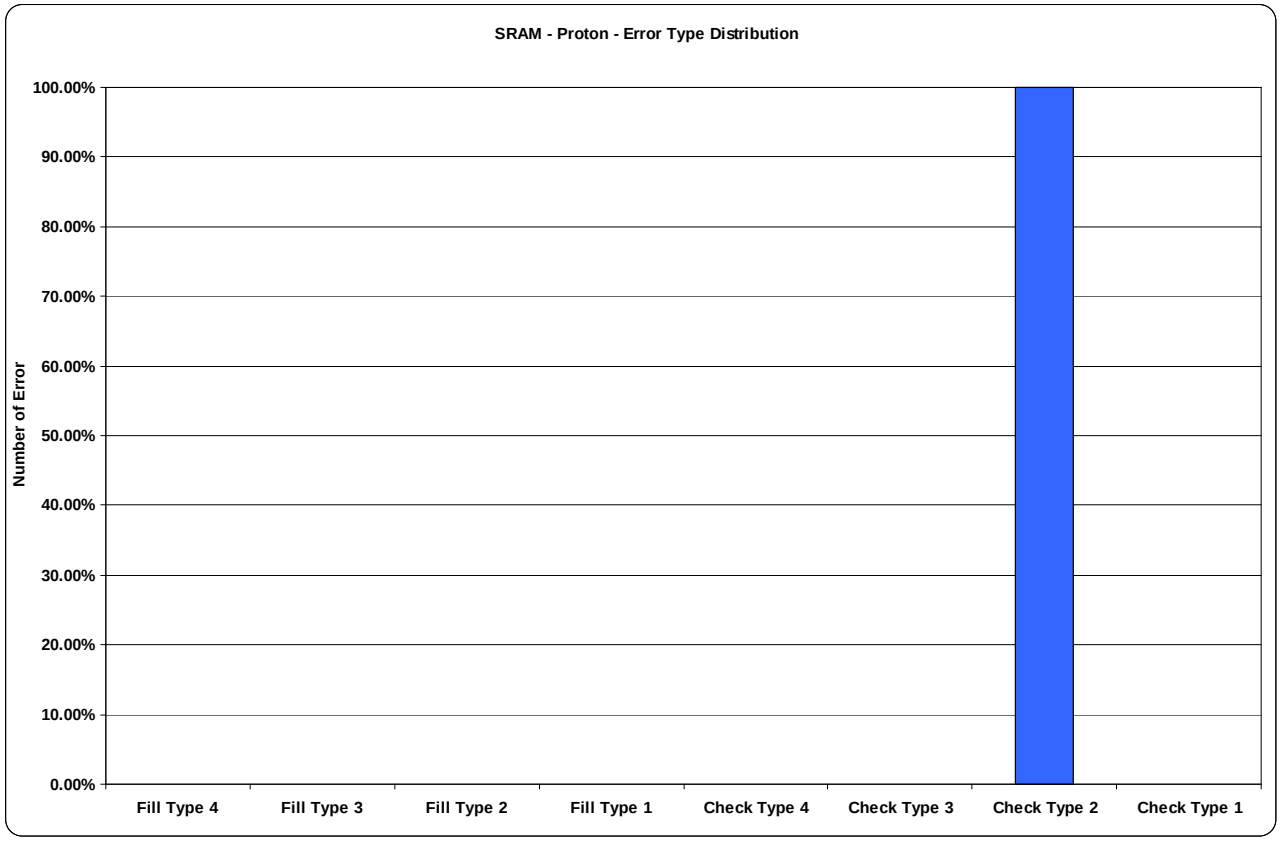


Figure 72: SRAM - Error type distribution

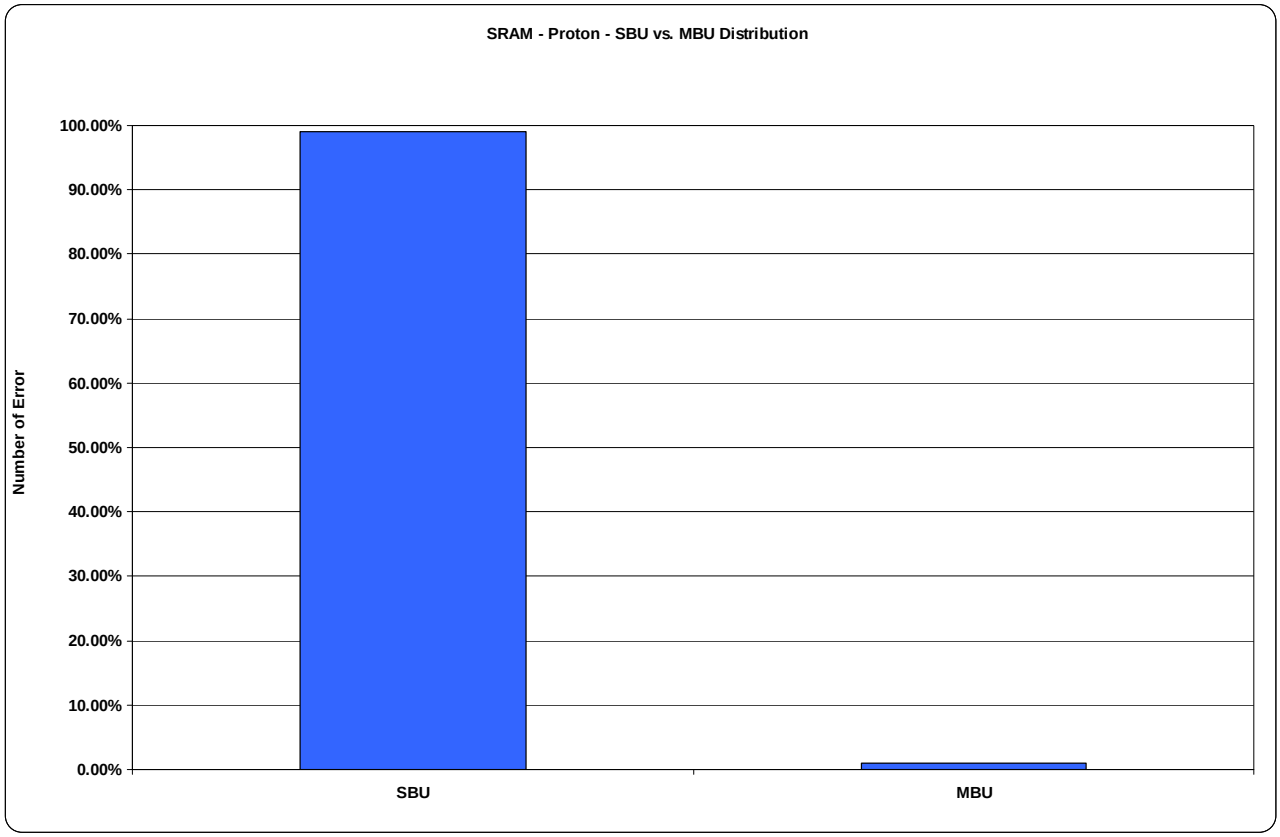


Figure 73: SRAM - SBU vs. MBU distribution

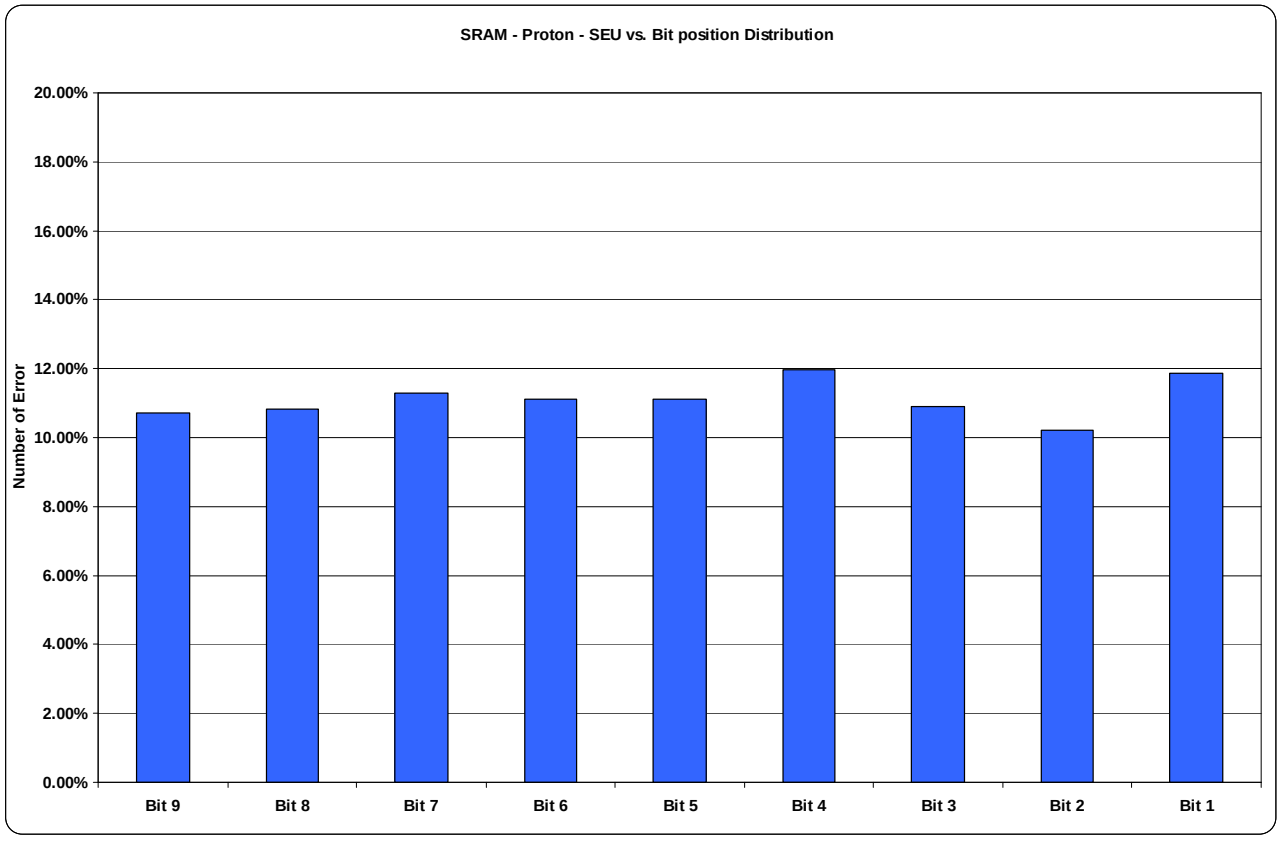


Figure 74: SRAM - SEU vs. Bit position distribution

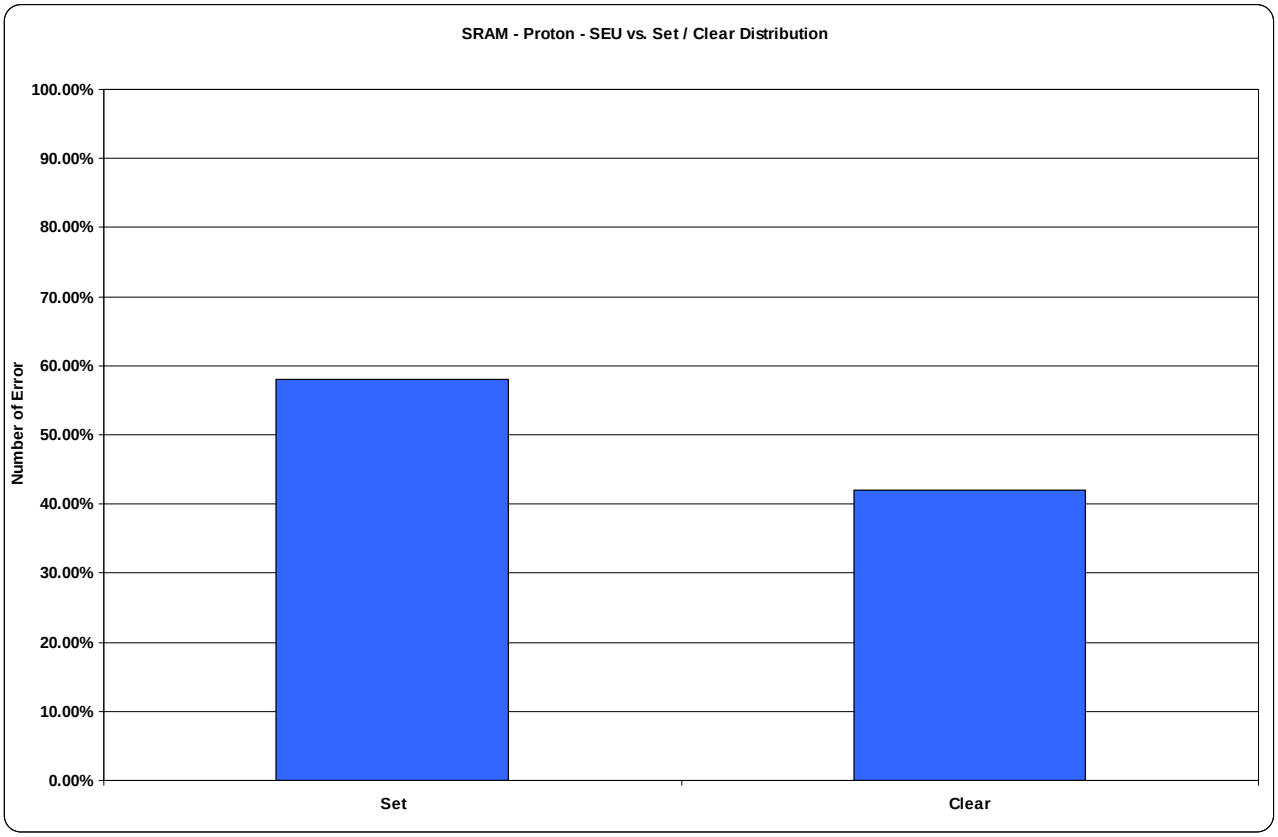


Figure 75: SRAM - SEU - Set / Clear distribution

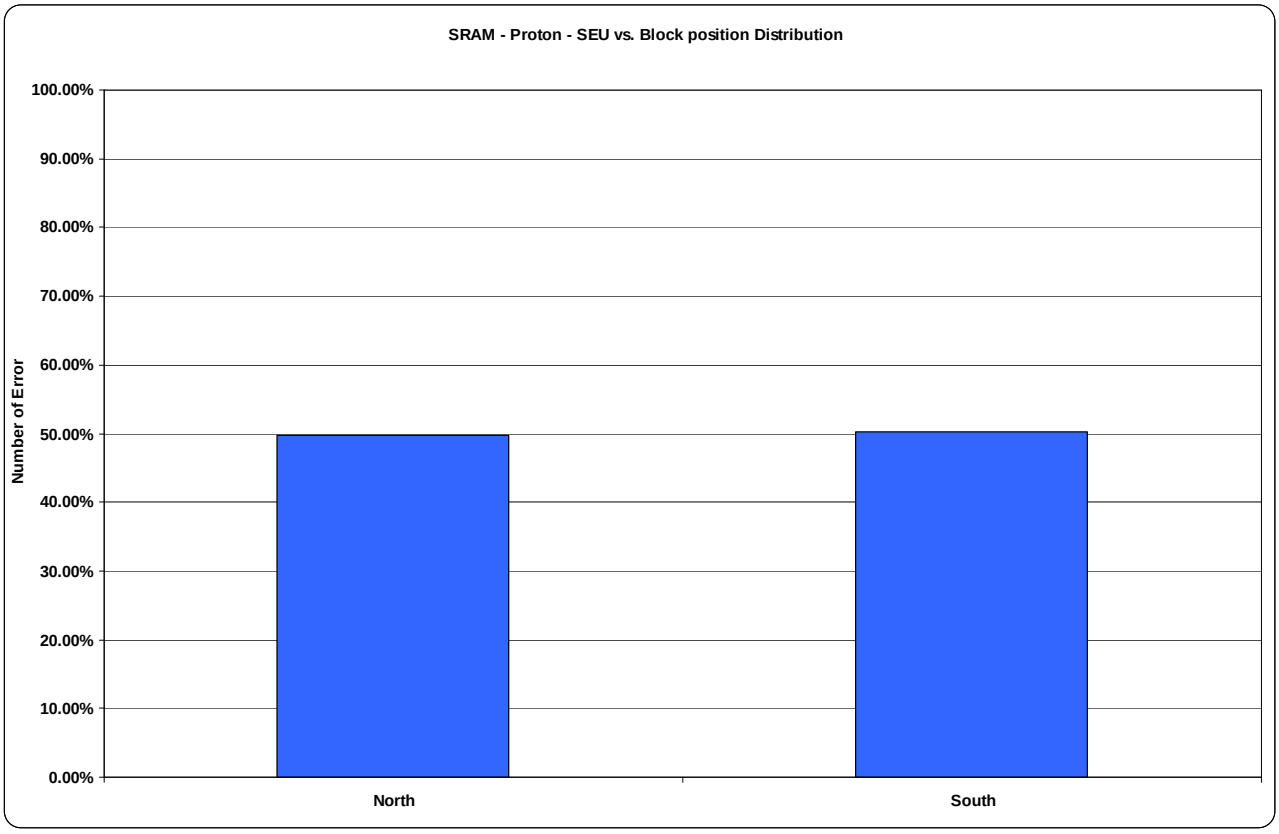


Figure 76: SRAM - SEU vs. Block position distribution

10.5 UFROM

No error was observed (neither recorded) on the UFROM up to an energy of 230 MeV and a total cumulated fluence of 2.03E10 p/cm².

10.6 CCC/PLL

The channels clocked by the PLL output clock were not tested to proton. Neither was the CCC/PLL block.

10.7 CONFIGURATION FLASH, CHARGE PUMP & IN SYSTEM PROGRAMMING

The configuration flash is not sensitive to SEE. No additional run was performed with proton to evaluate the sensitivity of the programming part of the configuration flash.

11 CONCLUSION

The A3PE3000L flash FPGA from the ProASIC3L family from ACTEL manufacturer was SEE characterized at the following facilities under ESA ESTEC contract number 22327/09/NL/SFE:

- ✓ RADEF, University of Jyväskylä, Jyväskylä, Finland in June and November 2010.
- ✓ PIF, PSI, Villigen, Switzerland in March 2011.

SEE mitigation methods applied on the same die were also characterized and their SEE sensitivities evaluated. 2 test vehicles (TV) were designed and tested. The first TV implemented 14 shift registers, one clock conditioning circuit with phase-locked loop and 100 % of the SRAM and UFROM memories. The second TV implemented SEU and SET mitigation on 6 shift registers. All shift registers of both TVs were made of 1024 registers made of D core flip-flop with clear and enable active high.

No SEL was observed up to a LET of 55 MeV.cm²/mg, a cumulated fluence of 1E7 p/cm², a temperature up to 125 °Celsius and a bias voltage of 1.65 Volts for the core voltage and 3.6 Volts for the input/output voltage.

The flash (configuration and user) was not seen sensitive to SEE up to a LET of 55 MeV.cm²/mg. It remained intact. However the programming part of the flash was stated sensitive to SEU, SHE and to the cumulated dose deposited by the cumulated fluence.

One SEFI was detected and recorded during the campaign at RADEF on November 2010 on the RUN 112 with an effective LET of 55 MeV.cm²/mg. The device was configured with the TV2 and all shift registers were tested with a working frequency of 2 MHz. From the Iteration N° 257 (a fluence of 3.69E5 p/cm²) up to the end of the run (a fluence of 5E5 p/cm²) all the read data from the device were read at the low state (“0”). The device did not recover from the SEFI state by itself. The recovery took place after a power cycle of the device allowing the next run with the exact same conditions to be performed without any more SEFI detected.

Concerning the shift registers:

- ✓ The reference and standard shift register (TV1 - SR1) SEU cross-section is characterized with an asymptotic cross-section below 3E-7 cm² per bit and a LET threshold below 1.8 MeV.cm²/mg. An extremely light influence of the working frequency can be seen on the SEU cross-section. Most errors are SBUs where almost 2/3 is due to clear transition. Some MBUs largely made of arbitrary numbers of consecutive reset bits (clear bit) were counted as well.
- ✓ The channel implementing combinational cells on the enable signal path (TV1 - SR2) results in an SEU cross-sectional area per bit similar to the reference. The frequency does not appear to influence the SEU cross-section or so lightly than it is not visible on the cross-section curve. Most errors are SBUs with more than half due to clear transition. MBUs are made of errors with the same signatures than the reference channel. However another signature shows un-shifted quartets caused by an SET on the enable signal caught at the active edge of the clock: data are held from shifting. Very few SETs on the enable signal were caught that way.
- ✓ The channel implementing combinational cells on the reset signal path (TV1 - SR3) results in a SEU cross-sectional area per bit characterized with an asymptotic cross-section below 1E-6 cm² and a LET threshold around 1.8 MeV.cm²/mg. This SEU cross-section per bit is higher than the reference. Almost 80% of SEUs are SBUs and 70% of those are due to clear transition. There is a high count of MBU compared to the reference channel and almost all of those are due to arbitrary numbers of reset bits.
- ✓ The channel implementing combinational cells in-between each register (TV1 - SR4) results in an SEU cross-sectional area per bit similar to the reference. A very light influence of the working frequency can be seen on the SEU cross-section. Most SEUs are SBUs and 2/3 of those are due to clear transition. Comparing SEU cross-section and error signatures, this channel seems very similar to the reference one.
- ✓ The channels implementing the DDR I/O registers (TV1 - SR5 to 8) and the channels implementing LVDS buffers (TV1 - SR9 and 10) show a SEU cross-sectional area per bit very similar to the reference. SEE signatures are also like the references ones.
- ✓ The channels clocked by the PLL output clock (TV1 - SR11 to 14) have a SEU cross-sectional area per bit identical to the reference. Most SEUs are SBUs with more than half due to clear transition. MBUs are largely attended to reset bits and flipped bits: it was not seen a total flip or stuck bit of the channels that could lead to a total or partial stop of the PLL output clock.

- ✓ The channel implementing sequential cell triplication (TV2 - SR1) results in a SEU cross-sectional area per bit characterized with an asymptotic cross-section below 2E-9 cm². There is a large difference (around 2 decades) on its SEU cross-section and the reference one. It is based on a poor statistic attended to the small number of errors. More than 70 % of SEUs are SBUs and all of those are due to clear transition. The high percentage of MBU (almost 30 %) compared to the reference channel is made of arbitrary numbers of reset bits. The sequential cell triplication SEU mitigation decreases the total amount of SEU and changes the SBU vs. MBU ratio. All events appearing on the only asynchronous global (or local) reset signal shared between all registers induced all recorded SEU without any available correction from the voter.
- ✓ The channel implementing sequential cell triplication and I/O bank triplication (TV2 - SR2) has a SEU cross-sectional area per bit characterized with an asymptotic cross-section below 2E-7 cm² and a LET threshold below 10 MeV.cm²/mg, lower than the reference but still higher than the channel implementing only sequential cell triplication. This result seems unrealistic compared to the other channels implementing only the sequential cell triplication (TV2 SR1). Because both channels use the same sequential cell triplication as SEU mitigation, a smaller (or in the worst case an equivalent) cross-section was expected on the SR2 channel. No explanation has been found yet to explain the result on this channel.
- ✓ The channel implementing the SET filtering method with a delay of 2 ns (TV2 - SR3) has a SEU cross-sectional area per bit similar to the reference. Its SEEs signatures are also very like the reference channel.
- ✓ The channel implementing sequential cell triplication, I/O block triplication and SET filtering with a delay of 3 ns (TV2 - SR4) did not show any event up to a LET of 55 MeV.cm²/mg and a cumulated fluence of 2E6 p/cm².
- ✓ The channel implementing sequential cell triplication, I/O block triplication and logic duplication (TV2 - SR5) did not show any event up to a LET of 55 MeV.cm²/mg and a cumulated fluence of 2E6 p/cm².
- ✓ The channel made of full TMR mitigation (TV2 - SR6) was the source of only 2 SBUs (single bit cleared). Based on an extremely poor statistic this channel look close to the result of the channel implementing only sequential cell triplication (TV2 - SR1).
- ✓ All the channels of the TV1, expected the channels clocked with the PLL output clock were tested to proton. They all have the same proton SEU cross-section per bit measured from a low sensitivity (with a low number of errors) below 1E-13 cm² at 230 MeV.

The SRAM heavy ion SEU cross-sectional area per bit is characterized with an asymptotic cross-section around 4E-8 cm² per bit and a LET threshold below 1.8 MeV.cm²/mg. The SRAM proton SEU cross-sectional area per bit is characterized with an asymptotic cross-section below 1E-13 cm² and an energy threshold below 23.5 MeV. All SEEs are upsets with a very large majority of SBUs very well balanced on bit position, on set / clear transitions and on RAM block position.

The PLL output clock never stopped. However the PLL lock signal is sensitive to PLL lock signal SEFI and to SET. It can be seen than the frequency influences those sensitivities. Because the PLL was set on a static mode to a nominal frequency of 200 MHz, increasing the gap between the nominal frequency and the working frequency increased those sensitivities. In nominal condition no any PLL lock signal SEFI was recorded on the PLL lock signal while its SET cross-sectional area based on a poor statistic attended to the small number of errors is characterized with an asymptotic cross-section below 1E-5 cm² and a LET threshold around 1.8 MeV.cm²/mg.

Few remarks have to be made:

- ✓ The sequential cell and I/O block triplication mitigation methods were used on the channels 2, 4, 5 and 6 of the TV2. The yet unexplained phenomenon that influences the 2^{sd} channel does not influence the channel 4, 5 and 6.
- ✓ TMR shift registers have a higher percentage of MBU compared to SBU than the non-mitigated shift registers.
- ✓ In the purpose to increase the SEU cross-section statistics, the total number of D core flip-flop (register) on the TV1 design could be increased. However this would have requested the usage of another TV1 design (including a higher number of register inside each shift register) or the modification of the requirements of the original test vehicle.
- ✓ The performance of the SET filtering method can only be evaluated if the SET sensitivity is evaluated (measured).
- ✓ The clock synchronization of global signals (seen on enable signal) highly reduces the probability to catch SETs appearing on the same global signals. Synchronizing the reset (clear) signal should so very probably decrease the sensitivity of SEUs induced by the SET on the global reset (clear) signal.

- ✓ The test of I/O blocks (I/O buffers and registers) would be characterized to SEE sensitivity with higher accuracy by being tested lonely instead of mixed with other parts.
- ✓ The usage of SERDES module would have been of great help during the design of the shift register test system. However requiring the output and the acquisition of the 4 last registers' output for all shift registers made it impossible. The high working frequency of SERDES system and the single data line would have greatly eased the high frequency access and the data line compensation.

12 RADEF – JUNE 2010 – RUN TABLES

12.1 RUN / BEAM / DUT / SEL - TABLES

	RUN				BEAM										DUT								
Line #	Date	Run #	JYFL Run #	Start Time	Ion specie	Energy (MeV)	LET (MeV/(mg/cm²))	Range (Si) (µm)	Tilt (Deg)	LETeff. (MeV/(mg/cm²))	Fluence (p/cm²)	Run Duration (s)	Mean flux (p/(cm².s))	Run dose (Rad)	SN	Total Dose (Rad)	TV	Temperature (°C)	Vcore (V)	Vio (V)	Mode	Exposition Time (s)	SEL
6	28/06/2010	-	1	11:30	82Kr22+	768	32	94	0	32.1	1.43E+04	1498	9.55E+00	7.34E+00	0	0	B	room=40	-	-	-	-	-
7	28/06/2010	6	2	12:02	82Kr22+	768	32	94	0	32.1	2.92E+04	296	9.86E+01	1.50E+01	5	12028.6	1p	room=40	1.5	3.3/2.5	Static	-	0
8	28/06/2010	7	3	12:10	82Kr22+	768	32	94	0	32.1	2.90E+04	292	9.93E+01	1.49E+01	5	12043.49	1p	room=40	1.5	3.3/2.5	Static	-	0
9	28/06/2010	8	4	12:24	82Kr22+	768	32	94	0	32.1	1.51E+04	159	9.50E+01	7.76E+00	5	12051.25	1p	room=40	1.5	3.3/2.5	Static	-	0
10	28/06/2010	9	5	12:33	82Kr22+	768	32	94	0	32.1	8.12E+03	90	9.02E+01	4.17E+00	5	12055.42	1p	room=40	1.5	3.3/2.5	Static	-	0
11	28/06/2010	10	6	12:40	82Kr22+	768	32	94	0	32.1	7.79E+02	11	7.08E+01	4.00E-01	5	12055.82	1p	room=40	1.5	3.3/2.5	Static	-	0
20	28/06/2010	20	7	02:24	82Kr22+	768	32	94	0	32.1	5.00E+05	443	1.13E+03	2.57E+02	2	256.8	1	room=40	1.5	3.3/2.5	Dyn	-	0
21	28/06/2010	21	8	02:35	82Kr22+	768	32	94	0	32.1	4.82E+05	391	1.23E+03	2.48E+02	2	504.3552	1	room=40	1.5	3.3/2.5	Dyn	-	0
22	28/06/2010	22	9	02:42	82Kr22+	768	32	94	0	32.1	5.00E+05	391	1.28E+03	2.57E+02	2	761.1552	1	room=40	1.5	3.3/2.5	Dyn	-	0
23	28/06/2010	23	10	02:50	82Kr22+	768	32	94	0	32.1	5.00E+05	397	1.26E+03	2.57E+02	2	1017.955	1	room=40	1.5	3.3/2.5	Dyn	-	0
25	28/06/2010	25	11	03:04	82Kr22+	768	32	94	0	32.1	5.00E+05	395	1.27E+03	2.57E+02	2	1274.755	1	room=40	1.5	3.3/2.5	Dyn	-	0
26	28/06/2010	26	12	03:14	82Kr22+	768	32	94	0	32.1	5.01E+05	394	1.27E+03	2.57E+02	2	1532.069	1	room=40	1.5	3.3/2.5	Dyn	-	0
28	28/06/2010	28	13	03:46	82Kr22+	768	32	94	0	32.1	1.00E+06	853	1.17E+03	5.14E+02	2	2045.669	1	room=40	1.5	3.3/2.5	Dyn	-	0
29	28/06/2010	29	14	04:04	82Kr22+	768	32	94	0	32.1	1.00E+06	892	1.12E+03	5.14E+02	2	2559.269	1	room=40	1.5	3.3/2.5	Dyn	-	0
33	28/06/2010	33	15	04:35	82Kr22+	768	32	94	0	32.1	1.00E+06	779	1.28E+03	5.14E+02	2	3072.869	1	room=40	1.5	3.3/2.5	Dyn	-	0
34	28/06/2010	34	16	04:50	82Kr22+	768	32	94	0	32.1	1.00E+06	544	1.84E+03	5.14E+02	2	3586.469	1	room=40	1.5	3.3/2.5	Dyn	-	0
35	28/06/2010	35	17	05:01	82Kr22+	768	32	94	0	32.1	1.00E+06	564	1.77E+03	5.14E+02	2	4100.069	1	room=40	1.5	3.3/2.5	Dyn	-	0
36	28/06/2010	-	18	05:11	82Kr22+	768	32	94	0	32.1	1.09E+05	66	1.65E+03	5.60E+01	2	4156.051	-	room=40	-	-	-	-	-
37	28/06/2010	36	19	05:13	82Kr22+	768	32	94	0	32.1	1.00E+06	579	1.73E+03	5.14E+02	2	4613.669	1	room=40	1.5	3.3/2.5	Dyn	-	0
38	28/06/2010	37	20	05:27	82Kr22+	768	32	94	0	32.1	1.00E+06	485	2.06E+03	5.14E+02	2	5127.269	1	room=40	1.5	3.3/2.5	Dyn FF	-	0
40	28/06/2010	39	21	05:48	82Kr22+	768	32	94	0	32.1	1.00E+06	453	2.21E+03	5.14E+02	2	5640.869	1	room=40	1.5	3.3/2.5	Static	10	0
44	28/06/2010	43	22	06:46	82Kr22+	768	32	94	0	32.1	1.00E+06	618	1.62E+03	5.14E+02	2	6154.469	2	room=40	1.5	3.3/2.5	Dyn	-	0
45	28/06/2010	44	23	06:59	82Kr22+	768	32	94	0	32.1	1.00E+06	661	1.51E+03	5.14E+02	2	6668.069	2	room=40	1.5	3.3/2.5	Dyn	-	0
46	28/06/2010	45	24	07:12	82Kr22+	768	32	94	0	32.1	1.00E+06	690	1.45E+03	5.14E+02	2	7181.669	2	room=40	1.5	3.3/2.5	Dyn	-	0
47	28/06/2010	46	25	07:25	82Kr22+	768	32	94	0	32.1	1.00E+06	728	1.37E+03	5.14E+02	2	7695.269	2	room=40	1.5	3.3/2.5	Dyn	-	0
50	28/06/2010	49	26	07:59	82Kr22+	768	32	94	0	32.1	1.00E+06	213	4.69E+03	5.14E+02	3	513.6	2	room=40	1.5	3.3/2.5	Dyn	-	0
51	28/06/2010	50	27	08:08	82Kr22+	768	32	94	0	32.1	1.00E+06	688	1.45E+03	5.14E+02	3	1027.2	2	room=40	1.5	3.3/2.5	Dyn	-	0
52	28/06/2010	51	28	08:45	82Kr22+	768	32	94	0	32.1	1.00E+06	302	3.31E+03	5.14E+02	3	1540.8	2	room=40	1.5	3.3/2.5	Dyn	-	0
54	28/06/2010	53	29	08:53	82Kr22+	768	32	94	0	32.1	1.00E+06	204	4.90E+03	5.14E+02	3	2054.4	2	room=40	1.5	3.3/2.5	Dyn	-	0
55	28/06/2010	54	30	08:58	82Kr22+	768	32	94	0	32.1	1.00E+06	205	4.88E+03	5.14E+02	3	2568	2	room=40	1.5	3.3/2.5	Dyn	-	0
60	28/06/2010	59	31	09:27	82Kr22+	768	32	94	0	32.1	1.14E+03	44	2.59E+01	5.86E-01	3	2568.586	1	room=40	1.5	3.3/2.5	Dyn	-	0
62	28/06/2010	61	32	09:37	82Kr22+	768	32	94	0	32.1	1.00E+06	201	4.98E+03	5.14E+02	3	3082.186	1	room=40	1.5	3.3/2.5	Dyn	-	0
64	28/06/2010	63	33	09:44	82Kr22+	768	32	94	0	32.1	1.00E+06	202	4.95E+03	5.14E+02	3	3595.786	1	room=40	1.5	3.3/2.5	Dyn	-	0
66	28/06/2010	65	34	09:52	82Kr22+	768	32	94	0	32.1	1.00E+06	205	4.88E+03	5.14E+02	3	4109.386	1	room=40	1.5	3.3/2.5	Dyn	-	0
67	28/06/2010	66	35	09:58	82Kr22+	768	32	94	0	32.1	1.00E+06	206	4.85E+03	5.14E+02	3	4622.986	1	room=40	1.5	3.3/2.5	Dyn	-	0
69	28/06/2010	68	36	10:06	82Kr22+	768	32	94	0	32.1	1.00E+06	210	4.76E+03	5.14E+02	3	5136.586	1	room=40	1.5	3.3/2.5	Dyn	-	0
70	28/06/2010	69	37	10:11	82Kr22+	768	32	94	0	32.1	1.00E+06	215	4.65E+03	5.14E+02	3	5650.186	1	room=40	1.5	3.3/2.5	Dyn	-	0
71	28/06/2010	70	38	10:17	82Kr22+	768	32	94	0	32.1	6.63E+05	152	4.36E+03	3.41E+02	3	5990.702	1p	room=40	1.5	3.3/2.5	-	-	0
72	28/06/2010	71	39	10:21	82Kr22+	768	32	94	0	32.1	7.31E+05	169	4.33E+03	3.75E+02	3	6366.144	1p	room=40	1.5	3.3/2.5	-	-	0
73	28/06/2010	72	40	10:28	82Kr22+	768	32	94	0	32.1	3.19E+05	75	4.25E+03	1.64E+02	3	6529.982	1p	room=40	1.5	3.3/2.5	-	-	0
74	28/06/2010	72b	41	10:29	82Kr22+	768	32	94	0	32.1	7.88E+03	4	1.97E+03	4.05E+00	3	6534.029	1p	room=40	1.5	3.3/2.5	-	-	0
75	28/06/2010	73	42	10:36	82Kr22+	768	32	94	0	32.1	6.50E+04	18	3.61E+03	3.34E+01	3	6567.413	1p	room=40	1.5	3.3/2.5	-	-	0
78	28/06/2010	-	43	10:45	15Ne15+	139	1.8	202	0	1.8	6.36E+05	75	8.48E+03	1.83E+01	0	0	B	room=40	-	-	-	-	-
82	28/06/2010	79	44	11:09	15Ne15+	139	1.8	202	0	1.8	2.01E+06	199	1.01E+04	5.79E+01	4	57.888	1	room=40	1.5	3.3/2.5	Dyn	-	0
83	28/06/2010	80	45	11:15	15Ne15+	139	1.8	202	0	1.8	2.01E+06	195	1.03E+04	5.79E+01	4	115.776	1	room=40	1.5	3.3/2.5	Dyn	-	0
84	28/06/2010	81	46	11:20	15Ne15+	139	1.8	202	0	1.8	2.00E+06	203	9.85E+03	5.76E+01	4	173.376	1	room=40	1.5	3.3/2.5	Dyn	-	0
85	28/06/2010	82	47	11:25	15Ne15+	139	1.8	202	0	1.8	2.01E+06	203	9.90E+03	5.79E+01	4	231.264	1	room=40	1.5	3.3/2.5	Dyn	-	0
86	28/06/2010	83	48	11:30	15Ne15+	139	1.8	202	0	1.8	2.00E+06	207	9.66E+03	5.76E+01	4	288.864	1	room=40	1.5	3.3/2.5	Dyn	-	0
87	28/06/2010	84	49	11:35	15Ne15+	139	1.8	202	0	1.8	2.00E+06	208	9.62E+03	5.76E+01	4	346.464	1	room=40	1.5	3.3/2.5	Dyn	-	0
90	28/06/2010	87	50	11:54	15Ne15+	139	1.8	202	0	1.8	2.01E+06	216	9.31E+03	5.79E+01	6	57.888	1	room=40	1.5	3.3/2.5	Dyn	-	0
91	28/06/2010	88	51	12:00	15Ne15+	139	1.8	202	0	1.8	2.00E+06	217	9.22E+03	5.76E+01	6	115.488	1	room=40	1.5	3.3/2.5	Dyn	-	0
92	28/06/2010	89	52	12:04	15Ne15+	139	1.8	202	0	1.8	2.01E+06	222	9.05E+03	5.79E+01	6	173.376	1	room=40	1.5	3.3/2.5	Dyn	-	0
93	28/06/2010	90	53	12:09	15Ne15+	139	1.8	202	0	1.8	2.01E+06	221	9.10E+03	5.79E+01	6	231.264	1	room=40	1.5	3.3/2.5	Dyn	-	0
94	28/06/2010	91	54	12:14	15Ne15+	139	1.8	202	0	1.8	2.01E+06	226	8.89E+03	5.79E+01	6	289.152	1	room=40	1.5	3.3/2.5	Dyn	-	0
95	28/06/2010	92	55	12:18	15Ne15+	139	1.8	202	0	1.8	2.00E+06	226	8.85E+03	5.76E+01	6	346.752	1	room=40	1.5	3.3/2.5	Dyn	-	0
96	29/06/2010	93	56	09:22	56Fe15+	523	19	97	0	18.5	1.42E+05	303	4.69E+02	4.20E+01	6	388.784	BS	room=40	1.5	3.3/2.5	-	-	-
97	29/06/2010	94	57	09:32	56Fe15+	523	19	97	0	18.5	1.00E+06	264	3.79E+03	2.96E+02	6	684.784	1	room=40	1.5	3.3/2.5	Dyn	-	0
98	29/06/2010	95	58	09:38	56Fe15+	523	19	97	0	18.5	1.00E+06	270	3.70E+03	2.96E+02	6	980.784	1	room=40	1.5	3.3/2.5	Dyn	-	0
99	29/06/2010	96	59	09:44	56Fe15+	523	19	97	0	18.5	1.00E+06	301	3.32E+03	2.96E+02	6	1276.784	1	room=40	1.5	3.3/2.5	Dyn	-	0
100	29/06/2010	97	60	09:50	56Fe15+	523	19	97	0	18.5	1.00E+06	319	3.13E+03	2.96E+02	6	1572.784	1	room=40	1.5	3.3/2.5	Dyn	-	0
101	29/06/2010	98	61	09:57	56Fe15+	523	19	97	0	18.5	1.00E+06	220	4.55E+03	2.96E+02	6	1868.784	1	room=40	1.5	3.3/2.5	Dyn	-	0
102	29/06/2010	99	62	10:03	56Fe15+	523	19	97	0	18.5	1.00E+06	218	4.59E+03	2.96E+02	6	2164.784	1	room=40	1.5	3.3/2.5	Dyn	-	0
104	29/06/2010	101	63	10:12	56Fe15+	523	19	97	0	18.5	1.00E+06	243	4.12E+03	2.96E+02	6	2460.784	1	room=40	1.5	3.3/2.5	Dyn	-	0
105	29/06/2010	102	64	10:17	56Fe15+	523	19	97	0	18.5	1.00E+06	247	4.05E+03	2.96E+02	6	2756.784	1	room=40	1.5	3.3/2.5	Dyn	-	0
106	29/06/2010	103	65	10:23	56Fe15+	523	19	97	0	18.5	1.00E+06	237	4.22E+03	2.96E+02	6	3052.784	1	room=40	1.5	3.3/2.5	Dyn	-	0
107	29/06/2010	104	66	10:28	56Fe15+	523	19	97	0	18.5	1.00E+06	248	4.03E+03	2.96E+02	6	3348.784	1	room=40	1.5	3.3/2.5	Dyn	-	0
109	29/06/2010	106	67	10:51	56Fe15+	523	19	97	0	18.5	1.00E+06	256	3.91E+03	2.96E+02	6	3644.784	2	room=40	1.5	3.3/2.5	Dyn	-	0
110	29/06/2010	107	68	10:56	56Fe15+	523	19	97	0	18.5	1.00E+06	244	4.10E+03	2.96E+02	6	3940.784	2	room=40	1.5	3.3/2.5	Dyn	-	0
111	29/06/2010	108	69	11:02	56Fe15+	523	19	97	0	18.5	1.00E+06	253	3.95E+03	2.96E+02	6	4236.784	2	room=40	1.5	3.3/2.5	Dyn	-	0
112	29/06/2010	109	70	11:07	56Fe15+	523	19	97	0	18.5	1.00E+06	255	3.92E+03	2.96E+02	6	4532.784	2	room=40	1.5	3.3/2.5	Dyn	-	0
113	29/06/2010	110	71	11:13	56Fe15+	523	19	97	0	18.5	9.74E+05	247	3.94E+03	2.88E+02	6	4821.088	2p	room=40	1.5	3.3/2.5	-	-	0
114	29/06/2010	111	72	11:19	56Fe15+	523	19	97	0	18.5	6.13E+05	161	3.81E+03	1.81E+02	6	5002.536	2p	room=40	1.5	3.3/2.5	-	-	0
119	29/06/2010	116	73	11:51	56Fe15+	523	19	97	0	18.5	1.00E+06	236	4.24E+03	2.96E+02	4	642.464	1	room=40	1.5	3.3/2.5	Dyn	-	0
120	29/06/2010	117	74	11:56	56Fe15+	523	19	97	0	18.5	1.00E+06	201	4.98E+03	2.96E+02	4	938.464	1	room=40	1.5	3.3/2.5	Dyn	-	0
121	29/06/2010	118	75	12:01	56Fe15+	523	19	97	0	18.5	1.00E+06	191	5.24E+03	2.96E+02	4	1234.464	1	room=40	1.5	3.3/2.5	Dyn	-	0
122	29/06/2010	119	76	12:05	56Fe15+	523	19	97	0	18.5	1.00E+06	203	4.93E+03	2.96E+02	4	1530.464	1	room=40	1.5	3.3/2.5	Dyn	-	0
123	29/06/2010	120	77	12:10	56Fe15+	523	19	97	0	18.5	1.00E+06	196	5.10E+03	2.96E+02	4	1826.464	1	room=40	1.5	3.3/2.5	Dyn	-	0
124	29/06/2010	121	78	12:16	56Fe15+	523	19	97	0	18.5	1.00E+06	198	5.05E+03	2.96E+02	4	2122.464	1	room=40	1.5	3.3/2.5	Dyn	-	0
125	29/06/2010	122	79	12:21	56Fe15+	523	19	97	0	18.5	1.00E+06	204	4.90E+03	2.96E+02	4	2418.464	1	room=40	1.5	3.3/2.5	Dyn	-	0

	RUN				BEAM									DUT								
Line #	Date	Run #	JYFL Run #	Start Time	Ion specie	Energy (MeV)	LET (MeV/(mg/cm²))	Range (Si) (µm)	Tilt (Deg)	LETeff. (MeV/(mg/cm²))	Fluence (p/cm²)	Run Duration (s)	Mean flux (p/(cm².s))	Run dose (Rad)	SN	Total Dose (Rad)	TV	Temperature (°C)	Vcore (V)	Vio (V)	Mode	Exposition Time (s)	SEL
126	29/06/2010	123	80	12:25	56Fe15+	523	19	97	0	18.5	1.00E+06	208	4.81E+03	2.96E+02	4	2714.464	1	room=40	1.5	3.3/2.5	Dyn	-	0
127	29/06/2010	124	81	12:30	56Fe15+	523	19	97	0	18.5	1.00E+06	205	4.88E+03	2.96E+02	4	3010.464	1	room=40	1.5	3.3/2.5	Dyn	-	0
128	29/06/2010	125	82	12:35	56Fe15+	523	19	97	0	18.5	1.00E+06	210	4.76E+03	2.96E+02	4	3306.464	1	room=40	1.5	3.3/2.5	Dyn	-	0
131	29/06/2010	128	83	12:58	56Fe15+	523	19	97	0	18.5	1.00E+06	162	6.17E+03	2.96E+02	4	3602.464	2	room=40	1.5	3.3/2.5	Dyn	-	0
132	29/06/2010	129	84	01:02	56Fe15+	523	19	97	0	18.5	1.00E+06	145	6.90E+03	2.96E+02	4	3898.464	2	room=40	1.5	3.3/2.5	Dyn	-	0
133	29/06/2010	130	85	01:05	56Fe15+	523	19	97	0	18.5	1.00E+06	141	7.09E+03	2.96E+02	4	4194.464	2	room=40	1.5	3.3/2.5	Dyn	-	0
134	29/06/2010	131	86	01:08	56Fe15+	523	19	97	0	18.5	1.00E+06	145	6.90E+03	2.96E+02	4	4490.464	2	room=40	1.5	3.3/2.5	Dyn	-	0
135	29/06/2010	-	87	01:37	131Xe35+	1217	55	89	0	55.3	2.27E+05	240	9.46E+02	2.01E+02	0	0	B	room=40	-	-	-	-	-
136	29/06/2010	133	88	01:45	131Xe35+	1217	55	89	0	55.3	5.00E+05	253	1.98E+03	4.42E+02	4	4932.864	2	room=40	1.5	3.3/2.5	Dyn	-	0
137	29/06/2010	134	89	01:50	131Xe35+	1217	55	89	0	55.3	5.00E+05	268	1.87E+03	4.42E+02	4	5375.264	2	room=40	1.5	3.3/2.5	Dyn	-	0
138	29/06/2010	135	90	01:55	131Xe35+	1217	55	89	0	55.3	5.00E+05	261	1.92E+03	4.42E+02	4	5817.664	2	room=40	1.5	3.3/2.5	Dyn	-	0
139	29/06/2010	136	91	02:00	131Xe35+	1217	55	89	0	55.3	5.00E+05	263	1.90E+03	4.42E+02	4	6260.064	2	room=40	1.5	3.3/2.5	Dyn	-	0
142	29/06/2010	139	92	02:33	131Xe35+	1217	55	89	0	55.3	5.00E+05	269	1.86E+03	4.42E+02	4	6702.464	1	room=40	1.5	3.3/2.5	Dyn	-	0
143	29/06/2010	140	93	02:40	131Xe35+	1217	55	89	0	55.3	5.00E+05	268	1.87E+03	4.42E+02	4	7144.864	1	room=40	1.5	3.3/2.5	Dyn	-	0
144	29/06/2010	141	94	02:45	131Xe35+	1217	55	89	0	55.3	5.00E+05	269	1.86E+03	4.42E+02	4	7587.264	1	room=40	1.5	3.3/2.5	Dyn	-	0
146	29/06/2010	143	95	02:51	131Xe35+	1217	55	89	0	55.3	5.00E+05	263	1.90E+03	4.42E+02	4	8029.664	1	room=40	1.5	3.3/2.5	Dyn	-	0
147	29/06/2010	144	96	02:58	131Xe35+	1217	55	89	0	55.3	5.00E+05	267	1.87E+03	4.42E+02	4	8472.064	1	room=40	1.5	3.3/2.5	Dyn	-	0
148	29/06/2010	145	97	03:04	131Xe35+	1217	55	89	0	55.3	5.00E+05	276	1.81E+03	4.42E+02	4	8914.464	1	room=40	1.5	3.3/2.5	Dyn	-	0
149	29/06/2010	146	98	03:09	131Xe35+	1217	55	89	0	55.3	5.00E+05	265	1.89E+03	4.42E+02	4	9356.864	1	room=40	1.5	3.3/2.5	Dyn	-	0
150	29/06/2010	147	99	03:15	131Xe35+	1217	55	89	0	55.3	5.00E+05	268	1.87E+03	4.42E+02	4	9799.264	1	room=40	1.5	3.3/2.5	Dyn	-	0
151	29/06/2010	148	100	03:21	131Xe35+	1217	55	89	0	55.3	5.00E+05	276	1.81E+03	4.42E+02	4	10241.66	1	room=40	1.5	3.3/2.5	Dyn	-	0
152	29/06/2010	149	101	03:26	131Xe35+	1217	55	89	0	55.3	5.00E+05	266	1.88E+03	4.42E+02	4	10684.06	1	room=40	1.5	3.3/2.5	Dyn	-	0
153	29/06/2010	150	102	03:39	131Xe35+	1217	55	89	0	55.3	5.00E+05	183	2.73E+03	4.42E+02	4	11126.46	1	85	1.5	3.3/2.5	Dyn	-	0
154	29/06/2010	151	103	03:44	131Xe35+	1217	55	89	0	55.3	5.00E+06	325	1.54E+04	4.42E+03	4	15550.46	1	85	1.5	3.3/2.5	Dyn	-	0
155	29/06/2010	152	104	03:56	131Xe35+	1217	55	89	0	55.3	5.00E+06	288	1.74E+04	4.42E+03	4	19974.46	1	105	1.5	3.3/2.5	Dyn	-	0
156	29/06/2010	153	105	04:05	131Xe35+	1217	55	89	0	55.3	5.00E+06	288	1.74E+04	4.42E+03	4	24398.46	1	125	1.5	3.3/2.5	Dyn	-	0
159	29/06/2010	156	106	04:26	131Xe35+	1217	55	89	0	55.3	1.62E+06	112	1.45E+04	1.43E+03	4	25831.84	1	125	1.65	3.6/2.5	Dyn	-	0
160	29/06/2010	157	107	04:29	131Xe35+	1217	55	89	0	55.3	3.49E+06	196	1.78E+04	3.09E+03	4	28919.79	1	125	1.65	3.6/2.5	Dyn	-	0
162	29/06/2010	159	108	05:10	131Xe35+	1217	55	89	0	55.3	5.00E+06	281	1.78E+04	4.42E+03	5	16479.82	1	125	1.65	3.6/2.5	Dyn	-	0
164	29/06/2010	161	109	05:38	131Xe35+	1217	55	89	0	55.3	5.00E+05	31	1.61E+04	4.42E+02	5	16922.22	1	room=40	1.5	3.3/2.5	Dyn	-	0
165	29/06/2010	162	110	05:43	131Xe35+	1217	55	89	0	55.3	5.00E+05	123	4.07E+03	4.42E+02	5	17364.62	1	room=40	1.5	3.3/2.5	Dyn	-	0
166	29/06/2010	163	111	05:46	131Xe35+	1217	55	89	0	55.3	5.00E+05	124	4.03E+03	4.42E+02	5	17807.02	1	room=40	1.5	3.3/2.5	Dyn	-	0
167	29/06/2010	164	112	05:49	131Xe35+	1217	55	89	0	55.3	5.00E+05	121	4.13E+03	4.42E+02	5	18249.42	1	room=40	1.5	3.3/2.5	Dyn	-	0
168	29/06/2010	165	113	05:52	131Xe35+	1217	55	89	0	55.3	5.00E+05	123	4.07E+03	4.42E+02	5	18691.82	1	room=40	1.5	3.3/2.5	Dyn	-	0
169	29/06/2010	166	114	05:55	131Xe35+	1217	55	89	0	55.3	5.00E+05	125	4.00E+03	4.42E+02	5	19134.22	1	room=40	1.5	3.3/2.5	Dyn	-	0
170	29/06/2010	167	115	06:01	131Xe35+	1217	55	89	0	55.3	5.00E+05	116	4.31E+03	4.42E+02	5	19576.62	1	room=40	1.5	3.3/2.5	Dyn	-	0
171	29/06/2010	168	116	06:04	131Xe35+	1217	55	89	0	55.3	5.00E+05	117	4.27E+03	4.42E+02	5	20019.02	1	room=40	1.5	3.3/2.5	Dyn	-	0
173	29/06/2010	170	117	06:20	131Xe35+	1217	55	89	0	55.3	5.00E+05	119	4.20E+03	4.42E+02	5	20461.42	1	room=40	1.5	3.3/2.5	Dyn	-	0
174	29/06/2010	171	118	06:23	131Xe35+	1217	55	89	0	55.3	5.00E+05	119	4.20E+03	4.42E+02	5	20903.82	1	room=40	1.5	3.3/2.5	Dyn	-	0
178	29/06/2010	175	119	07:07	131Xe35+	1217	55	89	0	55.3	5.00E+05	133	3.76E+03	4.42E+02	8	442.4	2	room=40	1.5	3.3/2.5	Dyn	-	0
179	29/06/2010	176	120	07:10	131Xe35+	1217	55	89	0	55.3	5.00E+05	129	3.88E+03	4.42E+02	8	884.8	2	room=40	1.5	3.3/2.5	Dyn	-	0
180	29/06/2010	177	121	07:13	131Xe35+	1217	55	89	0	55.3	5.00E+05	130	3.85E+03	4.42E+02	8	1327.2	2	room=40	1.5	3.3/2.5	Dyn	-	0
181	29/06/2010	178	122	07:16	131Xe35+	1217	55	89	0	55.3	5.00E+05	136	3.68E+03	4.42E+02	8	1769.6	2	room=40	1.5	3.3/2.5	Dyn	-	0
182	29/06/2010	-	123	10:02	40Ar12+	372	10	118	0	10.1	6.05E+05	381	1.59E+03	9.78E+01	8	1867.368	-	room=40	-	-	-	-	-
183	29/06/2010	179	124	10:10	40Ar12+	372	10	118	0	10.1	2.00E+06	291	6.87E+03	3.23E+02	8	2190.568	2	room=40	1.5	3.3/2.5	Dyn	-	0
184	29/06/2010	180	125	10:16	40Ar12+	372	10	118	0	10.1	2.00E+06	217	9.22E+03	3.23E+02	8	2513.768	2	room=40	1.5	3.3/2.5	Dyn	-	0
185	29/06/2010	181	126	10:20	40Ar12+	372	10	118	0	10.1	2.00E+06	216	9.26E+03	3.23E+02	8	2836.968	2	room=40	1.5	3.3/2.5	Dyn	-	0
189	29/06/2010	185	127	10:59	40Ar12+	372	10	118	0	10.1	2.00E+06	211	9.48E+03	3.23E+02	2	8018.469	2	room=40	1.5	3.3/2.5	Dyn	-	0
190	29/06/2010	186	128	11:03	40Ar12+	372	10	118	0	10.1	2.00E+06	193	1.04E+04	3.23E+02	2	8341.669	2	room=40	1.5	3.3/2.5	Dyn	-	0
191	29/06/2010	187	129	11:07	40Ar12+	372	10	118	0	10.1	2.00E+06	193	1.04E+04	3.23E+02	2	8664.869	2	room=40	1.5	3.3/2.5	Dyn	-	0
192	29/06/2010	188	130	11:11	40Ar12+	372	10	118	0	10.1	2.00E+06	199	1.01E+04	3.23E+02	2	8988.069	2	room=40	1.5	3.3/2.5	Dyn	-	0
194	29/06/2010	190	131	11:39	40Ar12+	372	10	118	0	10.1	2.00E+06	224	8.93E+03	3.23E+02	2	9311.269	1	room=40	1.5	3.3/2.5	Dyn	-	0
195	29/06/2010	191	132	11:43	40Ar12+	372	10	118	0	10.1	2.00E+06	227	8.81E+03	3.23E+02	2	9634.469	1	room=40	1.5	3.3/2.5	Dyn	-	0
196	29/06/2010	192	133	11:48	40Ar12+	372	10	118	0	10.1	2.00E+06	227	8.81E+03	3.23E+02	2	9957.669	1	room=40	1.5	3.3/2.5	Dyn	-	0
197	29/06/2010	193	134	11:52	40Ar12+	372	10	118	0	10.1	2.00E+06	228	8.77E+03	3.23E+02	2	10280.87	1	room=40	1.5	3.3/2.5	Dyn	-	0
198	29/06/2010	194	135	11:57	40Ar12+	372	10	118	0	10.1	2.00E+06	232	8.62E+03	3.23E+02	2	10604.07	1	room=40	1.5	3.3/2.5	Dyn	-	0
199	29/06/2010	195	136	12:01	40Ar12+	372	10	118	0	10.1	2.00E+06	1.33E+06	1.50E+00	3.23E+02	2	10927.27	1	room=40	1.5	3.3/2.5	Dyn	-	0
201	29/06/2010	197	137	12:08	40Ar12+	372	10	118	0	10.1	2.00E+06	236	8.47E+03	3.23E+02	2	11250.47	1	room=40	1.5	3.3/2.5	Dyn	-	0
202	29/06/2010	198	138	12:12	40Ar12+	372	10	118	0	10.1	2.00E+06	238	8.40E+03	3.23E+02	2	11573.67	1	room=40	1.5	3.3/2.5	Dyn	-	0
203	29/06/2010	199	139	12:17	40Ar12+	372	10	118	0	10.1	2.00E+06	241	8.30E+03	3.23E+02	2	11896.87	1	room=40	1.5	3.3/2.5	Dyn	-	0
204	29/06/2010	200	140	12:22	40Ar12+	372	10	118	0	10.1	2.00E+06	242	8.26E+03	3.23E+02	2	12220.07	1	room=40	1.5	3.3/2.5	Dyn	-	0
205	29/06/2010	201	141	12:27	40Ar12+	372	10	118	0	10.1	2.00E+06	361	5.54E+03	3.23E+02	2	12543.27	1p	room=40	1.5	3.3/2.5	-	-	0
207	29/06/2010	-	142	12:54	20Ne6+	186	3.6	146	0	3.6	9.86E+05	130	7.58E+03	5.68E+01	0	0	B	room=40	-	-	-	-	-
208	29/06/2010	203	143	12:59	20Ne6+	186	3.6	146	0	3.6	2.00E+06	181	1.10E+04	1.15E+02	2	12658.47	1	room=40	1.5	3.3/2.5	Dyn	-	0
209	29/06/2010	204	144	01:03	20Ne6+	186	3.6	146	0	3.6	2.00E+06	181	1.10E+04	1.15E+02	2	12773.67	1	room=40	1.5	3.3/2.5	Dyn	-	0
210	29/06/2010	205	145	01:07	20Ne6+	186	3.6	146	0	3.6	2.00E+06	181	1.10E+04	1.15E+02	2	12888.87	1	room=40	1.5	3.3/2.5	Dyn	-	0
211	29/06/2010	206	146	01:11	20Ne6+	186	3.6	146	0	3.6	2.00E+06	188	1.06E+04	1.15E+02	2	13004.07	1	room=40	1.5	3.3/2.5	Dyn	-	0
212	29/06/2010	207	147	01:15	20Ne6+	186	3.6	146	0	3.6	2.00E+06	189	1.06E+04	1.15E+02	2	13119.27	1	room=40	1.5	3.3/2.5	Dyn	-	0
213	29/06/2010	208	148	01:19	20Ne6+	186	3.6	146	0	3.6	2.00E+06	191	1.05E+04	1.15E+02	2	13234.47	1	room=40	1.5	3.3/2.5	Dyn	-	0
214	29/06/2010	209	149	01:23	20Ne6+	186	3.6	146	0	3.6	2.00E+06	188	1.06E+04	1.15E+02	2	13349.67	1	room=40	1.5	3.3/2.5	Dyn	-	0
215	29/06/2010	210	150	01:27	20Ne6+	186	3.6	146	0	3.6	2.00E+06	182	1.10E+04	1.15E+02	2	13464.87	1	room=40	1.5	3.3/2.5	Dyn	-	0
216	29/06/2010	211	151	01:30	20Ne6+	186	3.6	146	0	3.6	2.00E+06	182	1.10E+04	1.15E+02	2	13580.07	1	room=40	1.5	3.3/2.5	Dyn	-	0
217	29/06/2010	212	152	01:34	20Ne6+	186	3.6	146	0	3.6	2.00E+06	182	1.10E+04	1.15E+02	2	13695.27	1	room=40	1.5	3.3/2.5	Dyn	-	0
219	29/06/2010	214	153	02:01	20Ne6+	186	3.6	146	0	3.6	2.00E+06	182	1.10E+04	1.15E+02	2	13810.47	2	room=40	1.5	3.3/2.5	Dyn	-	0
220	29/06/2010	215	154	02:06	20Ne6+	186	3.6	146	0	3.6	2.00E+06	180	1.11E+04	1.15E+02	2	13925.67	2	room=40	1.5	3.3/2.5	Dyn	-	0
221	29/06/2010	216	155	02:10	20Ne6+	186	3.6	146	0	3.6	2.00E+06	179	1.12E+04	1.15E+02	2	14040.87	2	room=40	1.5	3.3/2.5	Dyn	-	0
222	29/06/2010	217	156	02:13	20Ne6+	186	3.6	146	0	3.6	2.00E+06	178	1.12E+04	1.15E+02	2	14156.07	2	room=40	1.5	3.3/2.5	Dyn	-	0
223	29/06/2010	218	157	02:17	20Ne6+	186	3.6	146	0	3.6	3.02E+06	263	1.15E+04	1.74E+02	2	14330.02	2p	room=40	1.5	3.3/2.5	-	-	0

12.2 SHIFT REGISTER CONDITIONS AND SEU - TABLES

	SR conditions				SR - Total SEU													
Line #	F (MHz)	Channel Mask (Hex)	Pattern	Valide	SR 1	SR 2	SR 3	SR 4	SR 5	SR 6	SR 7	SR 8	SR 9	SR 10	SR 11	SR 12	SR 13	SR 14	SR 15	SR 16
6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
20	100	3FFF	CKB /CKB	0	43	43	34	30	1					26	19	1	4			
21	100	3FFF	S0/S1	0	66	48	21	19					1	28	3	1	1			
22	100	3FFF	S0/S1	1	48	42	65	65	54	42	72	44	45	42	35	42	21	46		
23	100	3FFF	CKB /CKB	1	65	75	76	105	71	83	47	54	63	69	59	51	45	52		
25	150	351	CKB /CKB	1	65				27		23		56	68						
26	150	351	S0/S1	1	59				64		46		57	50						
28	200	3FF1	CKB /CKB	1	141				123	85	140	74	118	121	271	297	252	278		
29	200	3FF1	S0/S1	1	106				143	948	163	965	115	131	98	122	77	124		
33	50	3FF	CKB /CKB	1	103	113	174	123	102	122	106	97	95	102						
34	50	3FF	S0/S1	1	108	92	110	108	94	98	82	109	101	86						
35	2	3FF	CKB /CKB	1	76	79	142	58	72	92	88	79	82	91						
36	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
37	2	3FF	S0/S1	1	91	83	104	85	67	71	91	94	84	98						
38	-	-	-	-																
40	2	3FF	CKB /CKB	1	91	93	136	168	78	92	88	79	89	72						
44	2	FFC7	CKB /CKB	1	15	15	15				103									
45	2	FFC7	S0/S1	1	5	5	5				87									
46	37.5	FFC7	CKB /CKB	1	1	1	1				88									
47	37.5	FFC7	S0/S1	1	3	3	3				105									
50	2	FFC7	CKB /CKB	1	21	21	21				101									
51	2	FFC7	CKB /CKB	1	13	13	13				92									
52	2	FFC7	S0/S1	1	2	2	2				80									
54	37.5	FFC7	CKB /CKB	1	1	1	1				127									
55	37.5	FFC7	S0/S1	1	2	2	2				96									
60	100	3BFF	CKB /CKB	0													2			
62	100	3BFF	CKB /CKB	1	95	118	195	126	90	118	97	94	89	100		85	93	91		
64	100	3FFF	S0/S1	1	115	95	142	124	84	99	101	107	81	72	119	74	76	100		
66	150	351	S0/S1	1	100				85		106		110	116						
67	150	351	CKB /CKB	1	114				51		72		120	101						
69	200	3F51	CKB /CKB	-1	81				11		2		49	71	33	27	26	31		
70	200	3F51	S0/S1	1	135				174		156		130	138	109	104	101	121		
71	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
72	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
73	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
74	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
75	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
78	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
82	100	3FFF	CKB /CKB	1											34	1	3			
83	100	3FFF	S0/S1	1		1											1			
84	150	351	CKB /CKB	1																
85	150	351	S0/S1	1																
86	200	??	CKB /CKB																	
87	200	3FF1	S0/S1	1						231		231					1			
90	100	3FFF	CKB /CKB	1											148		10			
91	100	3FFF	S0/S1	1									1							
92	150	351	CKB /CKB	1																
93	150	351	S0/S1	1																
94	200	3FF1	CKB /CKB	1	7				6	6	9	7	7	12	9	14	9	11		
95	200	3FF1	S0/S1	1	1					196	1	197								
96	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
97	2	3FF	CKB /CKB	1	59	50	116	45	57	46	58	57	62	49						
98	2	3FF	S0/S1	1	55	59	64	52	44	49	56	49	59	59						
99	50	3FF	CKB /CKB	1	57	59	83	58	51	52	51	56	63	49						
100	50	3FF	S0/S1	1	51	60	66	46	64	53	64	48	64	45						
101	100	3FFF	CKB /CKB	1	81	55	132	60	66	56	59	62	58	78	95	57	58	55		
102	100	3FFF	S0/S1	1	62	59	70	59	56	67	59	71	54	46	51	63	36	61		
104	150	351	CKB /CKB	1	73				12		24		59	75						
105	150	351	S0/S1	1	56				64		66		62	55						
106	200	3FF1	CKB /CKB	1	5				6	10	3	1	19	13	1	1	1	21		
107	200	3FF1	S0/S1	1	80				114	330	82	314	57	80	60	61	30	58		
109	2	FFC7	CKB /CKB	1							51									
110	2	FFC7	S0/S1	1							52									
111	37.5	FFC7	CKB /CKB	1							49									
112	37.5	FFC7	S0/S1	1							51									
113	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
114	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
119	2	3FF	CKB /CKB	1	46	41	69	52	64	46	52	55	53	54						
120	2	3FF	S0/S1	1	49	46	70	50	56	50	56	59	45	58						
121	50	3FF	CKB /CKB	1	58	50	80	66	56	50	65	58	58	63						
122	50	3FF	S0/S1	1	56	66	67	62	45	52	65	68	60	55						
123	100	3FFF	CKB /CKB	1	58	59	94	62	75	62	64	53	74	59	86	59	68	52		
124	100	3FFF	S0/S1	1	69	44	62	51	56	60	50	58	67	57	59	60	24	64		
125	150	351	CKB /CKB	1	71				5		29		73	64						

	SR conditions				SR - Total SEU													
Line #	F (MHz)	Channel Mask (Hex)	Pattern	Valide	SR 1	SR 2	SR 3	SR 4	SR 5	SR 6	SR 7	SR 8	SR 9	SR 10	SR 11	SR 12	SR 13	SR 14	SR 15	SR 16
126	150	351	S0/S1	1	63				73		60		43	51						
127	200	3FF1	CKB /CKB	-1	27				1	5	1		14	33		1	3	10		
128	200	3FF1	S0/S1	1	60				113	275	81	256	65	63	67	59	39	62		
131	2	FFC7	CKB /CKB	1	9	9	9				63									
132	2	FFC7	S0/S1	1							52									
133	37.5	FFC7	CKB /CKB	1	1	1	1				68									
134	37.5	FFC7	S0/S1	1							62									
135	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
136	2	FFC7	CKB /CKB	1	10	10	10				86									
137	2	FFC7	S0/S1	1	6	6	6				62									
138	37.5	FFC7	CKB /CKB	1	16	16	16				77									
139	37.5	FFC7	S0/S1	1	9	9	9				109									
142	2	3FF	CKB /CKB	1	70	73	224	97	57	67	70	88	59	76						
143	2	3FF	S0/S1	1	77	76	108	69	74	60	57	66	73	57						
144	50	3FF	CKB /CKB	1	93	71	141	89	65	80	78	68	57	83						
146	50	3FF	S0/S1	1	66	90	138	70	72	71	78	64	73	79						
147	100	3FFF	CKB /CKB	1	78	76	172	99	84	71	90	91	108	81	106	95	87	117		
148	100	3FFF	S0/S1	1	83	88	141	76	80	83	81	74	77	94	60	70	60	76		
149	150	351	CKB /CKB	1	82				17		39		88	95						
150	150	351	S0/S1	1	80				92		83		77	80						
151	200	3FF1	CKB /CKB	-1	13				5	2	1		7	30	2		1	8		
152	200	3FF1	S0/S1	1	58				122	264	71	251	71	78	68	72	34	67		
153	200	3FF1	CKB /CKB	1	19				37	32	10	10	16	22	1		2	7		
154	200	3FF1	CKB /CKB	-1	224				28	28	51	5	82	234	22	18	10	72		
155	200	3FF1	CKB /CKB	-1	295				26	49	14		99	325	52	50	47	114		
156	200	3FF1	CKB /CKB	-1	666				29	11	7	3	86	553	27	25	31	88		
159	50	3FF	CKB /CKB	0	227	290	630	391	255	266	249	260	225	265						
160	50	3FF	CKB /CKB	0	586	568	1371	722	546	534	559	571	542	587						
162	50	3FF	CKB /CKB	1	79	89	189	129	164	167	235	242	81	84						
164	50	3FF	CKB /CKB	1	68	83	168	100	63	59	67	73	71	74						
165	50	3FF	CKB /CKB	1	93	80	179	131	72	65	76	61	70	73						
166	50	3FF	S0/S1	1	64	61	127	68	68	65	70	64	57	73						
167	100	3FFF	CKB /CKB	1	60	76	207	86	89	56	83	74	70	71	92	80	73	93		
168	100	3FFF	S0/S1	1	79	76	132	72	69	71	82	84	76	72	52	74	58	68		
169	150	351	CKB /CKB	1	64				9		62		92	141						
170	150	351	S0/S1	1	62				82		97		82	69						
171	200	3FF1	CKB /CKB	0	1				20	10	16		39	1	10	10	10	21		
173	200	3FF1	CKB /CKB	1	73				76	49	116	46	79	99	96	97	112	84		
174	200	3FF1	S0/S1	1	92				101	312	103	293	89	86	50	91	70	80		
178	2	FFC7	CKB /CKB	1	17	17	17				88									
179	2	FFC7	S0/S1	1	4	4	4				90									
180	37.5	FFC7	CKB /CKB	1	229	229	229				284									
181	37.5	FFC7	S0/S1	1							79									
182	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
183	2	FFC7	CKB /CKB	1							59									
184	2	FFC7	S0/S1	1							54									
185	37.5	FFC7	CKB /CKB	0	3131	3131	3131				3194									
189	2	FFC7	CKB /CKB	1							60									
190	2	FFC7	S0/S1	1							45									
191	37.5	FFC7	CKB /CKB	1							55									
192	37.5	FFC7	S0/S1	1							51									
194	2	3FF	CKB /CKB	1	60	49	74	69	59	67	52	52	54	44						
195	2	3FF	S0/S1	1	70	67	56	46	47	57	60	51	58	60						
196	50	3FF	CKB /CKB	1	54	59	79	51	53	54	60	51	55	49						
197	50	3FF	S0/S1	1	50	49	79	53	64	58	60	56	47	60						
198	100	3FFF	CKB /CKB	1	62	61	58	64	59	70	61	70	56	64	66	65	64	52		
199	100	3FFF	S0/S1	1	44	34	38	31	35	35	44	57	35	38	42	28	32	39		
201	150	351	CKB /CKB	1	74				13		25		54	75						
202	150	351	S0/S1	1	66				70		75		50	65						
203	200	3FF1	CKB /CKB	1	69				93	46	47	43	67	61	99	96	80	96		
204	200	3FF1	S0/S1	1	71				66	287	101	305	72	46	68	64	20	60		
205	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
207	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
208	2	3FF	CKB /CKB	1	7	8	11	7	12	10	8	9	10	8						
209	2	3FF	S0/S1	1	10	5	5	13	3	6	8	7	9	3						
210	50	3FF	CKB /CKB	1	9	11	11	12	11	18	8	10	9	7						
211	50	3FF	S0/S1	1	9	7	9	14	6	6	11	14	8	4						
212	100	3FFF	CKB /CKB	1	13	13	13	17	11	13	6	9	13	17	14	20	14	16		
213	100	3FFF	S0/S1	1	9	8	15	9	11	7	10	9	13	17	11	10	8	13		
214	150	351	CKB /CKB	1	15				2		8		7	12						
215	150	351	S0/S1	1	17				14		8		10	18						
216	200	3FF1	CKB /CKB	1	15				13	7	18	11	10	16	34	36	33	36		
217	200	3FF1	S0/S1	1	18				10	182	15	180	7	7	8	13	4	9		
219	2	FFC7	CKB /CKB	1							11									
220	2	FFC7	S0/S1	1							6									
221	37.5	FFC7	CKB /CKB	1							15									
222	37.5	FFC7	S0/S1	1							9									
223	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

12.3 SHIFT REGISTER CROSS-SECTION PER BIT - TABLE

	SR - Cross-Section / Bit															
Line #	SR 1	SR 2	SR 3	SR 4	SR 5	SR 6	SR 7	SR 8	SR 9	SR 10	SR 11	SR 12	SR 13	SR 14	SR 15	SR 16
6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
20	8.398E-08	8.398E-08	6.641E-08	5.859E-08	1.953E-09	-	-	-	-	5.078E-08	3.711E-08	1.953E-09	7.813E-09	-	-	-
21	1.337E-07	9.725E-08	4.255E-08	3.85E-08	-	-	-	-	2.026E-09	5.673E-08	6.078E-09	2.026E-09	2.026E-09	-	-	-
22	9.375E-08	8.203E-08	1.27E-07	1.27E-07	1.055E-07	8.203E-08	1.406E-07	8.594E-08	8.789E-08	8.203E-08	6.836E-08	8.203E-08	4.102E-08	8.984E-08	-	-
23	1.27E-07	1.465E-07	1.484E-07	2.051E-07	1.387E-07	1.621E-07	9.18E-08	1.055E-07	1.23E-07	1.348E-07	1.152E-07	9.961E-08	8.789E-08	1.016E-07	-	-
25	1.27E-07	-	-	-	5.273E-08	-	4.492E-08	-	1.094E-07	1.328E-07	-	-	-	-	-	-
26	1.15E-07	-	-	-	1.248E-07	-	8.966E-08	-	1.111E-07	9.746E-08	-	-	-	-	-	-
28	1.377E-07	-	-	-	1.201E-07	8.301E-08	1.367E-07	7.227E-08	1.152E-07	1.182E-07	2.646E-07	2.9E-07	2.461E-07	2.715E-07	-	-
29	1.035E-07	-	-	-	1.396E-07	9.258E-07	1.592E-07	9.424E-07	1.123E-07	1.279E-07	9.57E-08	1.191E-07	7.52E-08	1.211E-07	-	-
33	1.006E-07	1.104E-07	1.699E-07	1.201E-07	9.961E-08	1.191E-07	1.035E-07	9.473E-08	9.277E-08	9.961E-08	-	-	-	-	-	-
34	1.055E-07	8.984E-08	1.074E-07	1.055E-07	9.18E-08	9.57E-08	8.008E-08	1.064E-07	9.863E-08	8.398E-08	-	-	-	-	-	-
35	7.422E-08	7.715E-08	1.387E-07	5.664E-08	7.031E-08	8.984E-08	8.594E-08	7.715E-08	8.008E-08	8.887E-08	-	-	-	-	-	-
36	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
37	8.887E-08	8.105E-08	1.016E-07	8.301E-08	6.543E-08	6.934E-08	8.887E-08	9.18E-08	8.203E-08	9.57E-08	-	-	-	-	-	-
38	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
40	8.887E-08	9.082E-08	1.328E-07	1.641E-07	7.617E-08	8.984E-08	8.594E-08	7.715E-08	8.691E-08	7.031E-08	-	-	-	-	-	-
44	4.883E-09	4.883E-09	4.883E-09	-	-	-	3.353E-08	-	-	-	-	-	-	-	-	-
45	1.628E-09	1.628E-09	1.628E-09	-	-	-	2.832E-08	-	-	-	-	-	-	-	-	-
46	3.255E-10	3.255E-10	3.255E-10	-	-	-	2.865E-08	-	-	-	-	-	-	-	-	-
47	9.766E-10	9.766E-10	9.766E-10	-	-	-	3.418E-08	-	-	-	-	-	-	-	-	-
50	6.836E-09	6.836E-09	6.836E-09	-	-	-	3.288E-08	-	-	-	-	-	-	-	-	-
51	4.232E-09	4.232E-09	4.232E-09	-	-	-	2.995E-08	-	-	-	-	-	-	-	-	-
52	6.51E-10	6.51E-10	6.51E-10	-	-	-	2.604E-08	-	-	-	-	-	-	-	-	-
54	3.255E-10	3.255E-10	3.255E-10	-	-	-	4.134E-08	-	-	-	-	-	-	-	-	-
55	6.51E-10	6.51E-10	6.51E-10	-	-	-	3.125E-08	-	-	-	-	-	-	-	-	-
60	-	-	-	-	-	-	-	-	-	-	-	-	1.713E-06	-	-	-
62	9.277E-08	1.152E-07	1.904E-07	1.23E-07	8.789E-08	1.152E-07	9.473E-08	9.18E-08	8.691E-08	9.766E-08	-	8.301E-08	9.082E-08	8.887E-08	-	-
64	1.123E-07	9.277E-08	1.387E-07	1.211E-07	8.203E-08	9.668E-08	9.863E-08	1.045E-07	7.91E-08	7.031E-08	1.162E-07	7.227E-08	7.422E-08	9.766E-08	-	-
66	9.766E-08	-	-	-	8.301E-08	-	1.035E-07	-	1.074E-07	1.133E-07	-	-	-	-	-	-
67	1.113E-07	-	-	-	4.98E-08	-	7.031E-08	-	1.172E-07	9.863E-08	-	-	-	-	-	-
69	7.91E-08	-	-	-	1.074E-08	-	1.953E-09	-	4.785E-08	6.934E-08	3.223E-08	2.637E-08	2.539E-08	3.027E-08	-	-
70	1.318E-07	-	-	-	1.699E-07	-	1.523E-07	-	1.27E-07	1.348E-07	1.064E-07	1.016E-07	9.863E-08	1.182E-07	-	-
71	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
72	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
73	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
74	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
75	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
78	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
82	-	-	-	-	-	-	-	-	-	-	1.652E-08	4.859E-10	1.458E-09	-	-	-
83	-	4.859E-10	-	-	-	-	-	-	-	-	-	-	4.859E-10	-	-	-
84	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
85	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
86	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
87	-	-	-	-	-	1.128E-07	-	1.128E-07	-	-	-	-	4.883E-10	-	-	-
90	-	-	-	-	-	-	-	-	-	-	7.191E-08	-	4.859E-09	-	-	-
91	-	-	-	-	-	-	-	-	4.883E-10	-	-	-	-	-	-	-
92	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
93	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
94	3.401E-09	-	-	-	2.915E-09	2.915E-09	4.373E-09	3.401E-09	3.401E-09	5.83E-09	4.373E-09	6.802E-09	4.373E-09	5.344E-09	-	-
95	4.883E-10	-	-	-	-	9.57E-08	4.883E-10	9.619E-08	-	-	-	-	-	-	-	-
96	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
97	5.762E-08	4.883E-08	1.133E-07	4.395E-08	5.566E-08	4.492E-08	5.664E-08	5.566E-08	6.055E-08	4.785E-08	-	-	-	-	-	-
98	5.371E-08	5.762E-08	6.25E-08	5.078E-08	4.297E-08	4.785E-08	5.469E-08	4.785E-08	5.762E-08	5.762E-08	-	-	-	-	-	-
99	5.566E-08	5.762E-08	8.105E-08	5.664E-08	4.98E-08	5.078E-08	4.98E-08	5.469E-08	6.152E-08	4.785E-08	-	-	-	-	-	-
100	4.98E-08	5.859E-08	6.445E-08	4.492E-08	6.25E-08	5.176E-08	6.25E-08	4.688E-08	6.25E-08	4.395E-08	-	-	-	-	-	-
101	7.91E-08	5.371E-08	1.289E-07	5.859E-08	6.445E-08	5.469E-08	5.762E-08	6.055E-08	5.664E-08	7.617E-08	9.277E-08	5.566E-08	5.664E-08	5.371E-08	-	-
102	6.055E-08	5.762E-08	6.836E-08	5.762E-08	5.469E-08	6.543E-08	5.762E-08	6.934E-08	5.273E-08	4.492E-08	4.98E-08	6.152E-08	3.516E-08	5.957E-08	-	-
104	7.129E-08	-	-	-	1.172E-08	-	2.344E-08	-	5.762E-08	7.324E-08	-	-	-	-	-	-
105	5.469E-08	-	-	-	6.25E-08	-	6.445E-08	-	6.055E-08	5.371E-08	-	-	-	-	-	-
106	4.883E-09	-	-	-	5.859E-09	9.766E-09	2.93E-09	9.766E-10	1.855E-08	1.27E-08	9.766E-10	9.766E-10	9.766E-10	2.051E-08	-	-
107	7.813E-08	-	-	-	1.113E-07	3.223E-07	8.008E-08	3.066E-07	5.566E-08	7.813E-08	5.859E-08	5.957E-08	2.93E-08	5.664E-08	-	-
109	-	-	-	-	-	-	1.66E-08	-	-	-	-	-	-	-	-	-
110	-	-	-	-	-	-	1.693E-08	-	-	-	-	-	-	-	-	-
111	-	-	-	-	-	-	1.595E-08	-	-	-	-	-	-	-	-	-
112	-	-	-	-	-	-	1.66E-08	-	-	-	-	-	-	-	-	-
113	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
114	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
119	4.492E-08	4.004E-08	6.738E-08	5.078E-08	6.25E-08	4.492E-08	5.078E-08	5.371E-08	5.176E-08	5.273E-08	-	-	-	-	-	-
120	4.785E-08	4.492E-08	6.836E-08	4.883E-08	5.469E-08	4.883E-08	5.469E-08	5.762E-08	4.395E-08	5.664E-08	-	-	-	-	-	-
121	5.664E-08	4.883E-08	7.813E-08	6.445E-08	5.469E-08	4.883E-08	6.348E-08	5.664E-08	5.664E-08	6.152E-08	-	-	-	-	-	-
122	5.469E-08	6.445E-08	6.543E-08	6.055E-08	4.395E-08	5.078E-08	6.348E-08	6.641E-08	5.859E-08	5.371E-08	-	-	-	-	-	-
123	5.664E-08	5.762E-08	9.18E-08	6.055E-08	7.324E-08	6.055E-08	6.25E-08	5.176E-08	7.227E-08	5.762E-08	8.398E-08	5.762E-08	6.641E-08	5.078E-08	-	-
124	6.738E-08	4.297E-08	6.055E-08	4.98E-08	5.469E-08	5.859E-08	4.883E-08	5.664E-08	6.543E-08	5.566E-08	5.762E-08	5.859E-08	2.344E-08	6.25E-08	-	-
125	6.934E-08	-	-	-	4.883E-09	-	2.832E-08	-	7.129E-08	6.25E-08	-	-	-	-	-	-

	SR - Cross-Section / Bit															
Line #	SR 1	SR 2	SR 3	SR 4	SR 5	SR 6	SR 7	SR 8	SR 9	SR 10	SR 11	SR 12	SR 13	SR 14	SR 15	SR 16
126	6.152E-08	-	-	-	7.129E-08	-	5.859E-08	-	4.199E-08	4.98E-08	-	-	-	-	-	-
127	2.637E-08	-	-	-	9.766E-10	4.883E-09	9.766E-10	-	1.367E-08	3.223E-08	-	9.766E-10	2.93E-09	9.766E-09	-	-
128	5.859E-08	-	-	-	1.104E-07	2.686E-07	7.91E-08	2.5E-07	6.348E-08	6.152E-08	6.543E-08	5.762E-08	3.809E-08	6.055E-08	-	-
131	2.93E-09	2.93E-09	2.93E-09	-	-	-	2.051E-08	-	-	-	-	-	-	-	-	-
132	-	-	-	-	-	-	1.693E-08	-	-	-	-	-	-	-	-	-
133	3.255E-10	3.255E-10	3.255E-10	-	-	-	2.214E-08	-	-	-	-	-	-	-	-	-
134	-	-	-	-	-	-	2.018E-08	-	-	-	-	-	-	-	-	-
135	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
136	6.51E-09	6.51E-09	6.51E-09	-	-	-	5.599E-08	-	-	-	-	-	-	-	-	-
137	3.906E-09	3.906E-09	3.906E-09	-	-	-	4.036E-08	-	-	-	-	-	-	-	-	-
138	1.042E-08	1.042E-08	1.042E-08	-	-	-	5.013E-08	-	-	-	-	-	-	-	-	-
139	5.859E-09	5.859E-09	5.859E-09	-	-	-	7.096E-08	-	-	-	-	-	-	-	-	-
142	1.367E-07	1.426E-07	4.375E-07	1.895E-07	1.113E-07	1.309E-07	1.367E-07	1.719E-07	1.152E-07	1.484E-07	-	-	-	-	-	-
143	1.504E-07	1.484E-07	2.109E-07	1.348E-07	1.445E-07	1.172E-07	1.113E-07	1.289E-07	1.426E-07	1.113E-07	-	-	-	-	-	-
144	1.816E-07	1.387E-07	2.754E-07	1.738E-07	1.27E-07	1.563E-07	1.523E-07	1.328E-07	1.113E-07	1.621E-07	-	-	-	-	-	-
146	1.289E-07	1.758E-07	2.695E-07	1.367E-07	1.406E-07	1.387E-07	1.523E-07	1.25E-07	1.426E-07	1.543E-07	-	-	-	-	-	-
147	1.523E-07	1.484E-07	3.359E-07	1.934E-07	1.641E-07	1.387E-07	1.758E-07	1.777E-07	2.109E-07	1.582E-07	2.07E-07	1.855E-07	1.699E-07	2.285E-07	-	-
148	1.621E-07	1.719E-07	2.754E-07	1.484E-07	1.563E-07	1.621E-07	1.582E-07	1.445E-07	1.504E-07	1.836E-07	1.172E-07	1.367E-07	1.172E-07	1.484E-07	-	-
149	1.602E-07	-	-	-	3.32E-08	-	7.617E-08	-	1.719E-07	1.855E-07	-	-	-	-	-	-
150	1.563E-07	-	-	-	1.797E-07	-	1.621E-07	-	1.504E-07	1.563E-07	-	-	-	-	-	-
151	2.539E-08	-	-	-	9.766E-09	3.906E-09	1.953E-09	-	1.367E-08	5.859E-08	3.906E-09	-	1.953E-09	1.563E-08	-	-
152	1.133E-07	-	-	-	2.383E-07	5.156E-07	1.387E-07	4.902E-07	1.387E-07	1.523E-07	1.328E-07	1.406E-07	6.641E-08	1.309E-07	-	-
153	3.711E-08	-	-	-	7.227E-08	6.25E-08	1.953E-08	1.953E-08	3.125E-08	4.297E-08	1.953E-09	-	3.906E-09	1.367E-08	-	-
154	4.375E-08	-	-	-	5.469E-09	5.469E-09	9.961E-09	9.766E-10	1.602E-08	4.57E-08	4.297E-09	3.516E-09	1.953E-09	1.406E-08	-	-
155	5.762E-08	-	-	-	5.078E-09	9.57E-09	2.734E-09	-	1.934E-08	6.348E-08	1.016E-08	9.766E-09	9.18E-09	2.227E-08	-	-
156	1.301E-07	-	-	-	5.664E-09	2.148E-09	1.367E-09	5.859E-10	1.68E-08	1.08E-07	5.273E-09	4.883E-09	6.055E-09	1.719E-08	-	-
159	1.368E-07	1.748E-07	3.798E-07	2.357E-07	1.537E-07	1.603E-07	1.501E-07	1.567E-07	1.356E-07	1.597E-07	-	-	-	-	-	-
160	1.64E-07	1.589E-07	3.836E-07	2.02E-07	1.528E-07	1.494E-07	1.564E-07	1.598E-07	1.517E-07	1.643E-07	-	-	-	-	-	-
162	1.543E-08	1.738E-08	3.691E-08	2.52E-08	3.203E-08	3.262E-08	4.59E-08	4.727E-08	1.582E-08	1.641E-08	-	-	-	-	-	-
164	1.328E-07	1.621E-07	3.281E-07	1.953E-07	1.23E-07	1.152E-07	1.309E-07	1.426E-07	1.387E-07	1.445E-07	-	-	-	-	-	-
165	1.816E-07	1.563E-07	3.496E-07	2.559E-07	1.406E-07	1.27E-07	1.484E-07	1.191E-07	1.367E-07	1.426E-07	-	-	-	-	-	-
166	1.25E-07	1.191E-07	2.48E-07	1.328E-07	1.328E-07	1.27E-07	1.367E-07	1.25E-07	1.113E-07	1.426E-07	-	-	-	-	-	-
167	1.172E-07	1.484E-07	4.043E-07	1.68E-07	1.738E-07	1.094E-07	1.621E-07	1.445E-07	1.367E-07	1.387E-07	1.797E-07	1.563E-07	1.426E-07	1.816E-07	-	-
168	1.543E-07	1.484E-07	2.578E-07	1.406E-07	1.348E-07	1.387E-07	1.602E-07	1.641E-07	1.484E-07	1.406E-07	1.016E-07	1.445E-07	1.133E-07	1.328E-07	-	-
169	1.25E-07	-	-	-	1.758E-08	-	1.211E-07	-	1.797E-07	2.754E-07	-	-	-	-	-	-
170	1.211E-07	-	-	-	1.602E-07	-	1.895E-07	-	1.602E-07	1.348E-07	-	-	-	-	-	-
171	1.953E-09	-	-	-	3.906E-08	1.953E-08	3.125E-08	-	7.617E-08	1.953E-09	1.953E-08	1.953E-08	1.953E-08	4.102E-08	-	-
173	1.426E-07	-	-	-	1.484E-07	9.57E-08	2.266E-07	8.984E-08	1.543E-07	1.934E-07	1.875E-07	1.895E-07	2.188E-07	1.641E-07	-	-
174	1.797E-07	-	-	-	1.973E-07	6.094E-07	2.012E-07	5.723E-07	1.738E-07	1.68E-07	9.766E-08	1.777E-07	1.367E-07	1.563E-07	-	-
178	1.107E-08	1.107E-08	1.107E-08	-	-	-	5.729E-08	-	-	-	-	-	-	-	-	-
179	2.604E-09	2.604E-09	2.604E-09	-	-	-	5.859E-08	-	-	-	-	-	-	-	-	-
180	1.491E-07	1.491E-07	1.491E-07	-	-	-	1.849E-07	-	-	-	-	-	-	-	-	-
181	-	-	-	-	-	-	5.143E-08	-	-	-	-	-	-	-	-	-
182	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
183	-	-	-	-	-	-	9.603E-09	-	-	-	-	-	-	-	-	-
184	-	-	-	-	-	-	8.789E-09	-	-	-	-	-	-	-	-	-
185	5.096E-07	5.096E-07	5.096E-07	-	-	-	5.199E-07	-	-	-	-	-	-	-	-	-
189	-	-	-	-	-	-	9.766E-09	-	-	-	-	-	-	-	-	-
190	-	-	-	-	-	-	7.324E-09	-	-	-	-	-	-	-	-	-
191	-	-	-	-	-	-	8.952E-09	-	-	-	-	-	-	-	-	-
192	-	-	-	-	-	-	8.301E-09	-	-	-	-	-	-	-	-	-
194	2.93E-08	2.393E-08	3.613E-08	3.369E-08	2.881E-08	3.271E-08	2.539E-08	2.539E-08	2.637E-08	2.148E-08	-	-	-	-	-	-
195	3.418E-08	3.271E-08	2.734E-08	2.246E-08	2.295E-08	2.783E-08	2.93E-08	2.49E-08	2.832E-08	2.93E-08	-	-	-	-	-	-
196	2.637E-08	2.881E-08	3.857E-08	2.49E-08	2.588E-08	2.637E-08	2.93E-08	2.49E-08	2.686E-08	2.393E-08	-	-	-	-	-	-
197	2.441E-08	2.393E-08	3.857E-08	2.588E-08	3.125E-08	2.832E-08	2.93E-08	2.734E-08	2.295E-08	2.93E-08	-	-	-	-	-	-
198	3.027E-08	2.979E-08	2.832E-08	3.125E-08	2.881E-08	3.418E-08	2.979E-08	3.418E-08	2.734E-08	3.125E-08	3.223E-08	3.174E-08	3.125E-08	2.539E-08	-	-
199	2.148E-08	1.66E-08	1.855E-08	1.514E-08	1.709E-08	1.709E-08	2.148E-08	2.783E-08	1.709E-08	1.855E-08	2.051E-08	1.367E-08	1.563E-08	1.904E-08	-	-
201	3.613E-08	-	-	-	6.348E-09	-	1.221E-08	-	2.637E-08	3.662E-08	-	-	-	-	-	-
202	3.223E-08	-	-	-	3.418E-08	-	3.662E-08	-	2.441E-08	3.174E-08	-	-	-	-	-	-
203	3.369E-08	-	-	-	4.541E-08	2.246E-08	2.295E-08	2.1E-08	3.271E-08	2.979E-08	4.834E-08	4.688E-08	3.906E-08	4.688E-08	-	-
204	3.467E-08	-	-	-	3.223E-08	1.401E-07	4.932E-08	1.489E-07	3.516E-08	2.246E-08	3.32E-08	3.125E-08	9.766E-09	2.93E-08	-	-
205	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
207	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
208	3.418E-09	3.906E-09	5.371E-09	3.418E-09	5.859E-09	4.883E-09	3.906E-09	4.395E-09	4.883E-09	3.906E-09	-	-	-	-	-	-
209	4.883E-09	2.441E-09	2.441E-09	6.348E-09	1.465E-09	2.93E-09	3.906E-09	3.418E-09	4.395E-09	1.465E-09	-	-	-	-	-	-
210	4.395E-09	5.371E-09	5.371E-09	5.859E-09	5.371E-09	8.789E-09	3.906E-09	4.883E-09	4.395E-09	3.418E-09	-	-	-	-	-	-
211	4.395E-09	3.418E-09	4.395E-09	6.836E-09	2.93E-09	2.93E-09	5.371E-09	6.836E-09	3.906E-09	1.953E-09	-	-	-	-	-	-
212	6.348E-09	6.348E-09	6.348E-09	8.301E-09	5.371E-09	6.348E-09	2.93E-09	4.395E-09	6.348E-09	8.301E-09	6.836E-09	9.766E-09	6.836E-09	7.813E-09	-	-
213	4.395E-09	3.906E-09	7.324E-09	4.395E-09	5.371E-09	3.418E-09	4.883E-09	4.395E-09	6.348E-09	8.301E-09	5.371E-09	4.883E-09	3.906E-09	6.348E-09	-	-
214	7.324E-09	-	-	-	9.766E-10	-	3.906E-09	-	3.418E-09	5.859E-09	-	-	-	-	-	-
215	8.301E-09	-	-	-	6.836E-09	-	3.906E-09	-	4.883E-09	8.789E-09	-	-	-	-	-	-
216	7.324E-09	-	-	-	6.348E-09	3.418E-09	8.789E-09	5.371E-09	4.883E-09	7.813E-09	1.66E-08	1.758E-08	1.611E-08	1.758E-08	-	-
217	8.789E-09	-	-	-	4.883E-09	8.887E-08	7.324E-09	8.789E-08	3.418E-09	3.418E-09	3.906E-09	6.348E-09	1.953E-09	4.395E-09	-	-
219	-	-	-	-	-	-	1.79E-09	-	-	-	-	-	-	-	-	-
220	-	-	-	-	-	-	9.766E-10	-	-	-	-	-	-	-	-	-
221	-	-	-	-	-	-	2.441E-09	-	-	-	-	-	-	-	-	-
222	-	-	-	-	-	-	1.465E-09	-	-	-	-	-	-	-	-	-
223	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

12.4 SRAM CONDITIONS AND SEU - TABLES

	SRAM conditions							Fill Error Type				Check Error Type							
Line #	F (MHz)	Start Address	Stop Address	Mask (Hex)	# Bit Eff	Pattern	Valide	4	3	2	1	4	3	2	1	SCU	MCU	SEU	Cross-Section (Bit)
6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
20	20	0	16383	1FF	294912	CKB /CKB	0	0	0	0	0	0	0	360	0	355	5	360	2.44E-09
21	20	0	16383	1FF	294912	S0 S1	0	0	0	0	0	0	0	426	0	425	1	426	3.00E-09
22	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	3902	0	3896	6	3902	2.65E-08
23	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	4004	0	3995	9	4004	2.72E-08
25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
26	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
28	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	8650	0	8633	17	8650	2.93E-08
29	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	9082	0	8914	168	9082	3.08E-08
33	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	7771	0	7769	2	7771	2.64E-08
34	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	7679	0	7678	1	7679	2.60E-08
35	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	7236	0	7221	15	7236	2.45E-08
36	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
37	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	7220	0	7218	2	7220	2.45E-08
38	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	7372	0	7366	6	7372	2.50E-08
40	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	6851	0	6796	55	6851	2.32E-08
44	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
45	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
46	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
47	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
50	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
51	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
52	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
54	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
55	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
60	20	0	16383	1FF	294912	CKB /CKB	0	0	0	0	0	0	0	0	0	0	0	0	0.00E+00
62	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	7725	0	7698	27	7725	2.62E-08
64	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	7670	0	7644	26	7670	2.60E-08
66	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	7908	0	7881	27	7908	2.68E-08
67	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	8542	0	8311	231	8542	2.90E-08
69	20	0	16383	1FF	294912	CKB /CKB	0	0	0	0	0	0	0	475	0	472	3	475	1.61E-09
70	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	8299	0	8275	24	8299	2.81E-08
71	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
72	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
73	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
74	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
75	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
78	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
82	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	2181	0	2179	2	2181	3.68E-09
83	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	2240	0	2239	1	2240	3.78E-09
84	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	2253	0	2251	2	2253	3.82E-09
85	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	2334	0	2331	3	2334	3.94E-09
86	20	??	??	??	??	??	0											0	-
87	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	2353	0	2351	2	2353	3.99E-09
90	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	2319	0	2318	1	2319	3.91E-09
91	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	2265	0	2263	2	2265	3.84E-09
92	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	2384	0	2384	0	2384	4.02E-09
93	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	2396	0	2389	7	2396	4.04E-09
94	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	3585	0	3578	7	3585	6.05E-09
95	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	2535	0	2531	4	2535	4.30E-09
96	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
97	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	5299	0	5298	1	5299	1.80E-08
98	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	5297	0	5296	1	5297	1.80E-08
99	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	5528	0	5525	3	5528	1.87E-08
100	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	5258	0	5256	2	5258	1.78E-08
101	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
102	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
104	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
105	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
106	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
107	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
109	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
110	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
111	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
112	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
113	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
114	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
119	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	5215	0	5212	3	5215	1.77E-08
120	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	5146	0	5139	7	5146	1.74E-08
121	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	5396	0	5386	10	5396	1.83E-08
122	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	5321	0	5318	3	5321	1.80E-08
123	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
124	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
125	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

	SRAM conditions							Fill Error Type				Check Error Type							
Line #	F (MHz)	Start Address	Stop Address	Mask (Hex)	# Bit Eff	Pattern	Valide	4	3	2	1	4	3	2	1	SCU	MCU	SEU	Cross-Section (Bit)
126	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
127	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
128	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
131	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
132	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
133	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
134	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
135	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
136	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
137	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
138	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
139	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
142	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	5113	0	5101	12	5113	3.47E-08
143	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	5162	0	5159	3	5162	3.50E-08
144	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	5196	0	5182	14	5196	3.52E-08
146	20	0	16383	1FF	294912	FS0 FS1	1	0	0	0	0	0	0	7255	0	7244	11	7255	4.92E-08
147	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
148	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
149	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
150	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
151	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
152	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
153	-				0														-
154	-				0														-
155	-				0														-
156	-				0														-
159	20				0														-
160	20				0														-
162	20				0														-
164	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	5094	0	5002	92	5094	3.45E-08
165	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	5117	0	5099	18	5117	3.47E-08
166	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	4856	0	4848	8	4856	3.29E-08
167	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
168	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
169	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
170	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
171	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
173	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
174	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
178	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
179	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
180	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
181	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
182	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
183	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
184	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
185	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
189	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
190	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
191	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
192	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
194	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	6909	0	6905	4	6909	1.17E-08
195	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	6943	0	6941	2	6943	1.18E-08
196	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	7300	0	7293	7	7300	1.24E-08
197	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	7141	0	7139	2	7141	1.21E-08
198	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
199	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
201	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
202	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
203	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
204	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
205	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
207	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
208	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	3355	0	3350	5	3355	5.69E-09
209	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	3378	0	3362	16	3378	5.73E-09
210	20	0	16383	1FF	294912	CKB /CKB	1	0	0	0	0	0	0	3584	0	3584	0	3584	6.08E-09
211	20	0	16383	1FF	294912	S0 S1	1	0	0	0	0	0	0	3556	0	3553	3	3556	6.03E-09
212	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
213	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
214	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
215	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
216	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
217	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
219	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
220	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
221	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
222	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
223	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

12.5 UFROM / PLL - TABLES

	UFROM		PLL			
					Cross-Section	
Line #	F (MHz)	SEU	SET	SEFI	SET	SEFI
6	-	-	-	-	-	-
7	-	-	-	-	-	-
8	-	-	-	-	-	-
9	-	-	-	-	-	-
10	-	-	-	-	-	-
11	-	-	-	-	-	-
20	10	0	0	0	0	0
21	10	0	0	0	0	0
22	10	0	0	1	0	2E-06
23	10	0	3	0	6E-06	0
25	-	-	0	0	0	0
26	-	-	0	0	0	0
28	10	0	0	0	0	0
29	10	0	0	0	0	0
33	10	0	-	-	-	-
34	10	0	-	-	-	-
35	10	0	-	-	-	-
36	-	-	-	-	-	-
37	10	0	-	-	-	-
38	10	0	-	-	-	-
40	10	0	-	-	-	-
44	-	-	-	-	-	-
45	-	-	-	-	-	-
46	-	-	-	-	-	-
47	-	-	-	-	-	-
50	-	-	-	-	-	-
51	-	-	-	-	-	-
52	-	-	-	-	-	-
54	-	-	-	-	-	-
55	-	-	-	-	-	-
60	10	0	0	0	0	0
62	10	0	1	0	1E-06	0
64	10	0	2	0	2E-06	0
66	10	0	2	0	2E-06	0
67	10	0	2	1	2E-06	1E-06
69	10	0	0	0	0	0
70	10	0	3	0	3E-06	0
71	-	-	-	-	-	-
72	-	-	-	-	-	-
73	-	-	-	-	-	-
74	-	-	-	-	-	-
75	-	-	-	-	-	-
78	-	-	-	-	-	-
82	10	0	0	0	0	0
83	10	0	0	0	0	0
84	10	0	0	0	0	0
85	10	0	0	0	0	0
86	10	0	??	??	??	??
87	10	0	0	0	0	0
90	10	0	0	0	0	0
91	10	0	0	0	0	0
92	10	0	0	0	0	0
93	10	0	0	0	0	0
94	10	0	1	0	5E-07	0
95	10	0	0	0	0	0
96	-	-	-	-	-	-
97	10	0	-	-	-	-
98	10	0	-	-	-	-
99	10	0	-	-	-	-
100	10	0	-	-	-	-
101	-	-	1	0	1E-06	0
102	-	-	1	0	1E-06	0
104	-	-	2	1	2E-06	1E-06
105	-	-	1	0	1E-06	0
106	-	-	0	0	0	0
107	-	-	1	0	1E-06	0
109	-	-	-	-	-	-
110	-	-	-	-	-	-
111	-	-	-	-	-	-
112	-	-	-	-	-	-
113	-	-	-	-	-	-
114	-	-	-	-	-	-
119	10	0	-	-	-	-
120	10	0	-	-	-	-
121	10	0	-	-	-	-
122	10	0	-	-	-	-
123	-	-	2	0	2E-06	0
124	-	-	2	1	2E-06	1E-06
125	-	-	1	0	1E-06	0

	UFROM		PLL			
					Cross-Section	
Line #	F (MHz)	SEU	SET	SEFI	SET	SEFI
126	-	-	1	0	1E-06	0
127	-	-	0	0	0	0
128	-	-	0	0	0	0
131	-	-	-	-	-	-
132	-	-	-	-	-	-
133	-	-	-	-	-	-
134	-	-	-	-	-	-
135	-	-	-	-	-	-
136	-	-	-	-	-	-
137	-	-	-	-	-	-
138	-	-	-	-	-	-
139	-	-	-	-	-	-
142	10	0	-	-	-	-
143	10	0	-	-	-	-
144	10	0	-	-	-	-
146	10	0	-	-	-	-
147	-	-	1	0	2E-06	0
148	-	-	5	0	1.00E-05	0
149	-	-	3	0	6E-06	0
150	-	-	2	0	4E-06	0
151	-	-	0	0	0	0
152	-	-	0	0	0	0
153	-	-	0	0	0	0
154	-	-	1	0	2E-07	0
155	-	-	0	0	0	0
156	-	-	0	0	0	0
159	10	0	-	-	-	-
160	10	0	-	-	-	-
162	10	0	-	-	-	-
164	10	0	-	-	-	-
165	10	0	-	-	-	-
166	10	0	-	-	-	-
167	-	-	4	0	8E-06	0
168	-	-	2	0	4E-06	0
169	-	-	4	0	8E-06	0
170	-	-	0	0	0	0
171	-	-	0	0	0	0
173	-	-	1	0	2E-06	0
174	-	-	0	0	0	0
178	-	-	-	-	-	-
179	-	-	-	-	-	-
180	-	-	-	-	-	-
181	-	-	-	-	-	-
182	-	-	-	-	-	-
183	-	-	-	-	-	-
184	-	-	-	-	-	-
185	-	-	-	-	-	-
189	-	-	-	-	-	-
190	-	-	-	-	-	-
191	-	-	-	-	-	-
192	-	-	-	-	-	-
194	10	0	-	-	-	-
195	10	0	-	-	-	-
196	10	0	-	-	-	-
197	10	0	-	-	-	-
198	-	-	2	0	1E-06	0
199	-	-	1	0	5E-07	0
201	-	-	0	0	0	0
202	-	-	0	0	0	0
203	-	-	0	0	0	0
204	-	-	1	0	5E-07	0
205	-	-	-	-	-	-
207	-	-	-	-	-	-
208	10	0	-	-	-	-
209	10	0	-	-	-	-
210	10	0	-	-	-	-
211	10	0	-	-	-	-
212	-	-	0	0	0	0
213	-	-	0	0	0	0
214	-	-	0	0	0	0
215	-	-	0	0	0	0
216	-	-	0	0	0	0
217	-	-	0	0	0	0
219	-	-	-	-	-	-
220	-	-	-	-	-	-
221	-	-	-	-	-	-
222	-	-	-	-	-	-
223	-	-	-	-	-	-

12.6 CONFIGURATION - TABLE

	CONFIGURATION		
Line #	Configuration step	Result	Details
7	All	Failed	Exit 11 - Verify 0 failed at row 7419
8	All	Failed	Exit 11 - Verify 1 failed at row 3173
9	Erasing	Passed	
10	Programming	Failed	Exit 11 - Verify 0 failed at row 6166
11	Verifying	Failed	Exit 11 - Verify 0 failed at row 7246
71	All	Failed	Exit 11 - Verify 0 failed at row 7033
72	Erasing	Failed	Exit -24 - Failed to program UROW
73	Programming	Failed	Exit 11 - Failed to verify FlashROM at row 7
75	Verifying	Failed	Exit 11 - Verify 0 failed at row 7534
113	All	Failed	Exit 11 - Verify 0 failed at row 7843
114	Erasing	Failed	Exit -24 - Failed to program UROW
205	All	Failed	Exit 8 - Failed Erase Operation
223	All	Failed	Exit 8 - Failed Erase Operation

13 RADEF – NOVEMBER 2010 – RUN TABLES

13.1 RUN / BEAM / DUT / SEL / SEFI - TABLES

	RUN					BEAM										DUT											
Line #	Date	Run #	Start Time	JYFL Run #	JYFL Start time	Ion specie	Energy (MeV)	LET (MeV/(mg/cm²))	Range (µm)	Tilt (Deg)	LETeff. surface (MeV/(mg/cm²))	Fluence (#/cm²)	Run Duration (s)	Mean Flux (#/(cm²xs))	Run Dose (Rad)	SN	Total Dose (Rad)	TV	TV Version	Temperature (°C)	Vcore (V)	Vio (V)	Mode	Exposition Time (s)	SEL	SEFI
28	12/11/2010	27	10:49	2	11:51	82Kr22+	768	32	94	0	32.1	5.02E+05	210	2.39E+03	2.58E+02	11	2.58E+02	1	31	Room	1.5	3.3	Dyn	-	0	0
30	12/11/2010	29	10:58	3	11:58	82Kr22+	768	32	94	0	32.1	5.09E+05	226	2.25E+03	2.61E+02	11	5.19E+02	1	31	Room	1.5	3.3	Dyn	-	0	0
33	12/11/2010	32	11:10	4	12:09	82Kr22+	768	32	94	0	32.1	6.69E+05	230	2.91E+03	3.44E+02	11	8.63E+02	1	31	Room	1.5	3.3	Dyn	-	0	0
34	12/11/2010	33	11:15	5	12:14	82Kr22+	768	32	94	0	32.1	1.00E+06	256	3.91E+03	5.14E+02	11	1.38E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
37	12/11/2010	36	11:24	6	12:22	82Kr22+	768	32	94	0	32.1	1.00E+06	193	5.18E+03	5.14E+02	11	1.89E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
38	12/11/2010	37	11:29	7	12:27	82Kr22+	768	32	94	0	32.1	1.00E+06	194	5.15E+03	5.14E+02	11	2.40E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
39	12/11/2010	38	11:34	8	12:33	82Kr22+	768	32	94	0	32.1	1.00E+06	193	5.18E+03	5.14E+02	11	2.92E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
40	12/11/2010	39	11:40	9	12:39	82Kr22+	768	32	94	0	32.1	6.78E+05	281	2.41E+03	3.48E+02	11	3.27E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
49	12/11/2010	48	11:56	10	12:55	82Kr22+	768	32	94	0	32.1	6.00E+05	235	2.55E+03	3.08E+02	11	3.57E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
50	12/11/2010	49	12:01	11	13:00	82Kr22+	768	32	94	0	32.1	1.00E+06	380	2.63E+03	5.14E+02	11	4.09E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
65	12/11/2010	64	13:25	12	14:24	82Kr22+	768	32	94	0	32.1	6.54E+05	246	2.66E+03	3.36E+02	11	4.42E+03	2	17	Room	1.5	3.3	Dyn	-	0	0
66	12/11/2010	65	13:30	13	14:29	82Kr22+	768	32	94	0	32.1	6.52E+05	244	2.67E+03	3.35E+02	11	4.76E+03	2	17	Room	1.5	3.3	Dyn	-	0	0
67	12/11/2010	66	13:46	14	14:35	82Kr22+	768	32	94	0	32.1	6.51E+05	300	2.17E+03	3.34E+02	11	5.09E+03	2	17	Room	1.5	3.3	Dyn	-	0	0
68	12/11/2010	67	13:43	15	14:42	82Kr22+	768	32	94	0	32.1	6.45E+05	283	2.28E+03	3.31E+02	11	5.42E+03	2	17	Room	1.5	3.3	Dyn	-	0	0
70	12/11/2010	68	14:20	17	15:19	56Fe15+	523	19	97	0	18.5	8.49E+05	195	4.35E+03	2.51E+02	11	5.67E+03	2	17	Room	1.5	3.3	Dyn	-	0	0
71	12/11/2010	69	14:26	18	15:25	56Fe15+	523	19	97	0	18.5	1.12E+06	241	4.65E+03	3.32E+02	11	6.01E+03	2	17	Room	1.5	3.3	Dyn	-	0	0
72	12/11/2010	70	14:32	19	15:31	56Fe15+	523	19	97	0	18.5	1.00E+06	208	4.81E+03	2.96E+02	11	6.30E+03	2	17	Room	1.5	3.3	Dyn	-	0	0
73	12/11/2010	71	14:37	20	15:36	56Fe15+	523	19	97	0	18.5	1.00E+06	209	4.78E+03	2.96E+02	11	6.60E+03	2	17	Room	1.5	3.3	Dyn	-	0	0
75	12/11/2010	73	14:58	21	15:57	56Fe15+	523	19	97	0	18.5	1.00E+06	226	4.42E+03	2.96E+02	11	6.89E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
76	12/11/2010	74	15:04	22	16:03	56Fe15+	523	19	97	0	18.5	1.00E+06	204	4.90E+03	2.96E+02	11	7.19E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
77	12/11/2010	75	15:10	23	16:09	56Fe15+	523	19	97	0	18.5	1.00E+06	191	5.24E+03	2.96E+02	11	7.49E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
78	12/11/2010	76	15:16	24	16:14	56Fe15+	523	19	97	0	18.5	1.00E+06	238	4.20E+03	2.96E+02	11	7.78E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
80	12/11/2010	78	15:25	25	16:24	56Fe15+	523	19	97	0	18.5	1.00E+06	194	5.15E+03	2.96E+02	11	8.08E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
84	12/11/2010	81	16:44	27	17:43	131Xe35+	1217	55	89	0	55.3	5.00E+05	464	1.08E+03	4.42E+02	11	8.52E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
86	12/11/2010	83	17:00	28	17:59	131Xe35+	1217	55	89	0	55.3	5.01E+05	473	1.06E+03	4.43E+02	11	8.96E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
87	12/11/2010	84	17:09	29	18:08	131Xe35+	1217	55	89	0	55.3	5.00E+05	493	1.01E+03	4.42E+02	11	9.41E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
88	12/11/2010	85	17:19	30	18:18	131Xe35+	1217	55	89	0	55.3	5.00E+05	496	1.01E+03	4.42E+02	11	9.85E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
92	12/11/2010	89	17:52	31	18:50	131Xe35+	1217	55	89	0	55.3	5.01E+05	493	1.02E+03	4.43E+02	9	4.43E+02	1	31	Room	1.5	3.3	Dyn	-	0	0
93	12/11/2010	90	18:01	32	19:00	131Xe35+	1217	55	89	0	55.3	5.00E+05	482	1.04E+03	4.42E+02	9	8.86E+02	1	31	Room	1.5	3.3	Dyn	-	0	0
115	12/11/2010	112	20:31	33	21:30	131Xe35+	1217	55	89	0	55.3	5.00E+05	88	5.68E+03	4.42E+02	10	4.42E+02	2	17	Room	1.5	3.3	Dyn	-	0	1
116	12/11/2010	113	20:33	34	21:33	131Xe35+	1217	55	89	0	55.3	5.01E+05	381	1.31E+03	4.43E+02	10	8.86E+02	2	17	Room	1.5	3.3	Dyn	-	0	0
117	12/11/2010	114	20:43	35	21:41	131Xe35+	1217	55	89	0	55.3	5.01E+05	477	1.05E+03	4.43E+02	10	1.33E+03	2	17	Room	1.5	3.3	Dyn	-	0	0
118	12/11/2010	115	20:52	36	21:53	131Xe35+	1217	55	89	0	55.3	5.00E+05	238	2.10E+03	4.42E+02	10	1.77E+03	2	17	Room	1.5	3.3	Dyn	-	0	0
128	12/11/2010	124	22:19	38	23:17	40Ar12+	372	10	118	0	10.1	2.00E+06	216	9.26E+03	3.23E+02	16	3.23E+02	2	17	Room	1.5	3.3	Dyn	-	0	0
130	12/11/2010	126	22:24	39	23:23	40Ar12+	372	10	118	0	10.1	2.00E+06	203	9.85E+03	3.23E+02	16	6.46E+02	2	17	Room	1.5	3.3	Dyn	-	0	0
131	12/11/2010	127	22:28	40	23:27	40Ar12+	372	10	118	0	10.1	2.00E+06	188	1.06E+04	3.23E+02	16	9.70E+02	2	17	Room	1.5	3.3	Dyn	-	0	0
135	12/11/2010	-	-	41	23:46	40Ar12+	372	10	118	0	10.1	1	14	7.14E-02	1.62E-04	16	9.70E+02	1	31	Room	1.5	3.3	-	-	0	0
136	12/11/2010	131	22:49	42	23:47	40Ar12+	372	10	118	0	10.1	2.00E+06	187	1.07E+04	3.23E+02	16	1.29E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
137	12/11/2010	132	22:53	43	23:51	40Ar12+	372	10	118	0	10.1	2.01E+06	193	1.04E+04	3.25E+02	16	1.62E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
138	12/11/2010	133	22:57	44	23:55	40Ar12+	372	10	118	0	10.1	2.01E+06	197	1.02E+04	3.25E+02	16	1.94E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
139	12/11/2010	134	23:01	45	00:00	40Ar12+	372	10	118	0	10.1	2.01E+06	199	1.01E+04	3.25E+02	16	2.27E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
147	12/11/2010	142	23:13	46	00:12	40Ar12+	372	10	118	0	10.1	2.00E+06	214	9.35E+03	3.23E+02	16	2.59E+03	1	31	Room	1.5	3.3	Dyn	-	0	0
148	12/11/2010	143	23:18	47	00:17	40Ar12+	372	10	118	0	10.1	3.78E+06	389	9.72E+03	6.11E+02	16	3.20E+03	1P	31	Room	1.5	3.3	-	-	0	0
155	12/11/2010	150	23:55	49	00:54	20Ne6+	186	3.6	146	0	3.6	2.01E+06	139	1.45E+04	1.16E+02	17	1.16E+02	1	31	Room	1.5	3.3	Dyn	-	0	0
156	12/11/2010	151	23:59	50	00:57	20Ne6+	186	3.6	146	0	3.6	2.01E+06	121	1.66E+04	1.16E+02	17	2.32E+02	1	31	Room	1.5	3.3	Dyn	-	0	0
157	12/11/2010	152	00:01	51	01:00	20Ne6+	186	3.6	146	0	3.6	2.00E+06	120	1.67E+04	1.15E+02	17	3.47E+02	1	31	Room	1.5	3.3	Dyn	-	0	0
158	12/11/2010	153	00:04	52	01:03	20Ne6+	186	3.6	146	0	3.6	2.00E+06	122	1.64E+04	1.15E+02	17	4.62E+02	1	31	Room	1.5	3.3	Dyn	-	0	0
159	12/11/2010	154	00:07	53	01:07	20Ne6+	186	3.6	146	0	3.6	2.00E+06	120	1.67E+04	1.15E+02	17	5.77E+02	1	31	Room	1.5	3.3	Dyn	-	0	0
163	12/11/2010	158	00:27	54	01:26	20Ne6+	186	3.6	146	0	3.6	2.00E+06	120	1.67E+04	1.15E+02	17	6.92E+02	2	17	Room	1.5	3.3	Dyn	-	0	0
164	12/11/2010	159	00:30	55	01:29	20Ne6+	186	3.6	146	0	3.6	2.01E+06	117	1.72E+04	1.16E+02	17	8.08E+02	2	17	Room	1.5	3.3	Dyn	-	0	0
166	12/11/2010	161	00:35	56	01:33	20Ne6+	186	3.6	146	0	3.6	2.01E+06	118	1.70E+04	1.16E+02	17	9.24E+02	2	17	Room	1.5	3.3	Dyn	-	0	0
167	12/11/2010	162	00:38	57	01:37	20Ne6+	186	3.6	146	0	3.6	2.13E+06	268	7.95E+03	1.23E+02	17	1.05E+03	2P	17	Room	1.5	3.3	-	-	0	0

13.2 SHIFT REGISTER CONDITIONS AND SEU - TABLES

	SR conditions					SR - Total SEU														
Line #	F (MHz)	Channel Mask (Hex)	Reading ratio	Pattern	Valide	SR 1	SR 2	SR 3	SR 4	SR 5	SR 6	SR 7	SR 8	SR 9	SR 10	SR 11	SR 12	SR 13	SR 14	SR 15	SR 16
28	2	3FF	4/4	A-5	1	44	46	56	41	51	48	51	34	48	39	0	0	0	0	0	0
30	50	3FF	4/4	A-5	1	53	32	43	39	47	42	42	37	35	55	0	0	0	0	0	0
33	100	3FF	4/4, 1/4	A-5	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
34	100	3FF	4/4	A-5	1	112	106	120	122	93	87	104	103	72	75	0	0	0	0	0	0
37	150	3FF	4/4	A-5	1	92	101	126	117	103	103	103	103	116	105	0	0	0	0	0	0
38	150	3FF	4/4	A	1	98	118	129	105	95	98	85	87	88	95	0	0	0	0	0	0
39	150	3FF	4/4	A	1	112	112	170	112	125	144	105	106	131	142	0	0	0	0	0	0
40	150	3FF	4/4	A	1	61	65	75	54	64	64	71	70	64	71	0	0	0	0	0	0
49	200	3B9	4/4	A	1	69	0	0	52	56	34	0	43	46	62	0	0	0	0	0	0
50	200	3B9	1/4	A	1	108	0	0	115	99	82	0	66	129	109	0	0	0	0	0	0
65	2	FFFF	4/4	A	1	2	2	2	50	50	50	60	0	0	0	0	0	0	0	0	0
66	50	FFFF	4/4	A	1	0	0	0	75	75	75	59	0	0	0	0	0	0	1	1	1
67	50	FFFF	1/4	A	1	1	1	1	109	109	109	84	0	0	0	0	0	0	0	0	0
68	70	FC7F	1/4	A	1	2	2	2	46	46	46	62	0	0	0	0	0	0	0	0	0
70	70	FC7F	1/4	A	1	0	0	0	49	49	49	56	0	0	0	0	0	0	0	0	0
71	50	FFFF	1/4	A	1	0	0	0	50	50	50	53	0	0	0	0	0	0	0	0	0
72	2	FFFF	1/4	A	1	0	0	0	49	49	49	40	0	0	0	0	0	0	0	0	0
73	70	FC7F	1/4	A	1	0	0	0	48	48	48	64	0	0	0	0	0	0	0	0	0
75	2	3FF	1/4	A	1	58	63	59	52	58	55	57	59	50	44	0	0	0	0	0	0
76	50	3FF	1/4	A	1	63	51	68	63	55	45	44	40	54	55	0	0	0	0	0	0
77	100	3FF	1/4	A	1	57	48	72	68	52	57	65	54	72	60	0	0	0	0	0	0
78	150	3FF	1/4	A	1	68	61	63	77	68	68	68	68	50	63	0	0	0	0	0	0
80	200	3B9	1/4	A	1	73	0	0	86	53	41	0	29	62	59	0	0	0	0	0	0
84	200	3B9	1/4	A	1	81	0	0	112	91	81	0	59	105	71	0	0	0	0	0	0
86	150	3FF	1/4	A	1	84	83	166	88	97	98	87	87	94	70	0	0	0	0	0	0
87	100	3FF	1/4	A	1	87	87	178	88	59	77	64	72	79	73	0	0	0	0	0	0
88	50	3FF	1/4	A	1	82	74	114	89	71	66	86	73	81	88	0	0	0	0	0	0
92	50	3FF	1/4	A	1	77	81	182	84	68	70	73	75	89	95	0	0	0	0	0	0
93	2	3FF	1/4	A	1	63	84	106	83	66	77	71	80	75	64	0	0	0	0	0	0
115	2	FFFF	1/4	A	-1	1	1	1	19	19	19	11	0	0	0	0	0	0	0	0	0
116	2	FFFF	1/4	A	1	0	0	0	89	89	89	76	0	0	0	0	0	0	0	0	0
117	50	FFFF	1/4	A	1	2	2	2	158	158	158	100	0	0	0	0	0	0	1	1	1
118	70	FC7F	1/4	A	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
128	70	FC7F	1/4	A	1	0	0	0	48	48	48	53	0	0	0	0	0	0	0	0	0
130	50	FFFF	1/4	A	1	0	0	0	62	62	62	74	0	0	0	0	0	0	0	0	0
131	2	FFFF	1/4	A	1	0	0	0	51	51	51	46	0	0	0	0	0	0	0	0	0
135	-	-	-	-	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
136	2	3FF	1/4	A	1	55	58	59	53	76	71	53	52	56	57	0	0	0	0	0	0
137	50	3FF	1/4	A	1	48	59	54	57	73	69	58	53	48	67	0	0	0	0	0	0
138	100	3FF	1/4	A	1	62	60	64	70	68	68	68	47	50	69	0	0	0	0	0	0
139	150	3FF	1/4	A	1	67	58	67	67	78	79	63	63	67	72	0	0	0	0	0	0
147	200	3A1	1/4	A	1	68	0	0	447	220	64	0	66	75	66	0	0	0	0	0	0
148	-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
155	2	3FF	1/4	A	1	9	8	10	8	11	9	5	9	6	13	0	0	0	0	0	0
156	50	3FF	1/4	A	1	12	5	10	8	14	12	6	8	10	9	0	0	0	0	0	0
157	150	3FF	1/4	A	1	9	7	6	20	14	14	12	12	9	13	0	0	0	0	0	0
158	150	3FF	1/4	A	1	16	9	7	13	15	15	21	21	12	9	0	0	0	0	0	0
159	200	1B1	1/4	A	1	0	0	0	6	0	0	0	0	0	12	0	0	0	0	0	0
163	2	FFC7	1/4	A	1	0	0	0	0	0	0	8	0	0	0	0	0	0	0	0	0
164	50	FFC7	1/4	A	1	0	0	0	0	0	0	11	0	0	0	0	0	0	0	0	0
166	70	E047	1/4	A	1	0	0	0	0	0	0	15	0	0	0	0	0	0	0	0	0
167	-	-	-	-	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

13.3 SHIFT REGISTER CROSS-SECTION PER BIT - TABLE

	SR - Cross-Section / Bit														
Line #	SR 1	SR 2	SR 3	SR 4	SR 5	SR 6	SR 7	SR 8	SR 9	SR 10	SR 11	SR 12	SR 13	SR 14	SR 15	SR 16
28	8.54E-08	8.93E-08	1.09E-07	7.96E-08	9.90E-08	9.32E-08	9.90E-08	6.60E-08	9.32E-08	7.57E-08	-	-	-	-	-	-
30	1.01E-07	6.13E-08	8.23E-08	7.47E-08	9.00E-08	8.04E-08	8.04E-08	7.08E-08	6.70E-08	1.05E-07	-	-	-	-	-	-
33	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
34	1.09E-07	1.03E-07	1.17E-07	1.19E-07	9.06E-08	8.48E-08	1.01E-07	1.00E-07	7.02E-08	7.31E-08	-	-	-	-	-	-
37	8.97E-08	9.84E-08	1.23E-07	1.14E-07	1.00E-07	1.00E-07	1.00E-07	1.00E-07	1.13E-07	1.02E-07	-	-	-	-	-	-
38	9.55E-08	1.15E-07	1.26E-07	1.02E-07	9.26E-08	9.55E-08	8.28E-08	8.48E-08	8.58E-08	9.26E-08	-	-	-	-	-	-
39	1.09E-07	1.09E-07	1.66E-07	1.09E-07	1.22E-07	1.40E-07	1.02E-07	1.03E-07	1.28E-07	1.38E-07	-	-	-	-	-	-
40	8.77E-08	9.34E-08	1.08E-07	7.76E-08	9.20E-08	9.20E-08	1.02E-07	1.01E-07	9.20E-08	1.02E-07	-	-	-	-	-	-
49	1.12E-07	-	-	8.45E-08	9.10E-08	5.52E-08	-	6.99E-08	7.47E-08	1.01E-07	-	-	-	-	-	-
50	1.05E-07	-	-	1.12E-07	9.65E-08	7.99E-08	-	6.43E-08	1.26E-07	1.06E-07	-	-	-	-	-	-
65	9.95E-10	9.95E-10	9.95E-10	2.49E-08	2.49E-08	2.49E-08	8.94E-08	-	-	-	-	-	-	-	-	-
66	-	-	-	3.74E-08	3.74E-08	3.74E-08	8.82E-08	-	-	-	-	-	-	4.99E-10	4.99E-10	4.99E-10
67	5.00E-10	5.00E-10	5.00E-10	5.45E-08	5.45E-08	5.45E-08	1.26E-07	-	-	-	-	-	-	-	-	-
68	1.01E-09	1.01E-09	1.01E-09	2.32E-08	2.32E-08	2.32E-08	9.37E-08	-	-	-	-	-	-	-	-	-
70	-	-	-	1.88E-08	1.88E-08	1.88E-08	6.43E-08	-	-	-	-	-	-	-	-	-
71	-	-	-	1.45E-08	1.45E-08	1.45E-08	4.61E-08	-	-	-	-	-	-	-	-	-
72	-	-	-	1.59E-08	1.59E-08	1.59E-08	3.90E-08	-	-	-	-	-	-	-	-	-
73	-	-	-	1.56E-08	1.56E-08	1.56E-08	6.24E-08	-	-	-	-	-	-	-	-	-
75	5.65E-08	6.14E-08	5.75E-08	5.07E-08	5.65E-08	5.36E-08	5.56E-08	5.75E-08	4.87E-08	4.29E-08	-	-	-	-	-	-
76	6.14E-08	4.97E-08	6.63E-08	6.14E-08	5.36E-08	4.39E-08	4.29E-08	3.90E-08	5.26E-08	5.36E-08	-	-	-	-	-	-
77	5.56E-08	4.68E-08	7.02E-08	6.63E-08	5.07E-08	5.56E-08	6.34E-08	5.26E-08	7.02E-08	5.85E-08	-	-	-	-	-	-
78	6.63E-08	5.95E-08	6.14E-08	7.50E-08	6.63E-08	6.63E-08	6.63E-08	6.63E-08	4.87E-08	6.14E-08	-	-	-	-	-	-
80	7.12E-08	-	-	8.38E-08	5.17E-08	4.00E-08	-	2.83E-08	6.04E-08	5.75E-08	-	-	-	-	-	-
84	1.58E-07	-	-	2.18E-07	1.77E-07	1.58E-07	-	1.15E-07	2.05E-07	1.38E-07	-	-	-	-	-	-
86	1.63E-07	1.61E-07	3.23E-07	1.71E-07	1.89E-07	1.91E-07	1.69E-07	1.69E-07	1.83E-07	1.36E-07	-	-	-	-	-	-
87	1.70E-07	1.70E-07	3.47E-07	1.72E-07	1.15E-07	1.50E-07	1.25E-07	1.40E-07	1.54E-07	1.42E-07	-	-	-	-	-	-
88	1.60E-07	1.44E-07	2.22E-07	1.73E-07	1.38E-07	1.29E-07	1.68E-07	1.42E-07	1.58E-07	1.72E-07	-	-	-	-	-	-
92	1.50E-07	1.58E-07	3.54E-07	1.63E-07	1.32E-07	1.36E-07	1.42E-07	1.46E-07	1.73E-07	1.85E-07	-	-	-	-	-	-
93	1.23E-07	1.64E-07	2.07E-07	1.62E-07	1.29E-07	1.50E-07	1.38E-07	1.56E-07	1.46E-07	1.25E-07	-	-	-	-	-	-
115	6.51E-10	6.51E-10	6.51E-10	1.24E-08	1.24E-08	1.24E-08	2.14E-08	-	-	-	-	-	-	-	-	-
116	-	-	-	5.78E-08	5.78E-08	5.78E-08	1.48E-07	-	-	-	-	-	-	-	-	-
117	1.30E-09	1.30E-09	1.30E-09	1.03E-07	1.03E-07	1.03E-07	1.95E-07	-	-	-	-	-	-	6.49E-10	6.49E-10	6.49E-10
118	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
128	-	-	-	7.81E-09	7.81E-09	7.81E-09	2.58E-08	-	-	-	-	-	-	-	-	-
130	-	-	-	1.01E-08	1.01E-08	1.01E-08	3.61E-08	-	-	-	-	-	-	-	-	-
131	-	-	-	8.30E-09	8.30E-09	8.30E-09	2.24E-08	-	-	-	-	-	-	-	-	-
135	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
136	2.68E-08	2.83E-08	2.88E-08	2.68E-08	3.70E-08	3.46E-08	2.58E-08	2.53E-08	2.73E-08	2.78E-08	-	-	-	-	-	-
137	2.33E-08	2.86E-08	2.62E-08	2.76E-08	3.54E-08	3.35E-08	2.81E-08	2.57E-08	2.33E-08	3.25E-08	-	-	-	-	-	-
138	3.01E-08	2.91E-08	3.10E-08	3.39E-08	3.30E-08	3.30E-08	3.30E-08	2.28E-08	2.42E-08	3.35E-08	-	-	-	-	-	-
139	3.25E-08	2.81E-08	3.25E-08	3.25E-08	3.78E-08	3.83E-08	3.05E-08	3.05E-08	3.25E-08	3.49E-08	-	-	-	-	-	-
147	3.31E-08	-	-	2.18E-07	1.07E-07	3.12E-08	-	3.22E-08	3.65E-08	3.22E-08	-	-	-	-	-	-
148	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
155	4.36E-09	3.88E-09	4.85E-09	3.88E-09	5.33E-09	4.36E-09	2.42E-09	4.36E-09	2.91E-09	6.30E-09	-	-	-	-	-	-
156	5.82E-09	2.42E-09	4.85E-09	3.88E-09	6.79E-09	5.82E-09	2.91E-09	3.88E-09	4.85E-09	4.36E-09	-	-	-	-	-	-
157	4.39E-09	3.41E-09	2.92E-09	9.75E-09	6.82E-09	6.82E-09	5.85E-09	5.85E-09	4.39E-09	6.34E-09	-	-	-	-	-	-
158	7.80E-09	4.39E-09	3.41E-09	6.34E-09	7.31E-09	7.31E-09	1.02E-08	1.02E-08	5.85E-09	4.39E-09	-	-	-	-	-	-
159	-	-	-	2.92E-09	-	-	-	-	-	5.85E-09	-	-	-	-	-	-
163	-	-	-	-	-	-	3.90E-09	-	-	-	-	-	-	-	-	-
164	-	-	-	-	-	-	5.33E-09	-	-	-	-	-	-	-	-	-
166	-	-	-	-	-	-	7.27E-09	-	-	-	-	-	-	-	-	-
167	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

13.4 **CONFIGURATION - TABLE**

	Configuration	
Line #	Configuration step	Result
148	All	Failed Erase Operation
167	All	Verify 0 failed at row 6355

14 PIF – MARCH 2011 – RUN TABLES

14.1 RUN / BEAM / DUT / SEL - TABLES

	RUN					BEAM					DUT									
Line #	Date	Run #	Start Time	PSI Run #	PSI Start time	Energy (MeV)	Fluence (p/cm²)	Run Duration (s)	Mean Flux (p/(cm²·s))	Run Dose (Rad)	SN	Total Dose (Rad)	TV Design	TV Design Version	Temperature (°C)	Vcore (V)	Vio (V)	Mode	Exposition Time (s)	SEL
40	05/03/2011	40	19:30	1	19:23	230	1.02E+10	46	2.22E+08	5.46E+02	20	5.46E+02	1.3	1	Room	1.5	3.3	Dyn	-	0
41	05/03/2011	41	19:34	2	19:30	200	2.01E+10	101	1.99E+08	1.17E+03	20	1.72E+03	1.3	1	Room	1.5	3.3	Dyn	-	0
42	05/03/2011	42	19:40	3	19:34	151	2.01E+10	156	1.29E+08	1.40E+03	20	3.12E+03	1.3	1	Room	1.5	3.3	Dyn	-	0
43	05/03/2011	43	19:45	4	19:39	101	2.00E+10	266	7.52E+07	1.85E+03	20	4.97E+03	1.3	1	Room	1.5	3.3	Dyn	-	0
44	05/03/2011	44	19:51	5	19:45	75.3	2.00E+10	387	5.18E+07	2.31E+03	20	7.29E+03	1.3	1	Room	1.5	3.3	Dyn	-	0
45	05/03/2011	45	20:14	6	20:07	50.9	2.00E+10	525	3.81E+07	3.12E+03	20	1.04E+04	1.3	1	Room	1.5	3.3	Dyn	-	0
46	05/03/2011	46	20:25	7	20:19	75.3	2.01E+10	388	5.17E+07	2.32E+03	20	1.27E+04	1.3	1	Room	1.5	3.3	Dyn	-	0
47	05/03/2011	47	20:35	8	20:28	23.5	2.82E+09	174	1.62E+07	8.04E+02	20	1.35E+04	1.3	1	Room	1.5	3.3	Dyn	-	0
48	05/03/2011	48	20:45	9	20:39	23.5	5.76E+09	355	1.62E+07	1.64E+03	20	1.52E+04	1.3	1	Room	1.5	3.3	Dyn	-	0
49	05/03/2011	49	20:57	10	20:51	23.5	4.85E+09	300	1.62E+07	1.38E+03	20	1.65E+04	1.3	1	Room	1.5	3.3	Dyn	-	0
						23.5	1.34E+10	829	1.62E+07											
51	05/03/2011	51	21:12	11	21:07	230	1.00E+10	45	2.23E+08	5.36E+02	19	0.00E+00	1.3	1	Room	1.5	3.3	Dyn	-	0
52	05/03/2011	52	21:16	12	21:09	101	1.00E+10	134	7.47E+07	9.27E+02	19	5.36E+02	1.3	1	Room	1.5	3.3	Dyn	-	0
55	05/03/2011	55	21:40	13	21:35	230	1.02E+10	45	2.26E+08	5.43E+02	19	2.01E+03	1.1	1	Room	1.5	3.3	Dyn	-	0
56	05/03/2011	56	21:45	14	21:38	230	1.00E+10	45	2.22E+08	5.34E+02	19	2.54E+03	1.1	1	Room	1.5	3.3	Dyn	-	0
58	05/03/2011	58	21:51	15	21:44	230	6.45E+10	288	2.24E+08	3.44E+03	19	5.98E+03	1.1	1	Room	1.5	3.3	Dyn	-	0
60	05/03/2011	60	22:05	16	21:58	230	1.75E+10	78	2.25E+08	9.36E+02	19	6.92E+03	1.1	1	Room	1.5	3.3	Dyn	-	0
61	05/03/2011	61	22:16	17	22:09	230	1.00E+11	447	2.24E+08	5.35E+03	19	1.23E+04	1.1	1	Room	1.5	3.3	Dyn	-	0
63	05/03/2011	63	22:26	18	22:19	230	2.68E+10	119	2.25E+08	1.43E+03	19	1.37E+04	1.1	1	Room	1.5	3.3	Dyn	-	0
65	05/03/2011	65	22:44	19	22:37	230	1.00E+11	450	2.22E+08	5.34E+03	19	1.90E+04	1.1	1	Room	1.5	3.3	Dyn	-	0
66	05/03/2011	66	22:54	20	22:47	230	3.76E+10	168	2.24E+08	2.01E+03	19	2.10E+04	1.1	1	Room	1.5	3.3	Dyn	-	0
68	05/03/2011	68	23:03	21	22:56	230	1.00E+11	444	2.26E+08	5.35E+03	19	2.64E+04	1.1	1	Room	1.5	3.3	Dyn	-	0
69	05/03/2011	69	23:12	22	23:05	230	1.50E+10	66	2.27E+08	7.98E+02	19	2.72E+04	1.1	1	Room	1.5	3.3	Dyn	-	0
71	05/03/2011	71	23:25	23	23:18	230	8.92E+09	39	2.29E+08	4.76E+02	19	2.77E+04	1.1	1	Room	1.5	3.3	Dyn	-	0
73	05/03/2011	73	23:31	24	23:24	230	4.21E+10	187	2.25E+08	2.25E+03	19	2.99E+04	1.1	1	Room	1.5	3.3	Dyn	-	0
76	06/03/2011	76	00:06	25	00:04	230	3.71E+10	166	2.24E+08	1.98E+03	21	1.98E+03	1.1	1	Room	1.5	3.3	Dyn	-	0
85	06/03/2011	85	00:36	26	00:29	230	1.95E+10	87	2.24E+08	1.04E+03	21	3.02E+03	1.2	1	Room	1.5	3.3	Dyn	-	0
86	06/03/2011	86	00:43	27	00:36	230	1.38E+10	62	2.22E+08	7.36E+02	21	3.76E+03	1.2	1	Room	1.5	3.3	Dyn	-	0
87	06/03/2011	87	00:45	28	00:38	230	8.86E+09	39	2.27E+08	4.73E+02	21	4.23E+03	1.2	1	Room	1.5	3.3	Dyn	-	0
88	06/03/2011	88	00:46	29	00:48	230	3.33E+09	15	2.22E+08	1.78E+02	21	4.41E+03	1.2	1	Room	1.5	3.3	Dyn	-	0

14.2 SHIFT REGISTER CONDITIONS AND SEU - TABLES

	SR conditions					SR - Total SEU														
Line #	F (MHz)	Channel Mask (Hex)	Reading ratio	Pattern	Valide	SR 1	SR 2	SR 3	SR 4	SR 5	SR 6	SR 7	SR 8	SR 9	SR 10	SR 11	SR 12	SR 13	SR 14	SR 15	SR 16
40	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
41	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
42	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
43	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
44	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
45	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
46	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
47	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
48	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
49	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
51	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
52	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
55	2	3FF	4/4	A		1	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0
56	50	3FF	4/4	A		0	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0
58	100	FF	4/4	A		2	2	2	2	2	2	2	2	0	0	0	0	0	0	0	0
60	200	1	4/4	A		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
61	200	1	4/4	A		2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
63	150	35F	4/4	A		0	0	2	1	1	1	2	0	2	1	0	0	0	0	0	0
65	150	35F	4/4	A		2	1	2	2	2	0	2	0	2	2	0	0	0	0	0	0
66	50	3FF	4/4	A		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
68	50	3FF	4/4	A		2	2	2	2	2	2	2	2	2	2	0	0	0	0	0	0
69	2	3FF	4/4	A		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
71	2	3FF	4/4	A		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
73	2	3FF	4/4	A		0	1	0	1	0	0	1	1	0	1	0	0	0	0	0	0
76	100	3FF	4/4	A		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
85	190	3C00	4/4	A		0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0
86	190	3C00	4/4	A		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
87	190	3C00	4/4	A		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
88	190	3C00	4/4	A		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

14.3 SHIFT REGISTER CROSS-SECTION PER BIT - TABLES

	SR - Cross-Section / Bit															
Line #	SR 1	SR 2	SR 3	SR 4	SR 5	SR 6	SR 7	SR 8	SR 9	SR 10	SR 11	SR 12	SR 13	SR 14	SR 15	SR 16
40	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
41	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
42	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
43	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
44	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
45	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
46	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
47	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
48	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
49	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
51	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
52	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
55	9.57E-14	-	-	9.57E-14	9.57E-14	-	-	-	9.57E-14	9.57E-14	-	-	-	-	-	-
56	-	-	9.75E-14	-	9.75E-14	9.75E-14	9.75E-14	9.75E-14	-	-	-	-	-	-	-	-
58	3.02E-14	3.02E-14	3.02E-14	3.02E-14	3.02E-14	3.02E-14	3.02E-14	3.02E-14	-	-	-	-	-	-	-	-
60	5.56E-14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
61	1.95E-14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
63	-	-	7.27E-14	3.64E-14	3.64E-14	3.64E-14	7.27E-14	-	7.27E-14	3.64E-14	-	-	-	-	-	-
65	1.95E-14	9.74E-15	1.95E-14	1.95E-14	1.95E-14	-	1.95E-14	-	1.95E-14	1.95E-14	-	-	-	-	-	-
66	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
68	1.95E-14	1.95E-14	1.95E-14	1.95E-14	1.95E-14	1.95E-14	1.95E-14	1.95E-14	1.95E-14	1.95E-14	-	-	-	-	-	-
69	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
71	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
73	-	2.31E-14	-	2.31E-14	-	-	2.31E-14	2.31E-14	-	2.31E-14	-	-	-	-	-	-
76	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
85	-	-	-	-	-	-	-	-	-	-	-	4.98E-14	-	4.98E-14	-	-
86	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
87	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
88	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

14.4 SRAM / UFROM - TABLES

	SRAM																			UFROM	
	SRAM conditions							Fill Error Type				Check Error Type									
Line #	F (MHz)	Start Address	Stop Address	Mask (Dec)	# Bit Eff	Pattern	Valide	4	3	2	1	4	3	2	1	SCU	MCU	SEU	Cross-Section/Bit (cm²)	F (MHz)	SEU
40	20	0	6FFF	511	516096	CKB /CKB	1	0	0	0	0	0	0	409	0	408	8	416	7.887E-14	10	0
41	20	0	6FFF	511	516096	CKB /CKB	1	0	0	0	0	0	0	737	0	727	34	761	7.32141E-14	10	0
42	20	0	6FFF	511	516096	CKB /CKB	1	0	0	0	0	0	0	603	0	602	2	604	5.82541E-14	10	0
43	20	0	6FFF	511	516096	CKB /CKB	1	0	0	0	0	0	0	676	0	676	0	676	6.54917E-14	10	0
44	20	0	6FFF	511	516096	CKB /CKB	0	0	0	0	0	0	0	0	0	0	0	0	0	10	0
45	20	0	6FFF	511	516096	CKB /CKB	1	0	0	0	0	0	0	844	0	844	0	844	8.1686E-14	10	0
46	20	0	6FFF	511	516096	CKB /CKB	1	0	0	0	0	0	0	707	0	707	0	707	6.83242E-14	10	0
47	20	0	6FFF	511	516096	CKB /CKB	1	0	0	0	0	0	0	41	0	41	0	41	2.81512E-14	10	0
48	20	0	6FFF	511	516096	CKB /CKB	1	0	0	0	0	0	0	144	0	144	0	144	4.84743E-14	10	0
49	20	0	6FFF	511	516096	CKB /CKB	1	0	0	0	0	0	0	138	0	138	0	138	5.5121E-14	10	0
					516096			0	0	0	0	0	0	323	0	323	0	323	4.66046E-14		
51	20	0	6FFF	511	516096	CKB /CKB	1	0	0	0	0	0	0	389	0	389	0	389	7.51481E-14	10	0
52	20	0	6FFF	511	516096	CKB /CKB	1	0	0	0	0	0	0	312	0	312	0	312	6.03935E-14	10	0
55	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
56	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
58	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
60	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
61	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
63	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
65	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
66	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
68	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
69	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
71	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
73	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
76	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
85	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
86	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
87	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
88	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15 Acronyms and Abbreviations

CCC: Clock Conditioning Circuit
CMOS: Complementary Metal-Oxide-Semiconductor
DDR: Double Data Rate
DDR2SDRAM: Double Data Rate (version 2) Synchronous Dynamic Random Access Memory
DUT: Device Under Test
EDAC: Error Detection And Correction
FF: Flash Freeze
FPGA: Field Programmable Gate Array
FROM: Flash Read Only Memory
HI: Heavy Ion
ISP: In System Programming
LVCMOS: Low Voltage CMOS
LVDS: Low Voltage Differential Signaling.
MBU: Multi-Bit Upset
MCU: Multi-Cell Upset
UFROM: User FROM
PLL: Phase-locked Loop
ROM: Read Only Memory
SBU: Single Bit Upset
SCU: Single Cell Upset
SDR: Single Data Rate
SEB: Single-Event Burnout
SEE: Single-Event Effect
SEFI: Single-Event Functional Interrupt
SEGR: Single-Event Gate Rupture
SEL: Single-Event Latch-up
SET: Single-Event Transient
SEU: Single-Event Upset
SPI: Serial Programming Interface
SRAM: Static Random Access Memory
TMR: Triple Module Redundancy