GR740 Radiation Summary

Test Report

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1.3	2020-09-28	8	Minor text editing performed.

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1 INTRODUCTION

1.1 Scope of the document

This document consists of a summary of the GR740 radiation performance. The GR740 is a radiation-hardened system-on-chip that features a quad-core fault-tolerant LEON4 processor [RD1], developed by Cobham Gaisler. The GR740 is implemented in the 65nm CMOS technology platform for space applications developed by STMicroelectronics (C65SPACE) [RD3].

This work has been performed by Cobham Gaisler AB, Gothenburg, Sweden, with the collaboration of Roland Weigand from ESA/ESTEC. The work is funded by the European Space Agency under ESTEC contract 4000122419/17/NL/LF. The present document is a deliverable document of this contract and it shall be published on the ESCIES's website.

1.2 Applicable documents

The following documents contain requirements applicable to the contents of the document:

[AD1] ESCC Basic Specification No. 25100, Issue 2, October 2014.

[AD2] "Test Method Standard – Microcircuits - Ionizing Radiation (Total Dose) Test Procedure," Department of Defense – United States of America, MIL-STD-883K, TM1019.9, February 2017.

1.3 Reference documents

The following documents are referred as they contain relevant information:

[RD1] "GR740 Quad Core LEON4 SPARC V8 Processor," Cobham Gaisler, GR740-UM-DS-2-0, Version 2.0, July 2018.

Available online at: https://www.gaisler.com/GR740

[RD2] "GR740 Quad Core LEON4 SPARC V8 Processor," Cobham Gaisler, GR740-UM-DS-1-10, Version 1.10, July 2018.

Available online at: https://www.gaisler.com/GR740

[RD3] "A Commercial 65nm CMOS Technology for Space Applications: Heavy Ion, Proton and Gamma Test Results and Modeling," P. Roche, G. Gasiot, S. Uznanski, J.-M. Daveau, J. Torras-Flaquer, S. Clerc, and R. Harboe-Sørensen. European Conference on Radiation and Its Effects on Components and Systems, 2009.

[RD4] "ST 65nm a Hardened ASIC Technology for Space Applications," L. Hili, P. Roche, and F. Malou, 2016 European Space Components Conference, 2016.

[RD5] "TID and SEE Characterization of Rad-Hardened 1.2 GHz PLL IP from New ST CMOS 65nm Space Technology," F. Malou, G. Gasiot, R. Chevallier, L. Dugoujon, and P. Roche, 2014 IEEE Radiation Effects Data Workshop, July 2014.

[RD6] "Detailed SET Characterization of a 65nm Bulk Technology," A. Evans, M. Glorieux, and D. Alexandrescu, Presentation at the Single Event Effects Symposium, La Jolla, USA, May 2016.

[RD7] "Heavy Ions Test Result on a 65nm Sparc-V8 Radiation-Hard Microprocessor," C. Bottoni, M. Glorieux, J. M. Daveau, G. Gasiot, F. Abouzeid, S. Clerc, L. Naviner, and P. Roche. 2014 IEEE International Reliability Physics Symposium, June 2014.

[RD8] "GR-CPCI-GR740 Development Board User's Manual," Cobham Gaisler, GR-CPCI-GR740-UM, Version 1.7, September 2017.

Available online at: https://www.gaisler.com/GR-CPCI-GR740

[RD9] "GRLIB IP Core User's Manual," Cobham Gaisler, Version 2018.1, April 2018.

Available online at: https://www.gaisler.com/index.php/products/ipcores/soclibrary.

[RD10] "GRMON2 User's Manual," Cobham Gaisler, Version 2.0.93, April 2018.

Available online at: https://www.gaisler.com/GRMON

[RD11] "The OMERE Software," TRAD.

Available online at: http://www.trad.fr/en/space/omere-software

[RD12] "GR740 Technical Note on Benchmarking and Validation," Cobham Gaisler, GR740-VALT-0010, Version 3.3., January 2019.

Available online at: https://www.gaisler.com/GR740

1.4 Abbreviations

APV	Access Protection Vectors
ASIC	Application Specific Integrated Circuit
BCH	Bose Chaudhuri Hocquenghem
BTMR	Block Triple Modular Redundancy
CMOS	Complementary Metal Oxide Semiconductor
DMR	Double Modular Redundancy
DUT	Device Under Test
ESCIES	European Space Components Information Exchange System
ESA	European Space Agency
ESTEC	European Space Research and Technology Centre
FF	Flip Flop
FPGA	Field Programmable Gate Array
FPU	Float Point Unit
GEO	Geostationary Orbit
HIF	Heavy Ion Facility (at UCL)
I²C	Inter-Integrated Circuit
I/O	Input/Output

IOMMU	Input-Output Memory Management Unit
IP	Intellectual Property
JYU	University of Jyväskylä
L1	Level 1
L2	Level 2
LEO	Low Earth Orbit
LET	Linear Energy Transfer
LIF	Low Ion Facility (at UCL)
LSL	Lower Specification Limit
LVDS	Low-Voltage Differential Signaling
MBU	Multiple Bit Upset
PDMR	Parity Double Modular Redundancy
PLL	Phase-Locked Loop
RADEF	Radiation Effects Facility (at JYU)
RAM	Random-Access Memory
RHBD	Radiation Hardened by Design
RPP	Rectangular Parallelepiped
SDC	Silent Data Corruption
SDRAM	Synchronous Dynamic Random-Access Memory
SECDED	Single Error Correction, Double Error Detection
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEL	Single Event Latch-up
SRAM	Static Random-Access Memory
TCL	Tool Command Language
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
UART	Universal Asynchronous Receiver-Transmitter
UCL	Université Catholique de Louvain
USL	Upper Specification Limit

2 SUMMARY

This document presents the radiation performance of the GR740 system-on-chip developed by Cobham Gaisler [RD1] and implemented in the 65nm CMOS technology platform for space applications developed by STMicroelectronics (C65SPACE) [RD3].

The radiation performance data is based on test data collected from several radiation test campaigns performed by Cobham Gaisler with the prototype silicon (silicon revision 0) and the flight silicon (silicon revision 1). In addition, data publicly available from STMicroelectronics for the C65SPACE technology is also presented herein.

The following radiation performances of the GR740 have been demonstrated:

- An overall SEE error rate below 1E-5 events/device/day for typical space orbits[1].
- SEL immunity up to an LET of 125 MeV.cm²/mg (tested with elevated temperature - > 85 ºC - and maximum supply voltages).
- TID tolerance of 300 krad(Si).

This document provides motivation for these claims and reports how these performances have been proven.

The low functional error rate recorded in the application level tests under irradiation demonstrates that although an extensive amount of SEUs in the internal memory cells of the GR740 have been recorded, all events were successfully mitigated and corrected. There is no evidence of error build-up in the GR740.

[1] The Weibull parameters used to calculate the SEE error rates are provided further in this document.

3 DEVICE DESCRIPTION

The GR740 device is a system-on-chip featuring a quad-core fault-tolerant LEON4 SPARC V8 processor designed for high-performance general-purpose processing [RD1]. The architecture is suitable for both symmetric and asymmetric multiprocessing. The GR740 is the latest and highest performing processor in the line of European LEON processors based on the SPARC32 instruction set architecture [RD13]. The processor continues the evolution towards system-on-chip devices that allow a high-level of integration by adding additional computational power and additional devices in one integrated circuit while at the same time preserving software compatibility with previous generations of European space-grade microprocessors. The GR740 is implemented in the 65nm CMOS technology platform for space applications developed by STMicroelectronics (C65SPACE) [RD3]. Figure 1 provides an overview of the GR740 architecture. A full explanation of the functionalities embedded within the GR740 can be found in the datasheet of the device [RD1].

In line with previous generations of LEON-based processors, the fault-tolerance aims at allowing uninterrupted software execution in the presence of correctable errors. The architecture provides extensive means to keep statistics of correctable errors but their presence does not interrupt software execution. The first and foremost goal in the event of encountering un-correctable errors is to guarantee that faulty state is never propagated outside of the microprocessor device. The work and results described in this report focuses on the on-chip capabilities of the GR740. However, it is also important to highlight that error detection and correction capabilities also exist for external memories. In this context, the GR740 device introduces a novel concept of switching the coding used to protect external memories in order to regain fault resilience even when the function of one external memory device has been lost.

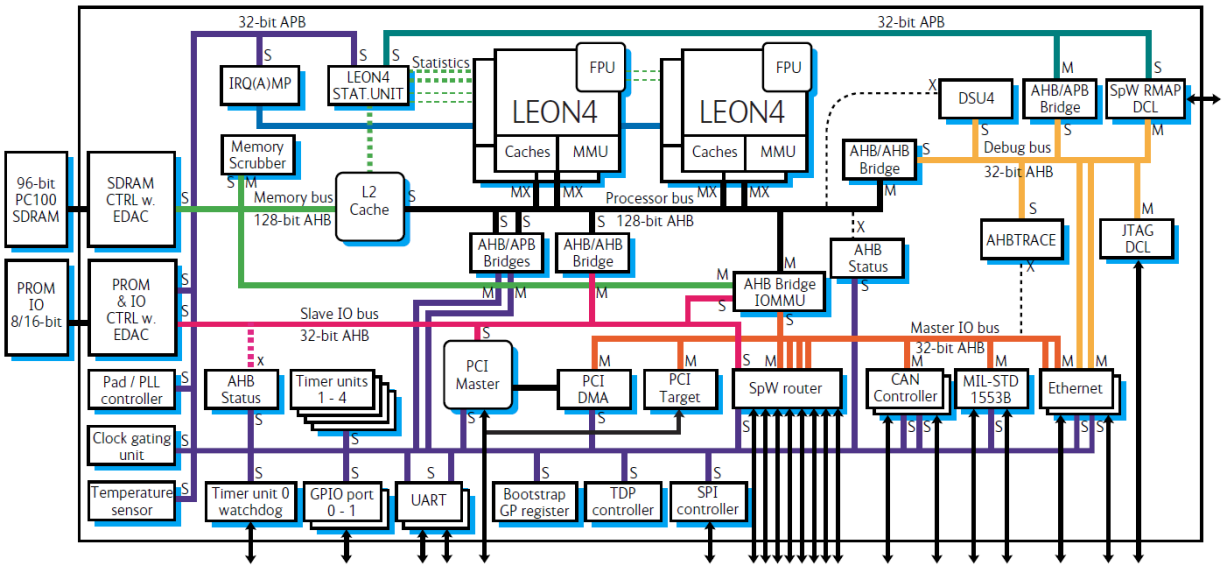

Figure 1. Overview of the GR740 architecture [RD1].

3.1 GR740 radiation hardening design approach

During the design phase of the GR740, Cobham Gaisler selected the C65SPACE technology as being the state-of-art radiation hardened ASIC technology in Europe. In the choice of using or not SEU hardened cells of the C65SPACE, each individually block and function in GR740 has been optimized for the best performance. In many cases, SEU sensitive cells, such as SRAMs, are used together with a mitigation scheme based on redundancy.

Table 1 compiles the different memory cell types used in the GR740, the total amount used of each one, and the hardening approaches selected for them.

The four processor cores in the GR740 have register files containing CORELIB flip-flops (non-SEU hardened) [RD3]. A Block TMR (BTMR) correction scheme, with bit-by-bit voting on the register read data outputs, is implemented in the register files to mask SEUs in the CORELIB FFs. In addition, the modules of the BTMR have adequate spacing among them to avoid sensitivity to potential uncorrectable MBUs. The L1 cache of each processor cores is composed of SRAM cells and includes an 8+1 parity error detection system with invalidation on error scheme. The L2 cache is also composed of SRAM cells and includes a 32+7 BCH SECDED scheme. Scrambling of all memory cells, one bit every four from the same word, is used to minimize the possibility of MBUs within one word. The SpaceWire and the Ethernet IPs also include blocks implemented with SRAM cells. These are protected either with TMR or PDMR (Parity DMR). All other memory cells and sequential logic in the GR740 are composed of SKYROB flip-flops (SEU hardened) [RD3] that do not require mitigation at design level thanks to its RHBD approach at ASIC library level. In addition, three RHBD PLLs are used in the GR740 and all global clocks and reset networks are SET hardened at ASIC library level.

Table 1. Memory cell types and hardening approaches in the GR740.

Memory cell type	Total number of bits	Hardening approach
SKYROB FFs	122,014	RHBD
CORELIB FFs	64,128	Block TMR
SRAM cells	24,360,704	Parity, SECDED, PDMR, or TMR

4 BACKGROUND CHARACTERIZATION AND RADIATION ASSESSMENT

This chapter presents a background of the radiation assessment of the GR740 device based on data from the C65SPACE technology and test results from the prototype (revision 0) version of the GR740. Several radiation test campaigns were performed in 2016 with the prototype silicon, in which both static and dynamic data results were collected. Due to an errata related to the L2 cache of the revision 0 silicon [RD2], no useful dynamic radiation test results with L2 cache enabled could be obtained in those campaigns. However, the static tests from those campaigns provided useful data that is reported in this section.

NOTE: Chapter 5 presents complete dynamic SEE data test results of the GR740 flight silicon, including results from dynamic tests using the L2 cache. Chapter 6 presents the SEL characterization of the GR740 flight silicon. Chapter 8 presents the TID radiation verification test performed in the GR740 flight silicon.

4.1 Single event effects

4.1.1 C65SPACE technology

The STMicroelectronics' C65SPACE technology is a derivation from a commercial CMOS 65 nm technology in which the standard cells library was hardened by design to improve its performance with regards to radiation-induced effects. The C65SPACE technology is immune to SELs, has a high tolerance for TID and it includes both SEU/SET hardened and non-hardened logic.

The publicly available SEE data for the C65SPACE technology is based on measurements carried out by STMicroelectronics on various test vehicles [RD3 – RD7]. The most relevant data for the GR740 device is based on the KIPSAT test vehicle, which contains shift registers with non-hardened (CORELIB FFs) and hardened (SKYROB FFs) flip-flops, a dual-port SRAM, three SPARC V8 microprocessors, and two microcontrollers. Both proton and heavy ion tests were performed in this test vehicle, and more details can be found in the reference documents [RD3 – RD7].

4.1.2 Results from the prototype version of the GR740

4.1.2.1 Heavy ion test results overview

NOTE: The SEE results obtained with the GR740 flight silicon (revision 1) are reported in Chapter 5 of this document. This Section reports other relevant SEE data collected with the GR740 prototype silicon (revision 0).

Three heavy ion irradiation test campaigns were performed by Cobham Gaisler during 2016 with the prototype (revision 0) version of the GR740 device. One campaign was performed at JYU/RADEF on week 17 and two at UCL/HIF, one on week 25 and the other on week 48.

Static and dynamic tests were performed. The static tests were focused on evaluating the SEU characteristics of the memory elements of the GR740. Concerning the dynamic tests, several application level test cases were executed, such as: dynamic test of the L1 cache memory(ies) in single- and multi-core modes, FPU-based test, 8-port SpaceWire test, and Ethernet test. The frequency of operation during the dynamic tests varied from 10 MHz (with the system PLL bypassed) to 250 MHz (50 MHz input clock with the x5 system PLL enabled). The dynamic test of

the L2 cache could not be achieved with the prototype silicon (revision 0) because of an errata with the L2 cache functionality [RD2]. A permanent solution via a re-spin of the die was implemented for the flight silicon (revision 1) to solve the issue.

The SEU cross section of various elements of the GR740, e.g., FFs, SRAM cells, and PLL were estimated and, whenever possible, compared with data from the C65SPACE technology. The results obtained for these elements with the static tests agree with the data known from the C65SPACE's test vehicles.

4.1.2.2 Proton test results summary

NOTE: The SEE results obtained with the GR740 flight silicon (revision 1) are reported in Chapter 5 of this document. This Section reports other relevant SEE data collected with the GR740 prototype silicon (revision 0).

One proton irradiation test campaign was performed in 2016 with the prototype (revision 0) version of the GR740 device with the purpose of verifying the results previously obtained with heavy ions. The campaign was performed at UCL/LIF on week 49.

The main objectives of the proton test campaign were the following: 1) to study the proton characteristics of the GR740; 2) to evaluate the occurrence of functional errors due to proton-induced events. The test setup, software, and conditions were similar to the ones described in Chapter 5, with the exception that dynamic tests using L2 cache could not be performed. The main results obtained are as follow:

- Memory cells:
  - All the results obtained for the SKYROB and CORELIB FFs and SRAM cells were in agreement with the data known from the C65SPACE's test vehicles.
- Application level tests:
  - Functional errors under proton irradiation were very rare. In order to record any event, the test fluence had be increased beyond the test requirements of 1E+11 p/cm² [AD1]. Table 2 summarizes the average cross section results obtained for functional errors collected over multiple test runs using the same test cases as of the heavy ion tests. No statistical differences in cross section were observed among the tested energies.

Table 2. GR740 average cross section results for functional errors versus proton energy.

Energy (MeV)	Integrated fluence (p/cm²)	Cross section (cm²/device)
10.00	1.49E+12	2.01E-12
30.10	2.10E+11	< 4.76E-12
62.00	1.68E+12	3.58E-12

- PLL:
  - No PLL loss of lock events were recorded during the proton test campaign of the GR740 for an integrated fluence of 3.37E+12 p/cm² (10-62 MeV). Therefore, one can consider that the PLLs are insensitive to proton-induced SEEs for the tested proton energy range. This result is also applicable to the GR740 flight silicon (revision 1), which uses the same PLLs.

Based on the obtained results, which agreed with the data known from the C65SPACE's test vehicles, and the recorded LET threshold with heavy ions (2.20 MeV.cm²/mg), one can conclude that:

- The results obtained for the memory cells of the GR740 prototype silicon (silicon revision 0) are fully applicable to the GR740 flight silicon (silicon revision 1);
- The GR740 is immune to functional errors from direct proton ionization-induced effects.

4.2 Single event latch-up

NOTE: The SEL immunity of the GR740 flight silicon (revision 1) was confirmed at maximum operating voltages and elevated temperature and is reported in Chapter 6 of this document. This section reports other relevant SEL data about the C65SPACE technology and collected with the GR740 prototype silicon (revision 0).

According to the publicly available data for the C65SPACE technology [RD3 – RD7], the technology is SEL free for ions with LET up to 60 MeV.cm²/mg when tested at the worst operating conditions and high temperature (125 °C).

The GR740 SEL immunity was initially tested by Cobham Gaisler at standard operating conditions and room temperature during the SEE test campaigns with both prototype (revision 0) and flight (revision 1) silicon versions. The prototype silicon was tested up to an effective LET of 98 MeV.cm²/mg and the flight silicon up to an effective LET of 125 MeV.cm²/mg (see Chapter 7). No SEL events were recorded in any of the test runs.

5 HEAVY ION SEE CHARACTERIZATION – GR740 FLIGHT SILICON

This chapter is a summary of the heavy ion-induced SEE test campaign performed by Cobham Gaisler at the UCL/HIF facility, in Louvain-la-Neuve, Belgium, on week 22, 2018, with the flight silicon (revision 1) version of the GR740 device.

5.1 Test setup and procedure

This section reports on the test setup and procedure for the results reported in this chapter.

5.1.1 Organization of the activities

The tested devices were provided by STMicroelectronics already delidded. The test setup and software were developed by Cobham Gaisler, and they are based on successful past irradiation tests. The entire setup was checked before the campaign at Cobham Gaisler premises through error injection campaigns. The test was carried out according to the ESCC25100 specification [AD1].

5.1.2 Tested samples

Table 3. Tested samples.

Device identification	GR740, silicon revision 1
Packaging	LGA625 (Ceramic Land Grid Array)
Wafer processing date	2018
Diffusion lot number	Q801934
Serial numbers	001, 002

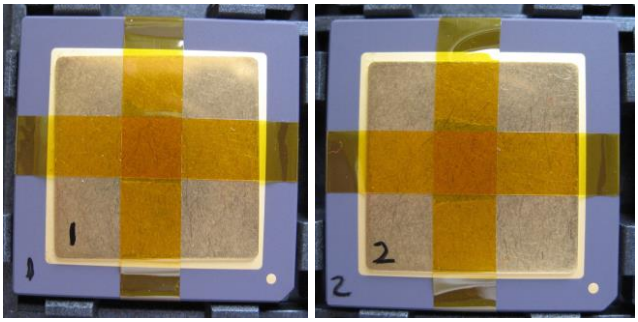

Figure 2. View of the tested samples (device 001 on the left and device 002 on the right) with the protection lid.

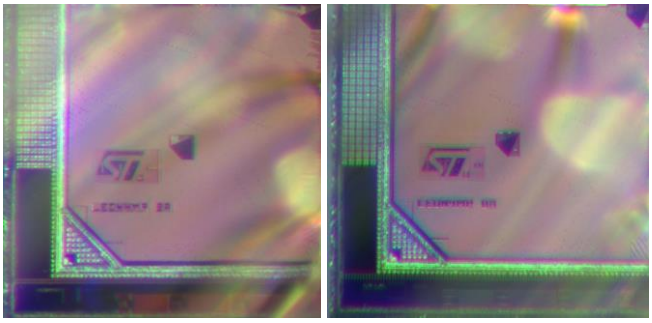

Figure 3. Die marking of the tested samples (device 001 on the left and device 002 on the right).

5.1.3 Irradiation facility

The Cyclotron of the Catholic University of Louvain-la-Neuve (UCL) can provide heavy ions covering a LET range between 1.3 and 62.5 MeV.cm²/mg (please refer to http://www.cyc.ucl.ac.be/HIF/HIF.php). The HIF facility also consists of a vacuum chamber equipped with motors to allow the placement and rotation of the DUT board (Figure 4). Testing at this facility is only possible under vacuum conditions. The facility also includes several radiation detectors used to control and monitor the beam parameters. The homogeneity of the beam is ± 10% on a 25 mm diameter. The maximum ion flux achievable at this facility is limited to approximately 30,000 ions/cm²/s. The characteristics of the ions used at this facility are shown in Table 4.

Table 4. Characteristics of the ions used at UCL/HIF (vacuum conditions).

Ion	DUT energy (MeV)	Range (µm Si)	LET @ surface (MeV.cm²/mg)
13 C 4+	131	269.3	1.30
22 Ne 7+	238	202.0	3.30
27 Al 8+	250	131.2	5.70
40 Ar 12+	379	120.5	10.0
53 Cr 16+	513	107.6	16.0
58 Ni 18+	582	100.5	20.4
84 Kr 25+	769	94.20	32.4
124 Xe 35+	995	73.10	62.5

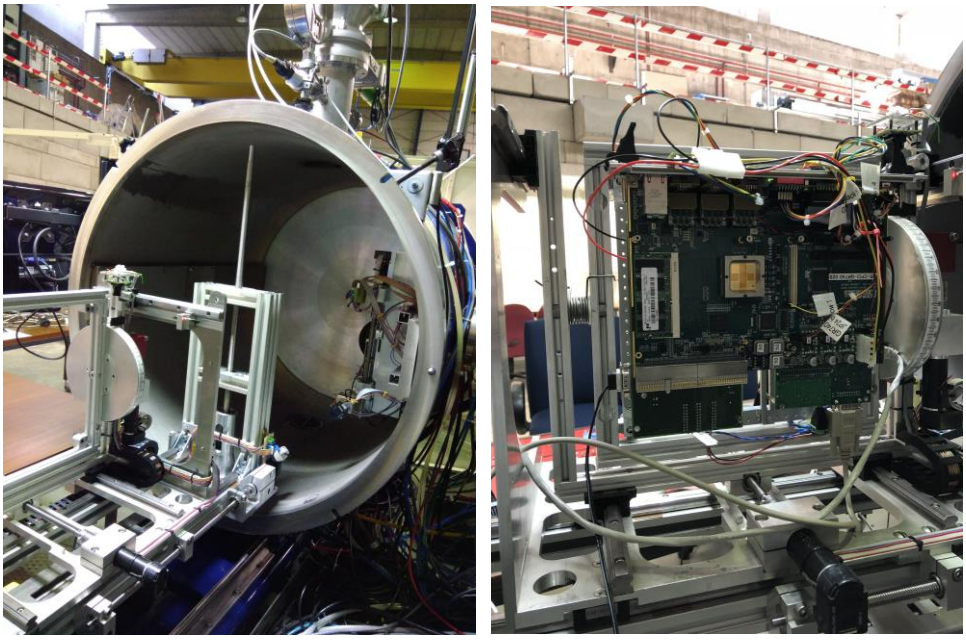

Figure 4. UCL/HIF facility.

5.1.4 Test setup description

The test setup consisted of 3 boards: a DUT board, an FPGA controller board, and a power control board. These boards were connected to two external computers placed outside the irradiation chamber/area via UART and Ethernet cables as shown in Figure 5.

The DUT board (GR-CPCI-GR740) used was a Cobham Gaisler's GR740 development board [RD8]. This board allows the functional validation of the processor. The specific board model used has a socket that allows exchanging easily the device under test. This board also includes, among other peripherals, external flash memory, SDRAM memory, power regulators, reset and clock circuits, as well as UART and Ethernet interfaces. The Ethernet interface was used to re-program the memories of the board between test runs without the need to open the test chamber. The SpaceWire ports included loopback connectors so that the signal could be routed out and in at each of the ports. Input clocks to the GR740 DUT board were provided during the tests through discrete crystal oscillators available on the board.

The FPGA controller board used was a standard Spartan-3-based board from Pender Electronics (GR-XC3S-1500) with a GRLIB-based [RD9] design embedded. The FPGA design allowed, through a GRMON2 [RD10] connection, to control the reset and boot signals, to monitor the PLL lock and watchdog signals, and to monitor the current and voltage supply (by interfacing the I^2C sensors on the DUT board) as well as the DUT temperature.

The power control board (GR-TC-PSC) was connected to an external power supply as shown in Figure 5 and provided the main voltage to the DUT and FPGA boards. The DUT board then regulated the input voltage to the different voltage levels required by the GR740: 1.2V for the core, 3.3V for the I/Os, and 2.5V for the LVDS ports. Each supply of the GR740 was monitored via the I^2C wired to the FPGA controller board. The power control board allowed to shut down the power when the supply current of GR740 showed a sudden increase above set limits (SEL protection mechanism). The SEL protection current limits were adjustable during the test from the external computer. Two SEL limits were implemented. The first one (soft limit) would place the device in reset but not power it down. This was done to verify if micro-latch-ups could take place on the GR740. The second limit (hard limit) was set to power down the device to avoid any potential damage. No latch-ups or micro-latch-ups were recorded during any irradiation test run.

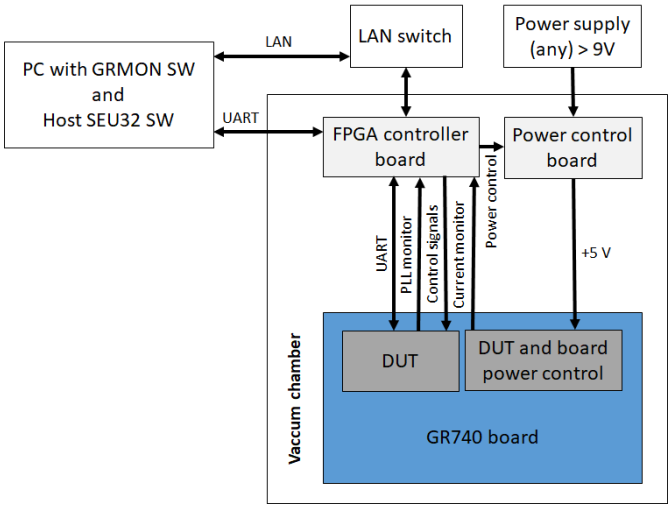

Figure 5. Block diagram of the test setup.

5.1.5 Test software

Two different software suites were used for the test campaign: SEU32 and GRMON2 [RD10]. These software suites are the same used to test silicon revision 0 in 2016, but with some updates and upgrades.

The Cobham Gaisler's SEU32 software was used from one of the external computers to test and monitor the status of the GR740 dynamically. The SEU32 test software has been designed for SEU testing of LEONFT processors. It consists of two parts: a target application running on a LEONFT processor, in this case, the GR740, and a host application running on the test computer. The target software can execute various types of applications (different memory tests, FPU-based test, multicore test, 8-port SpaceWire test, etc.) and report error events to the host computer. The host application can control which target application is being run and for how long. It can also collect error statistics during operation. Communication to the external computer was done using a UART interface during testing as shown in Figure 5.

The second software suite used was the Cobham Gaisler's GRMON2 software [RD10]. This was used to communicate from one of the external computers with the FPGA board via an Ethernet connection. A set of TCL scripts were developed to setup the GR740, reset the device before testing, and monitor and control the signals of DUT and power control boards.

5.2 Test conditions

Values of the supply current used during testing as well as latch-up current limits, input frequencies, and test temperature are given in Table 5.

Table 5. SEU/SET test conditions.

Core voltage and PLLs[2]	All test runs	1.2 V
I/O voltage	All test runs	3.3 V
LVDS I/O voltage	All test runs	2.5 V
Latch-up current limits	All test runs	Soft 1500 mA (Core), 500 mA (I/O and LVDS) Hard 1800 mA (Core), 800 mA (I/O and LVDS)
Temperature	All test runs	Room temperature
PLL input clocks[3]	All test runs	50 MHz for all PLLs (System clock = 250 MHz, Memory clock = 100 MHz, SpaceWire clock = 400 MHz)

[2] The PLLs are supplied together with the core supply.
[3] Default configuration as stated in the device's datasheet [RD1]:

- System clock PLL (SYSPLL): system clock output = 5 x (system clock input).
- Memory clock PLL (MEMPLL): memory clock output = 2 x (memory clock input).
- SpaceWire clock PLL (SPWPLL): SpaceWire clock output = 8 x (SpaceWire clock input).

5.3 Test results

This section gives a summary of the results of the heavy ion irradiation test campaign performed by Cobham Gaisler with the flight silicon (revision 1) version of the GR740 device.

5.3.1 Data analysis

The cross section (σ) results are calculated according to Equation (1). They were calculated taking into consideration the integrated fluence from all the runs with the same LET.

$$\sigma = \frac{\#\ events}{fluence} \tag{1}$$

A confidence level of 90%, as described in [AD1], was used to calculate the error bars of the cross section graphs (indicated with “min” and “max”). When no events were detected during a run or series of runs, the calculation of the upper limit cross section (“max”) assumed that one event had happened at the tested/integrated fluence.

5.3.2 SKYROB FFs

One of the main radiation hardening approaches to the GR740 is the use of RHBD SKYROB FFs. The IOMMU APV (access protection vector) data buffers is a small cache memory in the GR740's IOMMU block that was implemented using one SKYROB flip flop per bit. Because this memory can be read and written in a generic way through a diagnostic interface, and is not cleared on reset, this was convenient to use as a test structure for measuring the SKYROB static cross section.

Figure 6 together with Tables 6 and 7 show the obtained results.

Most events in the SKYROB FFs in the GR740 are masked by functional masking during normal device operation. Therefore, the SEU cross section data per bit presented herein cannot be used to estimate the overall error cross section of the GR740.

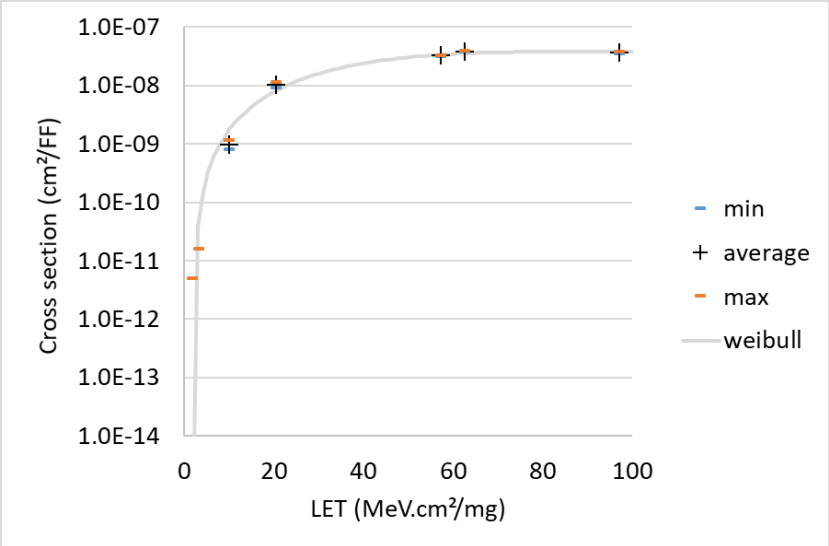

Figure 6. Cross section per bit results for SKYROB FFs in the GR740.

Table 6. Cross section per bit results for SKYROB FFs in the GR740.

LET (MeV.cm²/mg)	Cross section (cm²/FF)
1.87	< 1.67E-12
3.30	< 5.26E-12
10.07	9.61E-10
20.40	1.03E-08
57.30	3.29E-08
62.50	3.87E-08
97.20	3.71E-08

Table 7. Weibull parameters of Figure 6.

LET threshold (MeV.cm²/mg)	1.80
Cross section saturation (cm²/FF)	3.87E-08
W (MeV.cm²/mg)	38.63
S	1.98

5.3.3 CORELIB FFs

The register files of each processor core of the GR740 use SEU sensitive flip-flops (CORELIB FFs) together with block-level triplication and spacing (“Block TMR”). In order to verify the sensitivity of the CORELIB FFs, the data obtained from the register file has been analyzed. The Block TMR voting and correction on read is transparent to the hardware, however voter disagreement flags allow upsets to be counted by software.

Figure 7 together with Tables 8 and 9 show the obtained results. However, one must notice that the data presented here is underestimating the actual SEU cross section per bit of the CORELIB FFs due to two main masking factors:

- The polling rate of the voter disagreements flags may allow the saturation of the error counting.
- The dynamic behavior of the registers, since the device is not a test chip and it was tested from a user perspective, i.e., while running the different application test software. Therefore, registers may have been overwritten during the test runs and possible SEUs corrected.

The results obtained have presented a per-bit masking factor of one order of magnitude at the saturation cross section. Therefore, the actual SEU cross section per CORELIB FF is about 10 times higher than the data presented in Figure 7 and Table 8 and 9.

Results obtained from the static and dynamic tests performed show that all upsets observed were masked and corrected by the TMR scheme with no functional errors being observed in the GR740. Since all upsets in the CORELIB FFs in the GR740 are masked with Block TMR mitigation, the SEU cross section data per bit presented here cannot be used to estimate the overall error cross section of GR740.

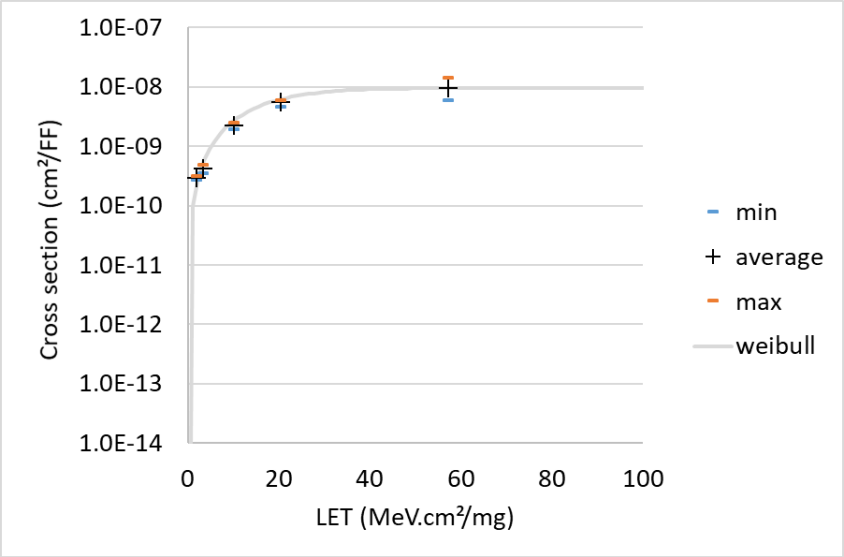

Figure 7. Measured cross section per bit results for the CORELIB FFs in the GR740.

Table 8. Cross section per bit results for the CORELIB FFs in the GR740.

LET (MeV.cm²/mg)	**Cross section (cm²/FF)**
1.87	2.90E-10
3.30	4.23E-10
10.07	2.21E-09
20.40	5.56E-09
57.30	9.54E-09

Table 9. Weibull parameters of Figure 7.

LET threshold (MeV.cm²/mg)	0.01
Cross section saturation (cm²/FF)	9.55E-09
W (MeV.cm²/mg)	19.89
S	1.63

5.3.4 SRAM memories

The L1 cache of the processor cores of the GR740 is composed of SEU sensitive SRAM cells that include an 8+1 parity error detection system with invalidation on error scheme. The L2 cache memory is also composed of SEU sensitive SRAM cells while the L2 cache logic is composed of RHBD SKYROB FFs. The L2 cache includes a 32+7 BCH SECDED scheme. Scrambling of all SRAM cells, one bit every 4 from the same word, is used to minimise the possibility of MBU events within one word. In order to verify the sensitivity of the SRAM cells, the data obtained from the L1 and L2 cache memories has been analyzed. Single errors in the L1 and L2 caches can be counted by individual counters in the GR740. All detected errors are corrected by the GR740.

Figure 8 together with Tables 10 and 11 show the obtained results.

The SEU cross section data per bit presented here cannot be used to estimate the overall error cross section of GR740.

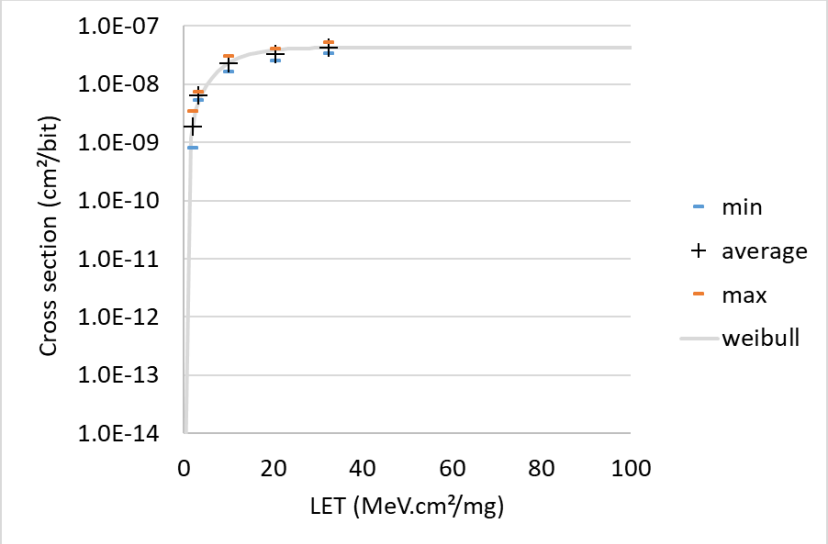

Figure 8. Cross section per bit results for the SRAM cells of the GR740.

Table 10. Cross section per bit results for the SRAM cells of the GR740.

LET (MeV.cm²/mg)	Cross section (cm²/bit)
1.87	1.84E-09
3.30	6.32E-09
10.07	2.29E-08
20.40	3.29E-08
32.40	4.24E-08

Table 11. Weibull parameters of Figure 8.

LET threshold (MeV.cm²/mg)	0.3
Cross section saturation (cm²/bit)	4.24E-08
W (MeV.cm²/mg)	11.32
S	1.57

5.3.5 PLL

The GR740 has three RHBD PLLs, the system (SYSPLL), the memory (MEMPLL), and the SpaceWire (SPWPLL). In order to verify the sensitivity of the PLLs, the data obtained from them has been analyzed. The results are based on the PLL loss of lock events recorded. All events were self-recovered by the PLLs. The same PLLs were also tested in the GR740 prototype silicon (revision 0) with protons with no events recorded (see Section 4.1.2.2).

Figure 9 together with Tables 12 and 13 show the obtained results. All PLL loss of lock events can be detected at system level by monitoring the PLL lock output signals of the GR740.

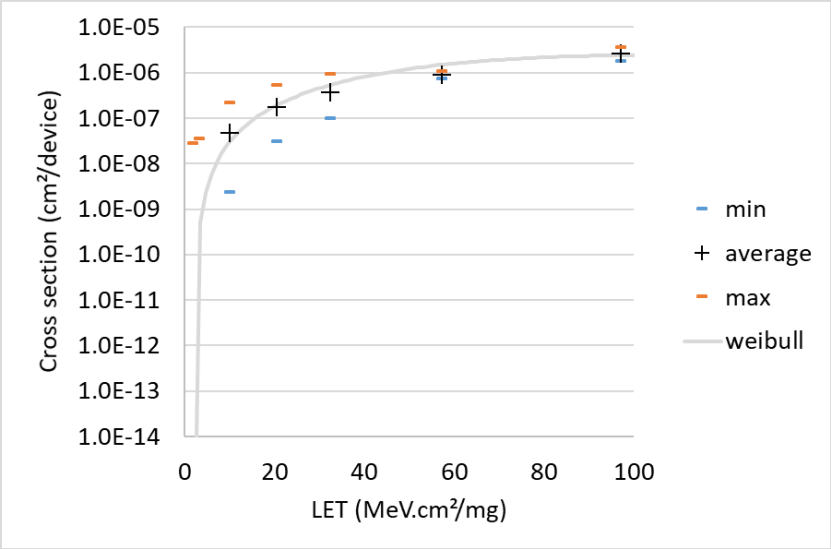

Figure 9. Cross section results of the GR740 for PLL loss of lock events.

Table 12. Cross section results of the GR740 for PLL loss of lock events.

LET (MeV.cm²/mg)	Cross section (cm²/device)
1.87	< 9.35E-09
3.30	< 1.22E-08
10.07	4.75E-08
20.40	1.75E-07
32.40	3.69E-07
57.30	8.98E-07
97.20	2.59E-06

Table 13. Weibull parameters of Figure 9.

LET threshold (MeV.cm²/mg)	2.38
Cross section saturation (cm²/device)	2.56E-06
W (MeV.cm²/mg)	58.22
S	2.18

5.3.6 Functional tests

Figure 10 and Tables 14 and 15 show the average error cross section results obtained from the functional tests performed, which consisted on the execution of different types of applications, such as L1 cache memory(ies) test in single- and multi-core modes, L2 cache memory test, and FPU-based test. In addition to a specific L2 cache memory test, the L2 cache was also enabled in all other test cases, which reinforces the correct operation of the L2 cache in the flight silicon and the effectiveness of the error mitigation schemes adopted in it. The results include Silent Data Corruption (SDC) and System events. SDC events refer to executions performed correctly but with wrong data output. System events refer to handling traps, program failures (hangs or error bursts), bus related errors (those with functional effects), communication errors (dirty data output, error bursts, timeouts), processor cores stopping to report errors, and PLL loss of lock events (also reported individually in the previous section). All errors are recoverable by resetting the device.

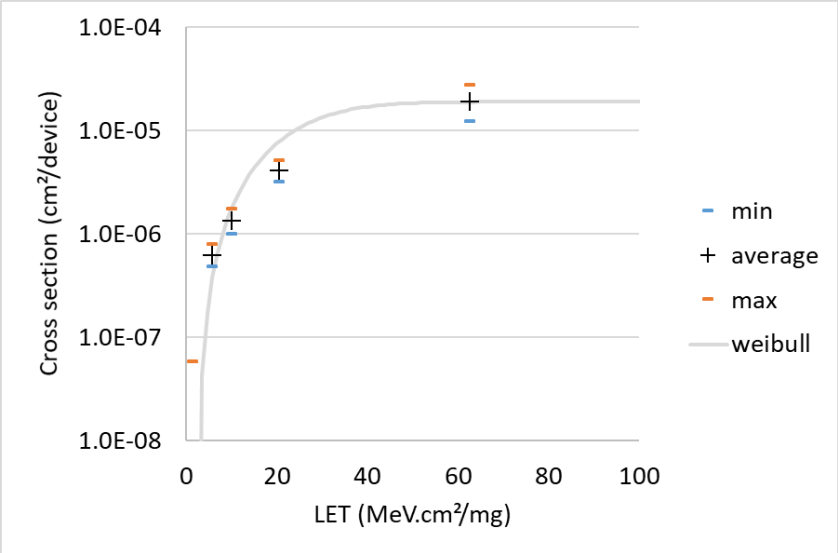

Figure 10. Cross section results of the GR740 for functional errors.

Table 14. Cross section results of the GR740 for functional errors.

LET (MeV.cm²/mg)	Cross section (cm²/device)
1.30	< 1.96E-08
5.70	6.24E-07
10.00	1.35E-06
20.40	4.13E-06
62.50	1.90E-05

Table 15. Weibull parameters of Figure 10.

LET threshold (MeV.cm²/mg)	2.20
Cross section saturation (cm²/device)	1.90E-05
W (MeV.cm²/mg)	25.00
S	2.00

6 HEAVY ION SEE ERROR RATES

The SEE error rates due to heavy ions for the GR740 flight silicon (revision 1) were estimated for the following orbits (solar minimum, Z=1-92, Al shielding of 1 g/cm²):

- GEO (36,000 km, AP8 min);
- LEO (700 km, 98.7 inclination, AP8 min).

The estimations consider the Weibull data presented in Figure 10 and Table 15. The SEE rates were calculated using TRAD's OMERE software [RD11]. The sensitive depth used for the calculations was 1.4 µm, with an approximate RPP[4] area of 2 µm x 2 µm. The results are given in Table 16. The mean time between events refers to two functional errors. All errors are recoverable by resetting the device.

Table 16. Heavy ion SEE error rates due to heavy ions for the GR740 flight silicon (revision 1) under different environments.

Environment	Events/device/day	Mean time between events (years)
GEO	7.81E-6	350
LEO	2.09E-6	1310

The SEE error rates due to protons adds up to the error rates presented above. However, due to the very low cross section for proton events of the GR740, the contribution of proton events is less significant in majority of all space orbits.

[4] The calculations consider 480 RPP elements. The number of RPP cells have been estimated by dividing the saturation cross section with the area of the RPP cells.

7 SINGLE EVENT LATCH-UP CHARACTERIZATION – GR740 FLIGHT SILICON

This chapter is a summary of the heavy ion-induced SEL test campaign performed by Cobham Gaisler at the UCL/HIF facility, in Louvain-la-Neuve, Belgium, on week 17, 2019, with the flight silicon (revision 1) version of the GR740 device.

7.1 Test setup and procedure

This section reports on the test setup and procedure for the results reported in this chapter.

7.1.1 Organization of the activities

The tested devices were provided by STMicroelectronics already delidded. The test setup and software were developed by Cobham Gaisler, and they are based on successful past irradiation tests. The entire setup was checked before the campaign at Cobham Gaisler premises through error injection campaigns.

7.1.2 Tested samples

Table 16. Tested samples.

Device identification	GR740, silicon revision 1
Packaging	LGA625 (Ceramic Land Grid Array)
Wafer processing date	2018
Diffusion lot number	Q801934
Serial numbers[5]	001, 002, 003, 006

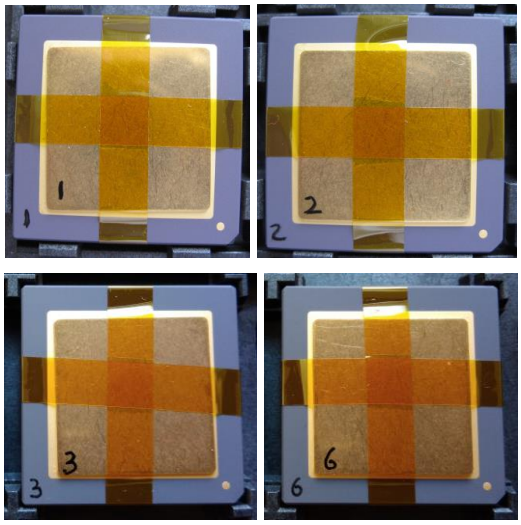

Figure 11. View of the tested samples (on the upper part, devices 001 on the left and device 002 on the right; on the bottom part, devices 003 on the left and device 006 on the right) with the protection lid.

[5] Devices 001 and 002 have been tested for SEEs before.

7.1.3 Irradiation facility

The SEL test campaign reported in this chapter was performed at the UCL/HIF facility, in Louvain-la-Neuve, Belgium. The characteristics of the facility are presented in Section 5.1.3 of this document.

Only Xenon ion beam was used in the SEL test campaign. The DUTs were irradiated at normal incident angle (0º, LET = 62.5 MeV.cm²/mg) as well as tilted (60º, LET = 125 MeV.cm²/mg). The Xenon beam provided sufficient range to reach the active silicon of the GR740. The distance from top surface down to diffusion silicon is < 10 µm, while the estimated penetration of the 60º tilted Xenon ion beam is of about 36.5 µm.

7.1.4 Test setup description and software

The SEL test setup system developed is similar to the one successfully used in the past heavy ion-induced SEE test campaigns and described in Section 5.1.4. Figure 12 illustrates the additions to the test setup for the SEL test campaign, which consisted mainly of a heating setup.

Concerning the maximum operating voltages, the supply voltages of the DUT were adjusted through multi turn potentiometers available on the DUT board. The monitoring of the GR740 supplies was performed via I2C-based current/power monitors available on the DUT board and wired to the FPGA monitor board. The power control board ("PSC monitor") allowed to shut down the power in case the supply current of GR740 showed a sudden increase above set limits (SEL protection mechanism), as mentioned in Section 5.1.4. The elevated operating temperature was achieved using heating elements placed on the socket of the DUT with an adhesive transfer tape and regulated by a DC temperature controller. The heating setup implemented allowed to achieve elevated temperatures of 85 ºC and above. However, the maximum operating temperature of 125 ºC could not be reached.

The current consumption monitoring was performed through a TCL script running in the GRMON2 (Section 5.1.5). The junction temperature monitoring of the DUT die was performed through the target application of the SEU32 software (Section 5.1.5), which was sampling at each second the on-chip temperature sensor and sending the read-out values (minimum, maximum, and average) to the host computer for logging. The DUT was operational during the SEL testing but with no application test software running in order to keep the current consumption constant. The only tasks performed by the target application of the SEU32 software were the setup of the GR740 (enabling of processor resources), the temperature monitoring, and error detection.

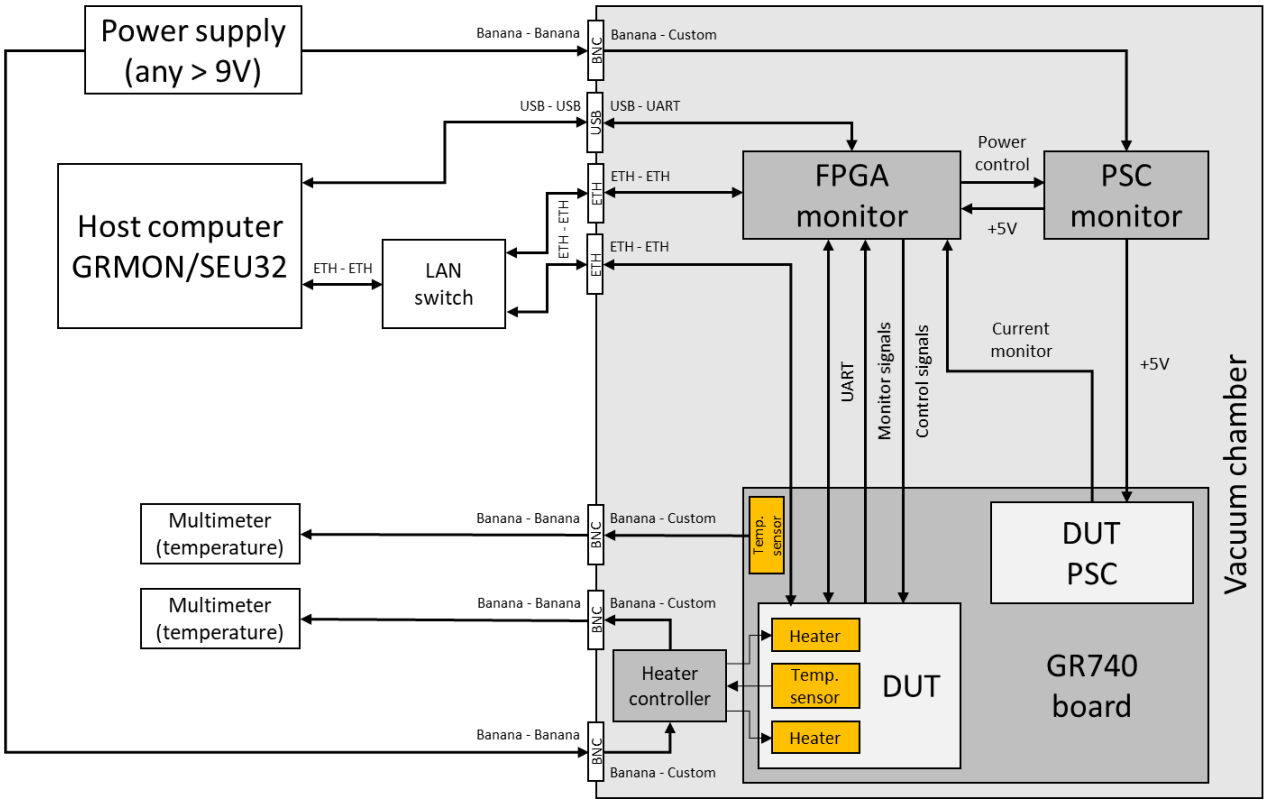

Figure 12. Block diagram of the SEL test setup.

7.2 Test conditions

The values of the input voltages used during the test campaign as well as current limits, input frequencies, and test temperature are given in Table 17.

Table 17. SEL test conditions.

Core voltage and PLLs[6]	All test runs	1.32 V
I/O voltage	All test runs	3.63 V
LVDS I/O voltage	All test runs	2.75 V
Latch-up current limits (Section 5.1.4)	All test runs	Soft 1500 mA (Core), 500 mA (I/O and LVDS) Hard 1800 mA (Core), 800 mA (I/O and LVDS)
Junction Temperature	All test runs	85 ºC < T_j < 125 ºC
PLL input clocks[7]	All test runs	50 MHz for all PLLs (System clock = 250 MHz, Memory clock = 100 MHz, SpaceWire clock = 400 MHz)

[6] The PLLs are supplied together with the core supply.
[7] Default configuration as stated in the device's datasheet [RD1]:

- System clock PLL (SYSPLL): system clock output = 5 x (system clock input).
- Memory clock PLL (MEMPLL): memory clock output = 2 x (memory clock input).
- SpaceWire clock PLL (SPWPLL): SpaceWire clock output = 8 x (SpaceWire clock input).

7.3 Test results

Table 18 presents the results of the heavy ion SEL test campaign performed by Cobham Gaisler with the flight silicon (revision 1) version of the GR740 device. Two DUTs were tested at LET of 62.5 MeV.cm²/mg with no tilting, and four DUTs were tested at LET on 125 MeV.cm²/mg with 60º tilting. No SEL events were recorded in any of the test runs with neither the soft nor the hard latch-up current limit (Section 5.1.4 and Table 17) being triggered.

Table 18. SEL test results.

Run	DUT	Effective LET (MeV.cm²/mg)	Fluence (ions/cm²)	DUT junction temperature (ºC)			SEL events
				Minimum	Average	Maximum	
1	002	62.50	1E+7	95.00	96.50	98.00	0
4	003	62.50	1E+7	104.00	106.00	108.00	0
2	002	125.00	1E+7	85.00	89.00	93.00	0
3	003	125.00	1E+7	88.00	96.00	104.00	0
5	006	125.00	1E+7	99.00	106.00	113.00	0
6	001	125.00	1E+7	90.00	97.00	104.00	0

8 TOTAL IONIZING DOSE RADIATION VERIFICATION TEST – GR740 FLIGHT SILICON

This chapter is a summary of the TID radiation verification test campaign performed by Cobham Gaisler with the flight silicon (revision 1) version of the GR740 device. A full TID radiation verification test report is available at Cobham Gaisler, providing all details of the tests that are summarised herein.

The TID radiation verification test of the GR740 device up to 300 krad(Si) was performed as per MIL-STD-883K standard, test method 1019.9. Ten (10) samples from wafer diffusion lot 41923001, run Q801934, wafer 2 were irradiated. Five (5) samples were biased in “Normal bias” mode and five (5) samples were biased in “Cold spare” mode.

In-flux and remote intermediate electrical measurements were performed as per MIL-STD-883K standard, test method 1019.9, in accordance with the accelerated annealing test procedure.

The dose rate used in the test was 0.21 rad(Si)/s, as per Condition B of test method 1019.9. Table 19 provides the traceability of the devices tested.

Table 19. Tested samples.

Device identification	GR740, silicon revision 1
Device marking	GR740-EVAL1
Package	LGA625 (Ceramic Land Grid Array)
Technology	65nm CMOS
Die lot identification	Identification 3390200101, diffusion 41923001, run Q801934, wafer 2
Date code (DC)	1913A
Quantity tested	5 “Normal bias” mode, 5 “Cold spare” mode, 2 reference samples
Serial numbers[8]	“Normal bias” mode: • DUT SN1: 1 (GR740-EVAL1, DC1913A) • DUT SN2: 2 (GR740-EVAL1, DC1913A) • DUT SN3: 3 (GR740-EVAL1, DC1913A) • DUT SN4: 4 (GR740-EVAL1, DC1913A) • DUT SN5: 5 (GR740-EVAL1, DC1913A) “Cold spare” mode: • DUT SN6: 6 (GR740-EVAL1, DC1913A) • DUT SN7: 7 (GR740-EVAL1, DC1913A) • DUT SN8: 8 (GR740-EVAL1, DC1913A) • DUT SN9: 9 (GR740-EVAL1, DC1913A) • DUT SN10: 10 (GR740-EVAL1, DC1913A) Reference sample: • DUT SN11-REF: 11 (GR740-EVAL1, DC1913A) Spare sample: • DUT SN12-SPARE: 12 (GR740-EVAL1, DC1913A)

“Cold spare” is a biasing configuration where the core of the device is unbiased and the I/Os that

[8] All samples successfully completed dynamic burn-in (240 hours at 125°C), static burn-in (144 hours at 125°C) and final electrical (25°C) before the start of the irradiation.

support “cold spare” mode are statically biased at maximum voltage. No TID degradation was recorded.

“Normal bias” is a biasing configuration where all supplies are set to the maximum voltages. All input signals are held static. A low frequency (1 MHz) signal to the system clock and the reset input, which is kept asserted, maintains all the sequential logic and outputs in a static state. No parametric drifts outside specification limits were recorded.

Only in “Normal bias” biasing configuration, a parametric drift was recorded on the standby core supply current, which was observed both with in-flux tests and with remote electrical measurements. As one can see in Figure 13, all measurements were within the specified limits after irradiation to the target total ionizing dose level of 300 krad(Si), after room temperature annealing, and accelerated annealing. The drift recorded in the standby supply current has no impact during the normal operation of the device, in which the dynamic supply current is one order of magnitude higher or more in many cases.

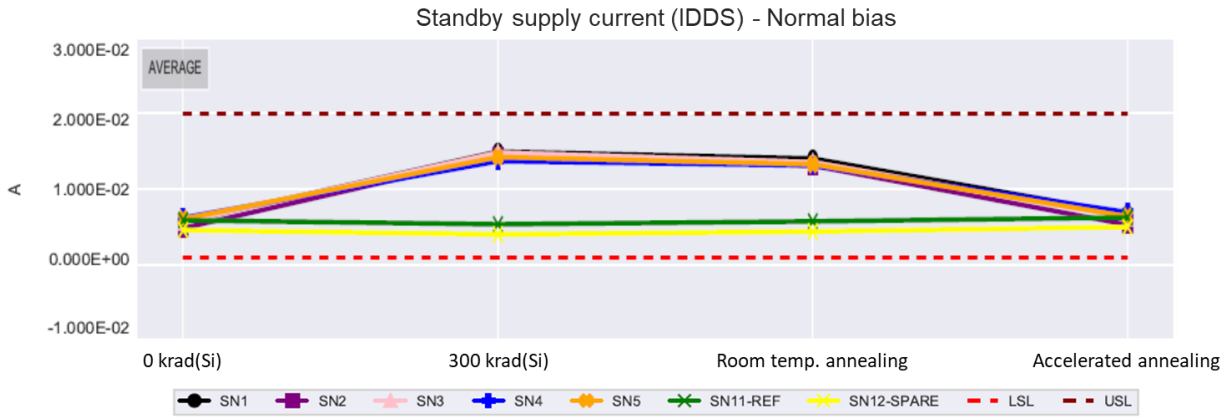

Figure 13. Parametric drift within the specified limits observed on the standby core supply current during TID testing.

No evidence of time-dependent effects were observed after the accelerated annealing test step.

All tested samples passed the total ionizing dose test to the specified level of 300 krad(Si).

9 CONCLUSIONS

The Total Ionizing Dose (TID) radiation verification tests of GR740 device to the targeted dose of 300 krad(Si) have been completed successfully. Both normal and cold spare operation modes of the GR740 have been verified in the TID testing.

The Single Event Latch-up (SEL) testing of the GR740 device has confirmed the SEL immunity of the device up to an LET of 125 MeV.cm²/mg (tested with elevated temperature - > 85 ºC - and maximum supply voltages).

The GR740 device has also been tested for Single event effects (SEE) in both static and dynamic modes. In dynamic mode, the tests consisted of several application level tests, ranging from memory tests to a multicore test. The main SEE results obtained were as follow:

- Heavy ions:
  - Error cross section Weibull parameters of the average results obtained from all application level tests performed with heavy ions (sensitive depth = 1.4 µm, approximate RPP cell area = 2 µm x 2 µm, 480 RPP elements):
    - LET_{th}: 2.20 MeV.cm²/mg;
    - σ_{sat}: 1.90E-5 cm²/device;
    - W: 25.00;
    - S: 2.00.
  - Estimated error rates per day due to heavy ions[9] with above Weibull parameters considering a solar minimum, Z=1-92, and Al shielding of 1 g/cm²:
    - GEO (36,000 km, AP8 min.):
      - 7.81E-6 events/device/day.
    - LEO (700 km, 98.7º inclination, AP8 min.):
      - 2.09E-6 events/device/day.
- Protons:
  - The average cross section for functional errors over the entire tested proton energy range (10-62 MeV) was of about 1.61E-12 cm²/device. Based on the obtained results from the proton test campaign reported in Section 4.1.2.2 and the recorded LET threshold with heavy ions (2.20 MeV.cm²/mg), it can be concluded that the GR740 is immune to functional errors from direct proton ionization-induced effects.

The low functional error rate recorded in the application level tests under irradiation demonstrates that although an extensive amount of SEUs in the internal memory cells of the GR740 have been recorded, all events were successfully mitigated and corrected. There is no evidence of error build-up in the GR740.

The excellence and importance of the GR740 fault tolerance concept can be better expressed with numbers by comparing the errors rate in, e.g., the GEO orbit environment for functional errors versus the overall rate of upsets in the internal memory cells in the GR740. These numbers can be estimated with the Weibull data for bit upsets presented in this document for the CORELIB FFs,

[9] The SEE error rates due to protons adds up to the error rates presented above. However, in majority of space orbits, the contribution of proton events is less significant.

SKYROB FFs, and SRAM cells (Sections 5.3.2-5.3.4) and multiplied with the number bits used of each type (Section 3.1). Therefore, the total number of upsets in a GEO orbit environment will be 9 upsets/device/day while the functional error rate will be 7.81E-6 events/device/day. As consequence, the fault tolerance concept of the GR740 has improved the reliability in a GEO orbit environment by 6 orders of magnitudes.

One must notice that a flawless operation of the GR740 in a radiation environment is pending on the software being implemented correctly by enabling all mitigation features of the device, such as a proper interrupt handling and the continuous usage of scrubbing in all the L1 and L2 caches to prevent error build-up. All the guidelines for the correct operation of the device are documented in the GR740 User's Manual [RD1].

Additional information about the radiation performance of GR740 can be inquired through support@gaisler.com.