SINGLE EVENT EFFECTS
TEST REPORT

Test Type:	Heavy ion
Test facility:	RADEF, JYFL, University of Jyvaskyla, Jyvaskyla, Finland
Test Date:	February 2015
Part Type:	ADC128S102
Part Description:	8-Channel, 500 ksps to 1 Msps, 12-Bit A/D Converter
Part Manufacturer:	Texas Instruments

Alter Technology PO n° 5506888/ 05.02.2015

Hirex reference :	HRX/SEE/532	Issue : 02	Date :	April 29 2015
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DOCUMENTATION CHANGE NOTICE

Issue	Date	Page	Change Item	
01	29/04/2015	All	Original issue	
02	22/05/2015		Corrections as per Alter comments	

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SEE TEST REPORT

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1 Glossary

Most of the definitions here below are from JEDEC standard JESD89A

DUT: Device under test.

Fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.
In this document, Fluence is expressed in ions per cm2.

Flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.
In this document, Flux is expressed in ions per cm2*s.

Single-Event Effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.
Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL.

Single-Event Transient (SET): A soft error caused by the transient signal induced by a single energetic particle strike.

Single-Event Latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.
SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.
An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.
Single-Event Latch-up (SEL) cross-section: the number of events per unit fluence. For chip SEL cross-section, the dimensions are cm2 per chip.

Error cross-section: the number of errors per unit fluence. For device error cross-section, the dimensions are cm2 per device. For bit error cross-section, the dimensions are cm2 per bit.

Tilt angle: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis
Weibull fit: $F(x) = A\,(1-\exp\{-[(x-x_0)/W]^s\})$ with:

> x = effective LET in MeV/(mg/cm^2);
> F(x) = SEE cross-section in cm^2;
> A = limiting or plateau cross-section;
> x_0 = onset parameter, such that F(x) = 0 for $x < x_0$;
> W = width parameter;
> s = a dimensionless exponent.

Error bars: error bars are computed using a confidence level of 95% and a beam flux uncertainty of +/-10% as recommended by Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100.

2 Introduction

This report presents the results of Heavy Ions test program carried out on ADC128S102 part type from Texas Instruments. ADC128S102 samples were used for heavy ions testing at RADEF, JYFL, University of Jyvaskyla, Jyvaskyla, Finland.
This work was performed for Alter Technology under PO n° 5506888/ 15.02.2015.

3 Applicable and Reference Documents

3.1 Applicable Documents

AD-1. SEU TEST TEST PLAN No. ATN-RP-187
AD-2. ADC128S102 Texas Instruments datasheet, SNAS298F –AUGUST 2005–REVISED MAY 2013

3.2 Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

4 DEVICE INFORMATION

4.1 Device description

ADC128S102 provides 8-Channel, 500 ksps to 1 Msps, 12-Bit A/D Converter.

Part type:	ADC128S102
Manufacturer:	Texas Instruments
Manufacturer part number:	ADC128S102CIMT/NOPB
Datecode:	1414
Package:	TSSOP-16
Top marking:	logo 44CC40U 128S02 CIMT
Bottom marking:	-
Die dimensions:	891µ x 1649µ

4.2 Sample identification

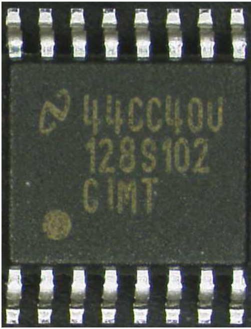


Photo 1 – Device top view

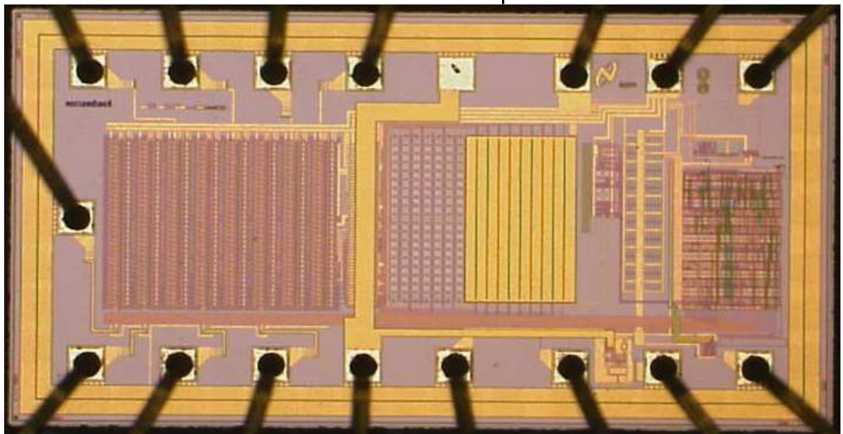


Photo 3 – Die full view

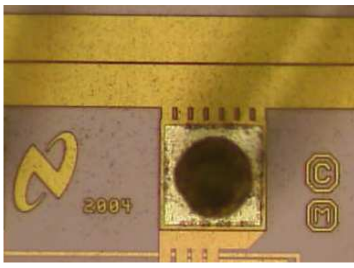


Photo 4 - Die Marking1 Photo 5 - Die Marking2

Figure 1: ADC128S102 device identification

5 RADEF Facility

Test at the cyclotron accelerator was performed at University of Jyvaskyla (JYFL) (Finland) under HIREX Engineering responsibility.
The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.
The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula,

$$130\ Q^2/M,$$

where Q is the ion charge state and M is the mass in Atomic Mass Units.

Test chamber

Irradiation of components is performed in a vacuum chamber with an inside diameter of 75 cm and a height of 81 cm.
The vacuum in the chamber is achieved after 15 minutes of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the X, Y and Z directions. The possibility of rotation around the Y-axis is provided by a round table. The free movement area reserved for the components is 25 cm x 25 cm, which allows one to perform several consecutive irradiations for several different components without breaking the vacuum.
The assembly is equipped with a standard mounting fixture. The adapters required to accommodate the special board configurations and the vacuum feed-throughs can also be made in the laboratory's workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components.
A CCD camera with a magnifying telescope is located at the other end of the beam line to determine accurate positioning of the components. The coordinates are stored in the computer's memory allowing fast positioning of various targets during the test.

Beam quality control

For measuring beam uniformity at low intensity, a CsI(TI) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis.
A set of four collimated PIN-CsI(TI) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.
Two beam wobblers and/or a 0.5 microns diffusion Gold foil can be used to achieve good beam homogeneity. The foil is placed 3 m in front of the chamber. The wobbler-coils vibrate the beam horizontally and vertically, the proper sweeping area being attained with the adjustable coil-currents.

Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI(TI) detectors. Three collimators of different size and shape are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.
At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(TI) detectors.

Ion	LET^{SRIM} at surface [$MeV.cm^2.mg^{-1}$]	$Range^{SRIM}$ [µm]	Beam energy [MeV]
$^{20}Ne^{+6}$	3.63	146	186
$^{40}Ar^{+12}$	10.2	118	372
$^{56}Fe^{15+}$	18.5	97	523
$^{82}Kr^{22+}$	32.1	94	768
$^{131}Xe^{35+}$	60.0	89	1217

SRIM-2003.26

Table 1 – Ion beam setting

6 Test Set-up

Test system Figure 2 shows the principle of the Heavy Ion test system.

The test system is based on a Virtex4 FPGA (Xilinx). It runs at 50 MHz. The test board has 168 I/Os which can be configured using several I/O standards.

The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 24 independent channels.
Offsets of few milliamps can be observed in the absolute value recorded for a given channel due to our current digital conversion hardware. However, this offset being constant, current variations are representative of the actual current ones

- A SEL event is detected when corresponding UI current exceeds a given threshold current within a few microseconds; it is then followed by a device under test power reset after a given off time.
- SET events are detected by using hirex 4 channels custom digitizer (200MSPS SDR). SET event is detected when the DUT output is above or below the expected value plus or minus a given threshold.
-

The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.
Test board has been designed so that 3 samples can be tested at the same time to heavy ions.
3 ADC128S102 parts are mounted on the daughter board as shown in Figure 3.

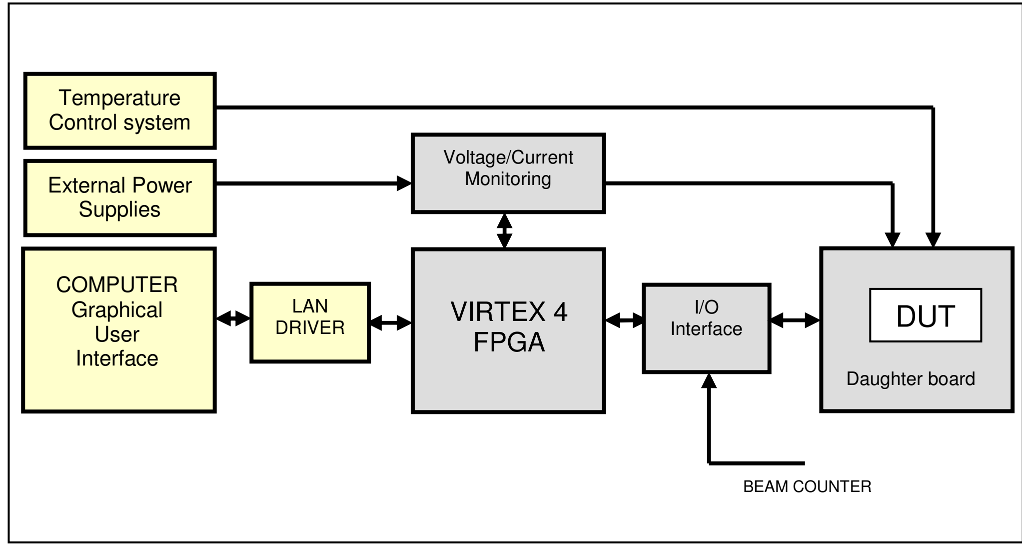


Figure 2: ADC128S102, Heavy ion test set-up

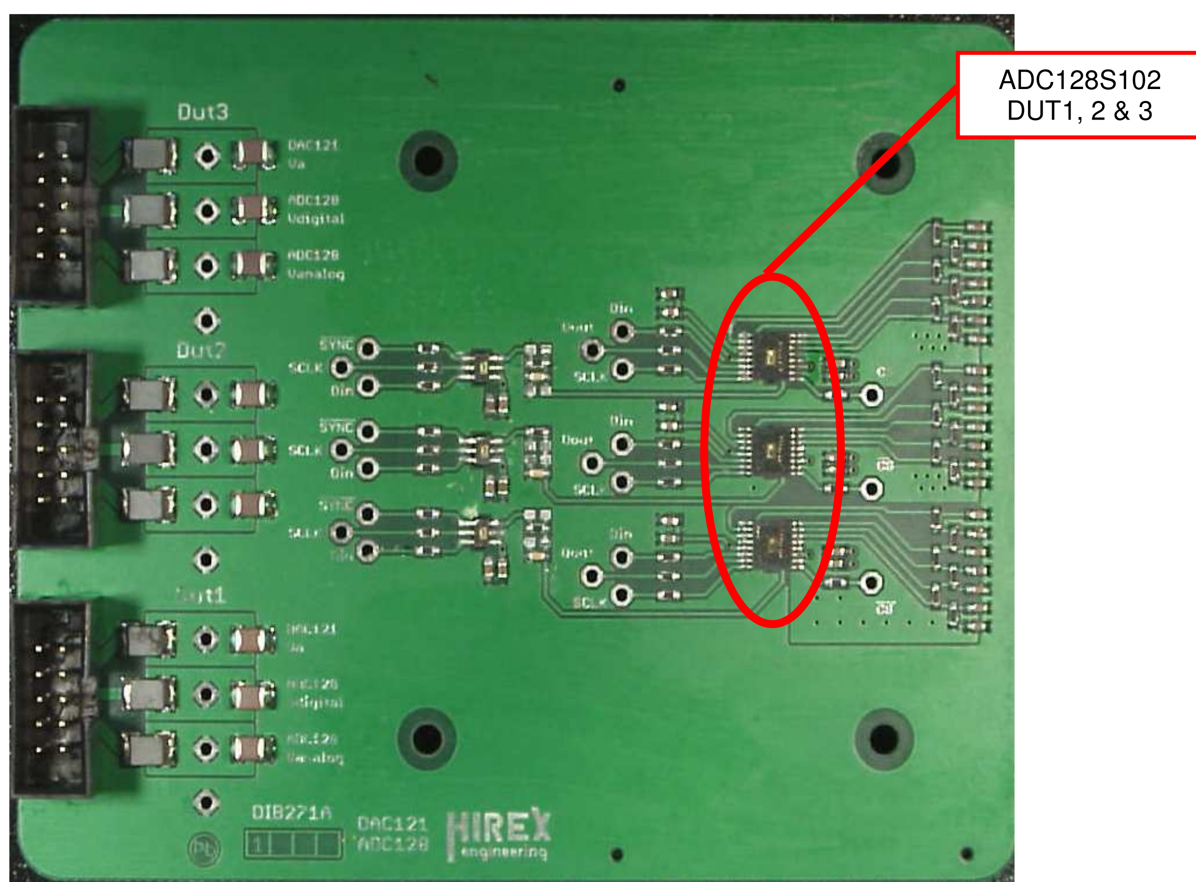


Figure 3: Daughter board (DIB271A) photo

7 Bias conditions

3 chains are built, each one constitued by 1 DAC121S101 linked to 1 ADC128S102ADC.
For SEL test mode ADC128S102 bias is 3.6V for VA and VD while during SET test mode bias is 2.97V for both VA and VD.
Samples can be heated thanks to an heating resistor mounted on the back of the test board.

ADC128S102 clock is set to 16MHz, conversion frequency to 711KSPS

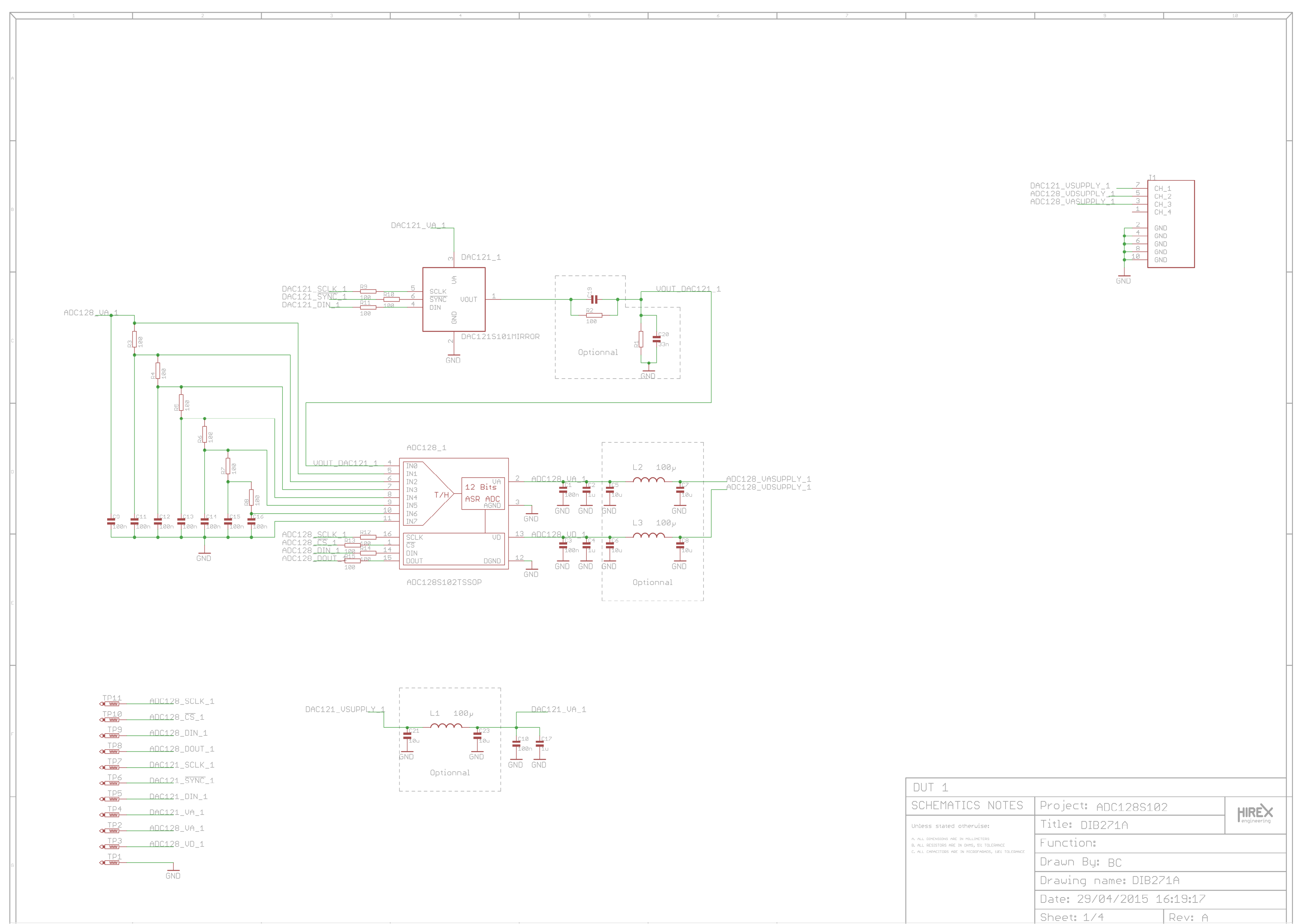


Figure 4 – Test board schematics

8 SEE Test Results

Samples were tested using test conditions of paragraph7.
Run details and results are provided in Table 2 for SEL test runs and in Table 3 for SET test runs.
In accordance with RD-1, error bars have been computed using a confidence level of 95% and a beam flux uncertainty of +/-10%.

SEL test runs

SEL cross-section for each sample is shown in Figure 5.
For SEL test condition (VA=VD=3.6V), DUT case temperature was set to 50°C and SEL detection threshold for each DUT was 80mA for VA and 50mA for VD.
SEL have been observed on VA only and measured SEL currents are about 180mA. In addition step current increase have been recorded but significantly below 80mA.
No SEL was observed with Krypton (tilt=45 and Effective LET=45).
When tested in the SEL test mode but at room temperature, few SEL has been observed on VA as well as some step currents with Xenon (LET=60).

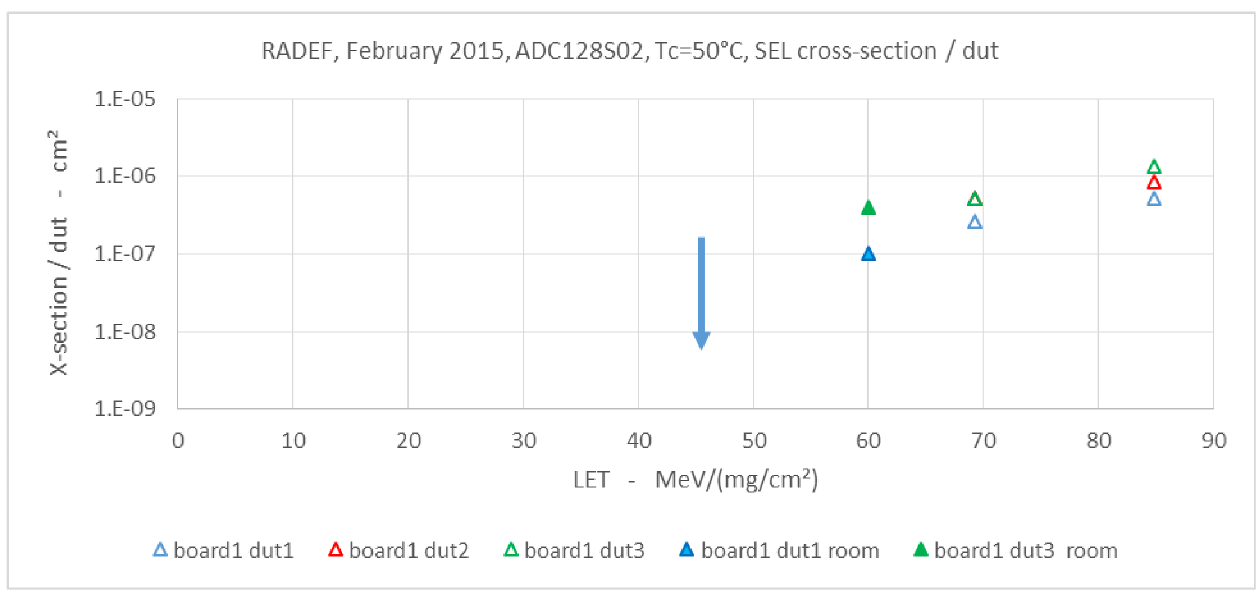


Figure 5 – Radef, February 2015, ADC128S102,SEL cross-section / device as a function of LET

SET test runs

DAC inputs codes are created such that DAC output to DUT input is a sine wave of 2.96KHz.
ADC sample conversion is 240 times the output sine wave frequency.
SET cross-section for each sample is shown in Figure 6.
with krypton (LET=32) and higher LETs, when a step current occurred, sample might enter a SEFI mode error (permanent errors) or not and the step current as well as the SEFI mode were cured by a manual power reset.
In Figure 6, SET cross-section is computed by discarding the time periods and the associated events when SEFIs are detected.
All events are one conversion error but one event only during run022 (see Figure 10).
Figure 7, Figure 8, Figure 9 show examples of SET events, a small event, a large one and a very large one. Figure 10 shows theonly event recorded with multiple successive conversion errors.Figure 11 shows an event lasting permanently at the start of the SEFI. The SEFI states is cleared by a manual power reset.
In these plots, one can see the ADC output, the ADC output 240 periods before and the delta between these two curves. It is the way used to detect and trigger the event record when delta point is above the given threshold. Threshold used for the different runs is 60 LSBs.

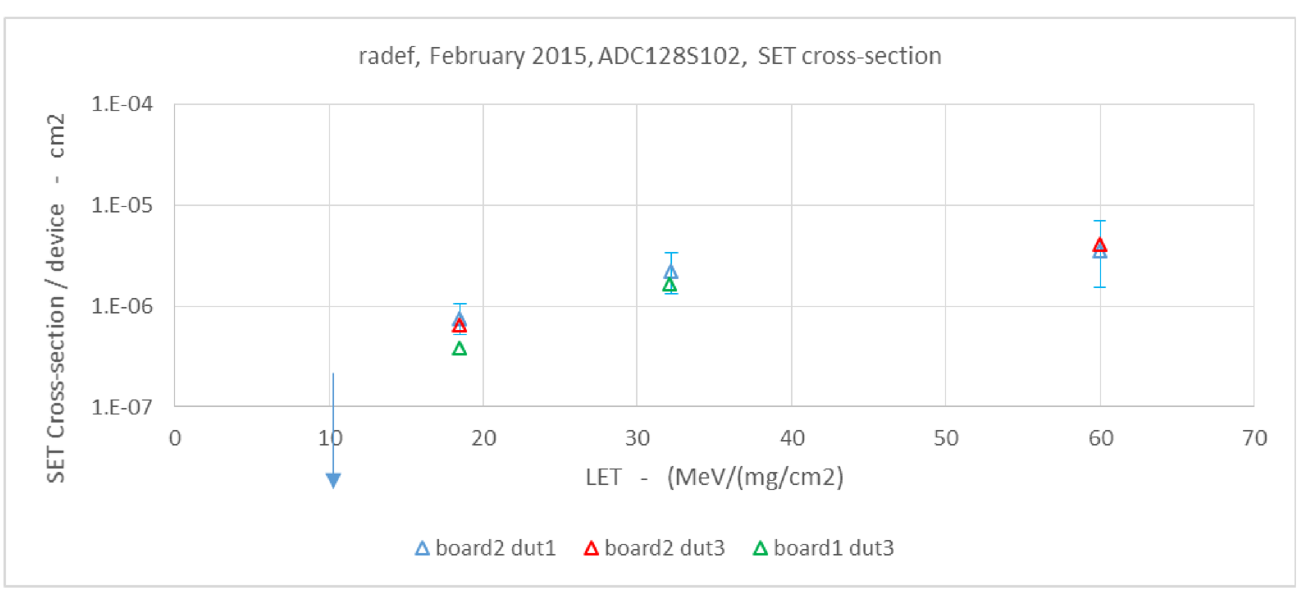


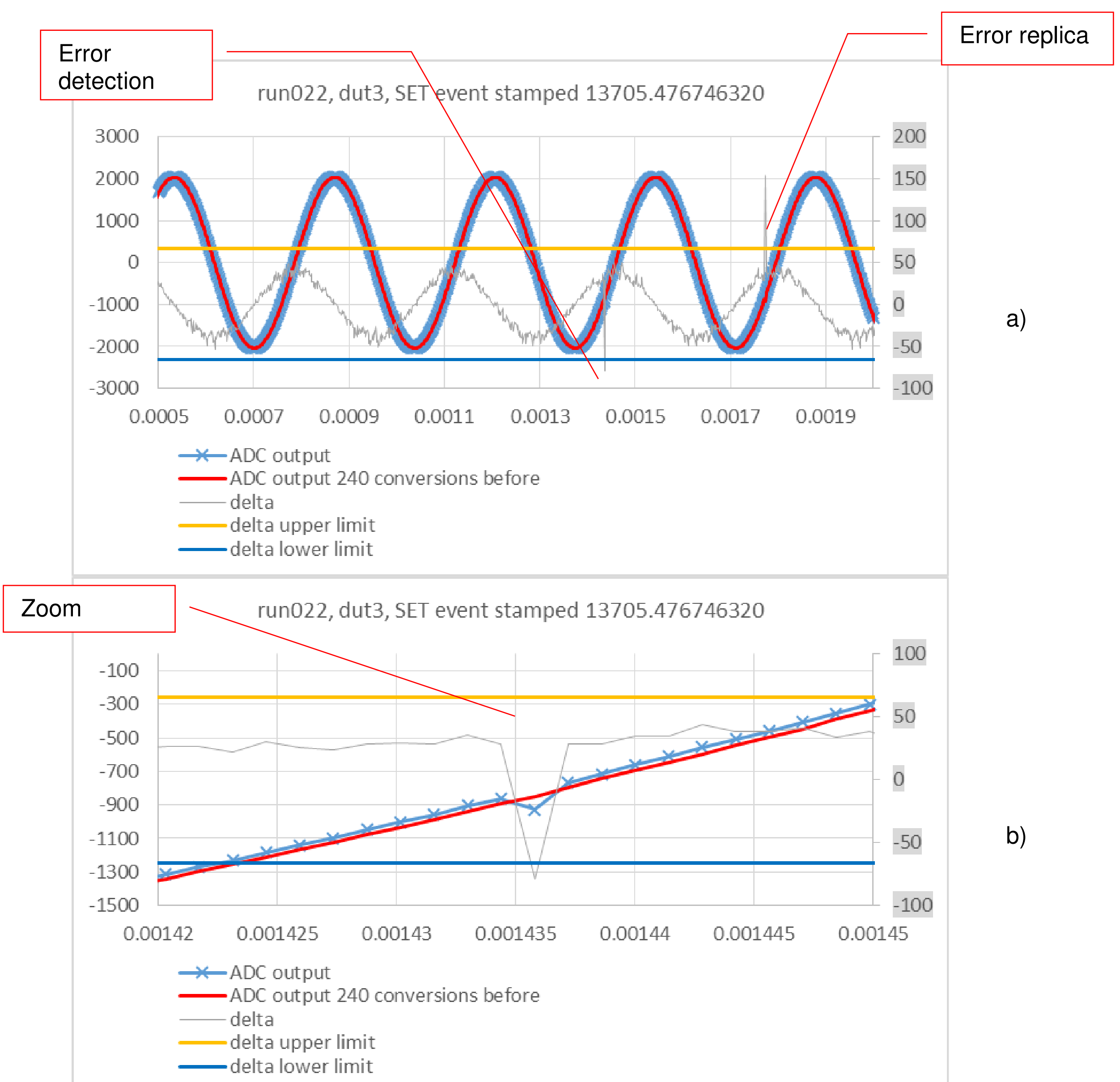
Figure 6 – Radef, February 2015, ADC128S102,SET cross-section / device as a function of LET

								ch3	ch2	ch1							DUT1					DUT2					DUT3				
Facility	medium	run_number	Facility_run_number	dut_part_id	power_config	test_mode	temperature	SEL DUT1 (UI3)	SEL DUT2 (UI7)	SEL DUT3 (UI11)	Ion	LET	tilt	Eff. LET	on_fluence	run_duration	DUT1_X-section_SEL	error bar up	error bar down	delta up	delta down	DUT2_X-section_SEL	error bar up	error bar down	delta up	delta down	DUT3_X-section_SEL	error bar up	error bar down	delta up	delta down
RADEF	vacuum	1	9	1	3.3	SEL		1	0	4	Xe	60	0	60.0	9.97E+06	1112	1.00E-07	5.59E-07	2.03E-09	4.6E-07	9.8E-08	0.00E+00	3.70E-07	0.00E+00	3.7E-07	0.0E+00	4.01E-07	1.03E-06	1.07E-07	6.3E-07	2.9E-07
RADEF	vacuum	5	13	1	3.63	SEL	50	3	6	6	Xe	60	30	69.3	1.16E+07	595	2.59E-07	7.57E-07	5.18E-08	5.0E-07	2.1E-07	5.18E-07	1.13E-06	1.86E-07	6.1E-07	3.3E-07	5.18E-07	1.13E-06	1.86E-07	6.1E-07	3.3E-07
RADEF	vacuum	7	15	1	3.63	SEL	50	5	8	13	Xe	60	45	84.9	9.50E+06	524	5.26E-07	1.23E-06	1.67E-07	7.0E-07	3.6E-07	8.42E-07	1.66E-06	3.56E-07	8.2E-07	4.9E-07	1.37E-06	2.35E-06	7.14E-07	9.8E-07	6.5E-07
RADEF	vacuum	10	18	1	3.63	SEL	50	0	0	0	Kr	32.2	45	45.5	1.00E+07	346	0	3.67E-07	0	3.7E-07	0	0	3.67E-07	0	3.7E-07	0	0	3.67E-07	0	3.7E-07	0

Table 2 – RADEF, February 2015, ADC128S102, SEL test runs

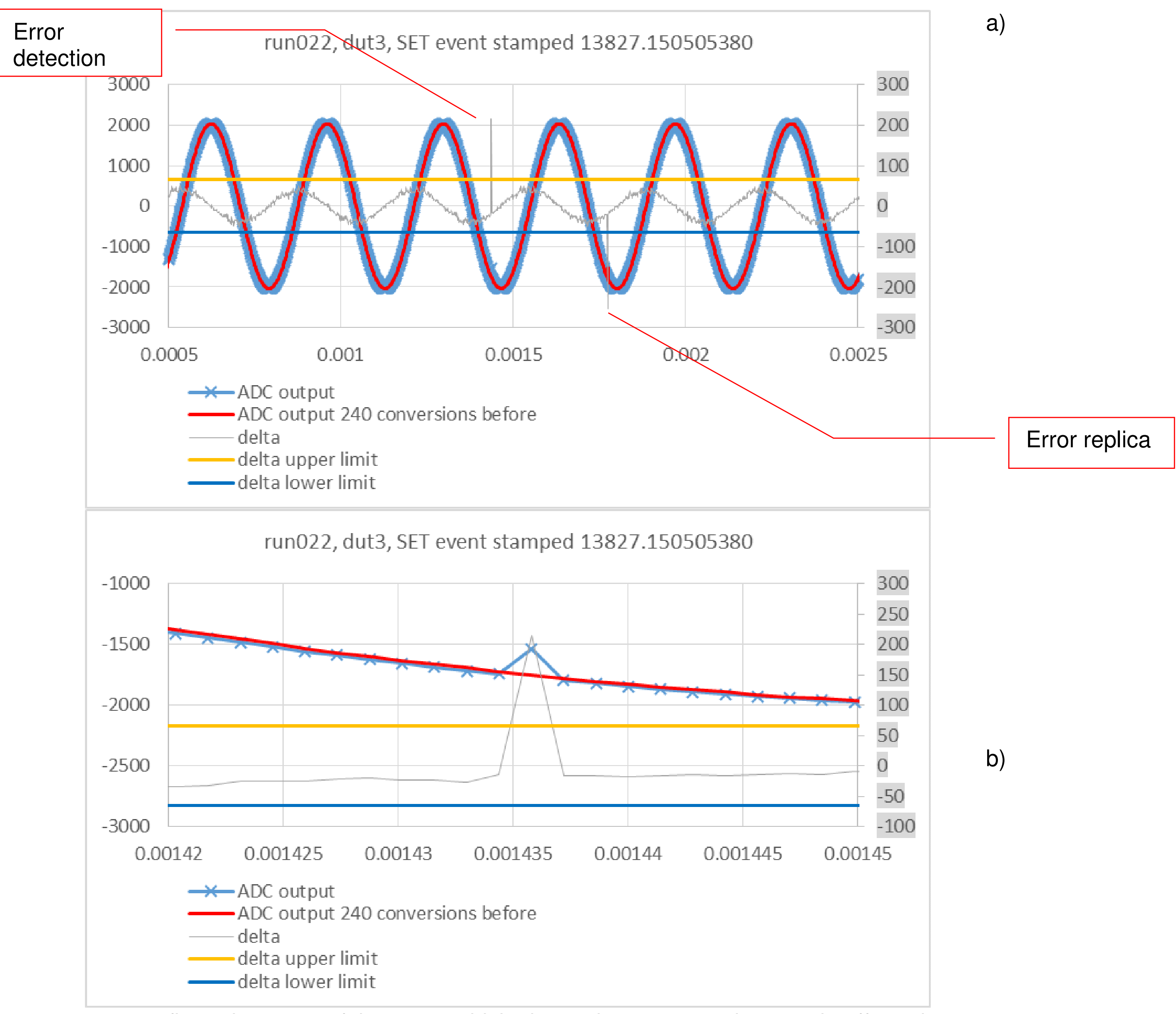
								ch3	ch1													DUT1					DUT3				
Facility	medium	run_number	Facility_run_number	board_part_id	power_config	test_mode	temperature	DUT1 (UI3)	DUT3 (UI11)	Ion	LET	tilt	Eff. LET	on_fluence	run_duration	SET_DUT1	SEFI_DUT1	Step_current_DUT1	SET_DUT3	SEFI_DUT3	Step_current_DUT3	SET_X-section_DUT1	error bar up	error bar down	delta up	delta down	SET_X-section_DUT3	error bar up	error bar down	delta up	delta down
RADEF	vacuum	16	23	1	2.97	SET	25	0	0	Kr	32.1	0	32.1	6.0E+06	668	-	-	-	18	0	0	-	-	-	-	-	3.0E-06	4.8E-06	1.7E-06	1.8E-06	1.3E-06
RADEF	vacuum	17	24	1	2.97	SET	25	0	0	Fe	18.5	0	18.5	1.3E+07	519	-	-	-	14	0	0	-	-	-	-	-	1.1E-06	1.8E-06	5.7E-07	7.3E-07	4.9E-07
RADEF	vacuum	38	45	1	2.97	SET	25	0	0	Ne	3.63	56	6.5	2.0E+06	72	-	-	-	0	0	0	-	-	-	-	-	0	1.8E-06	0	1.8E-06	0
RADEF	vacuum	11	19	2	2.97	SET	25	0	0	Kr	32.2	0	32.2	9.6E+06	546	52	1	1	19	1	1	5.4E-06	7.2E-06	3.9E-06	1.8E-06	1.5E-06	0	3.1E-06	1.2E-06	3.1E-06	-1.2E-06
RADEF	vacuum	20	27	2	2.97	SET	25	0	0	Fe	18.5	0	18.5	5.0E+07	552	71	0	0	63	0	0	1.4E-06	1.8E-06	1.1E-06	4.0E-07	3.4E-07	1.3E-06	1.6E-06	9.4E-07	3.7E-07	3.2E-07
RADEF	vacuum	22	29	2	2.97	SET	25	0	0	Xe	60	0	60.0	2.2E+06	746	10	1	1	11	2	2	4.5E-06	8.2E-06	2.1E-06	3.8E-06	2.4E-06	4.9E-06	8.8E-06	2.4E-06	3.9E-06	2.5E-06
RADEF	vacuum	34	41	2	2.97	SET	25	0	0	Ar	10.2	0	10.2	2.0E+06	177	0	0	0	0	0	0		1.8E-06	0.0E+00	1.8E-06	0.0E+00	0	1.8E-06	0	1.8E-06	0
RADEF	vacuum	39	46	2	2.97	SET	25	0	0	Ne	3.63	0	3.6	2.1E+06	59	0	0	0	0	0	0		1.8E-06	0.0E+00	1.8E-06	0.0E+00	0	1.8E-06	0	1.8E-06	0

Table 3 – RADEF, February 2015, ADC128S102, SET test runs



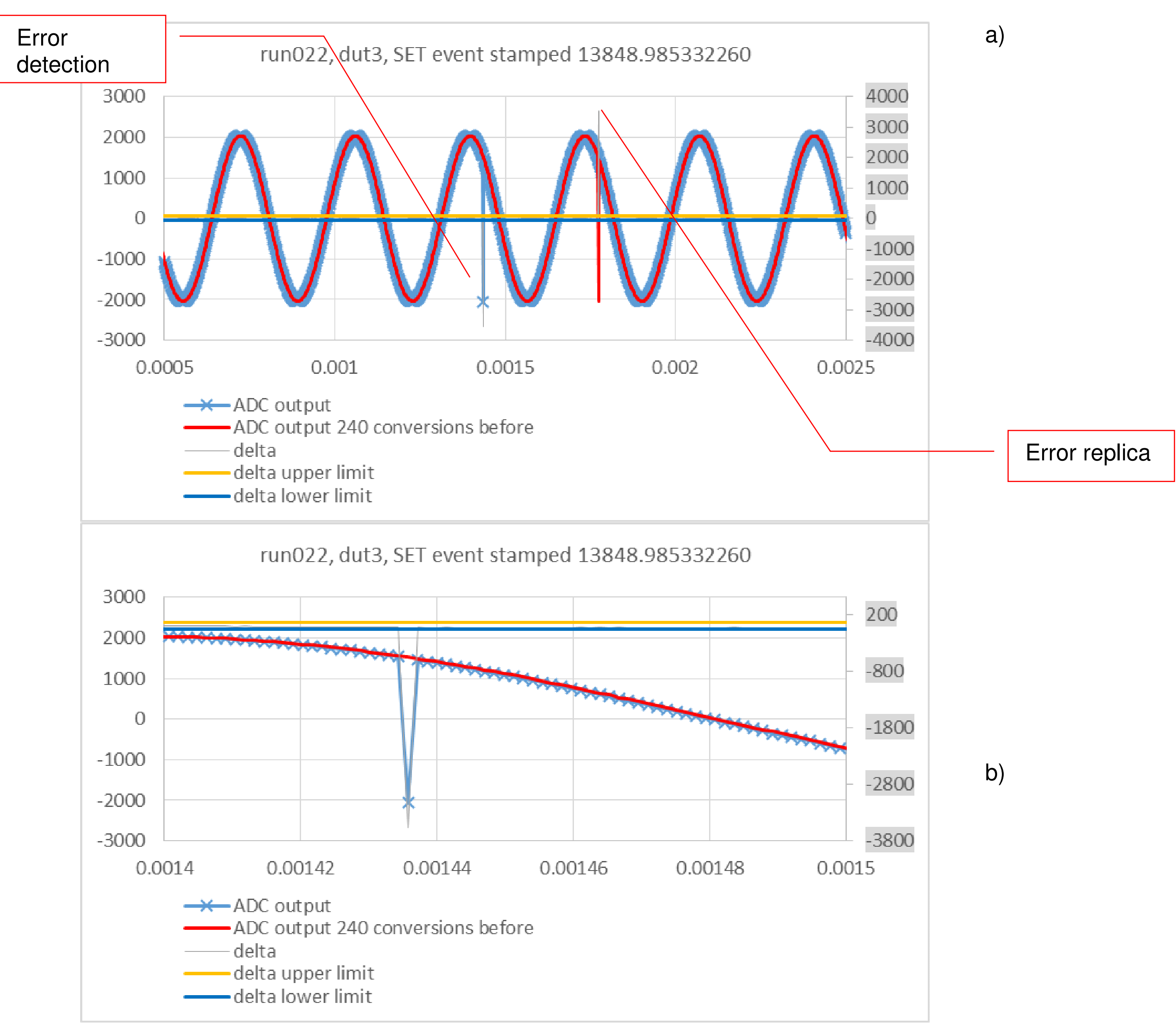
- In figure b, zoom of the event which show that 1 conversion only is affected

Figure 7 – run022, dut3, small SET event stamped 13705.476746320



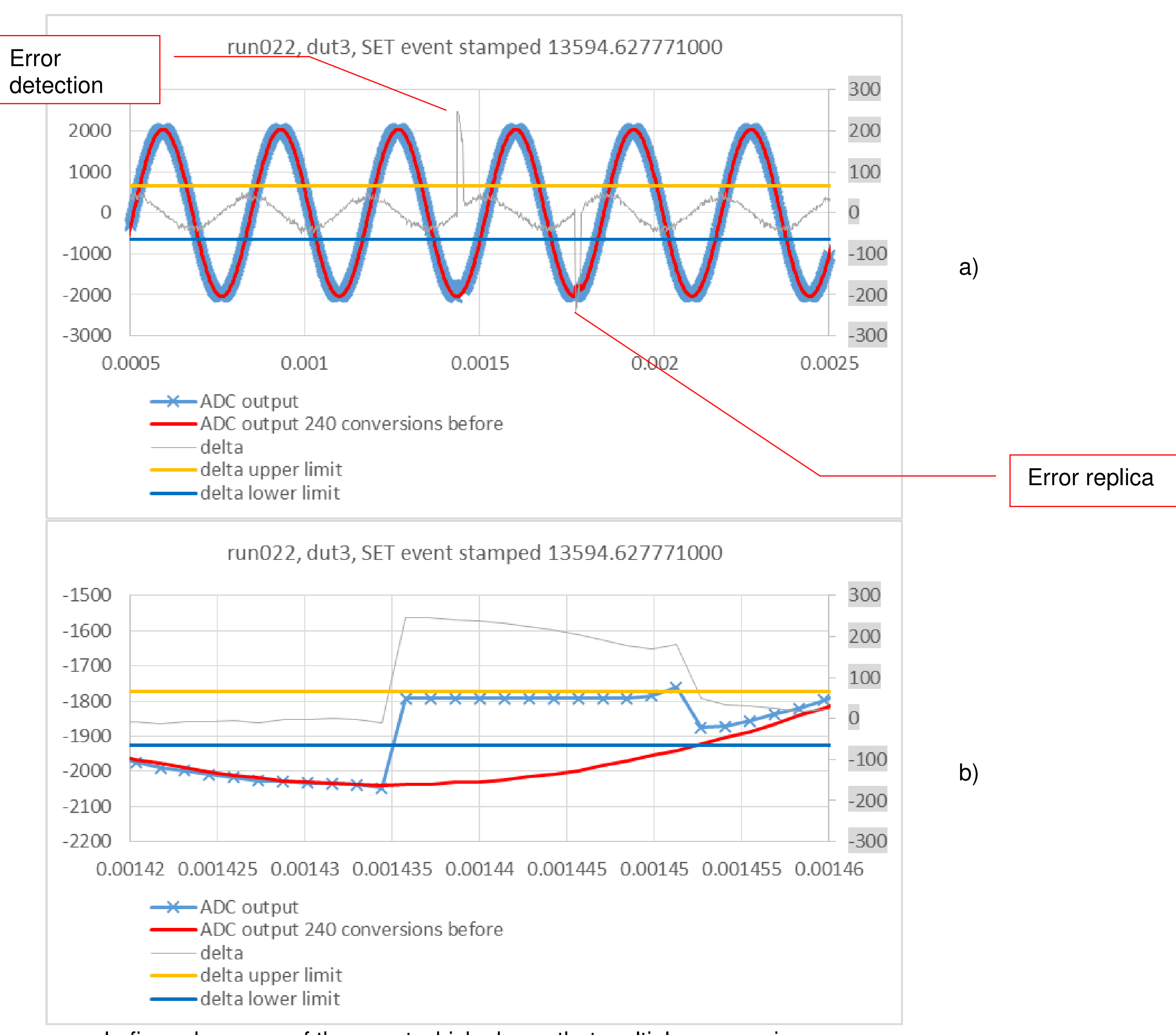
- In figure b, zoom of the event which shows that 1 conversion only is affected

Figure 8 – run022, dut3, SET event stamped 13827.150505380



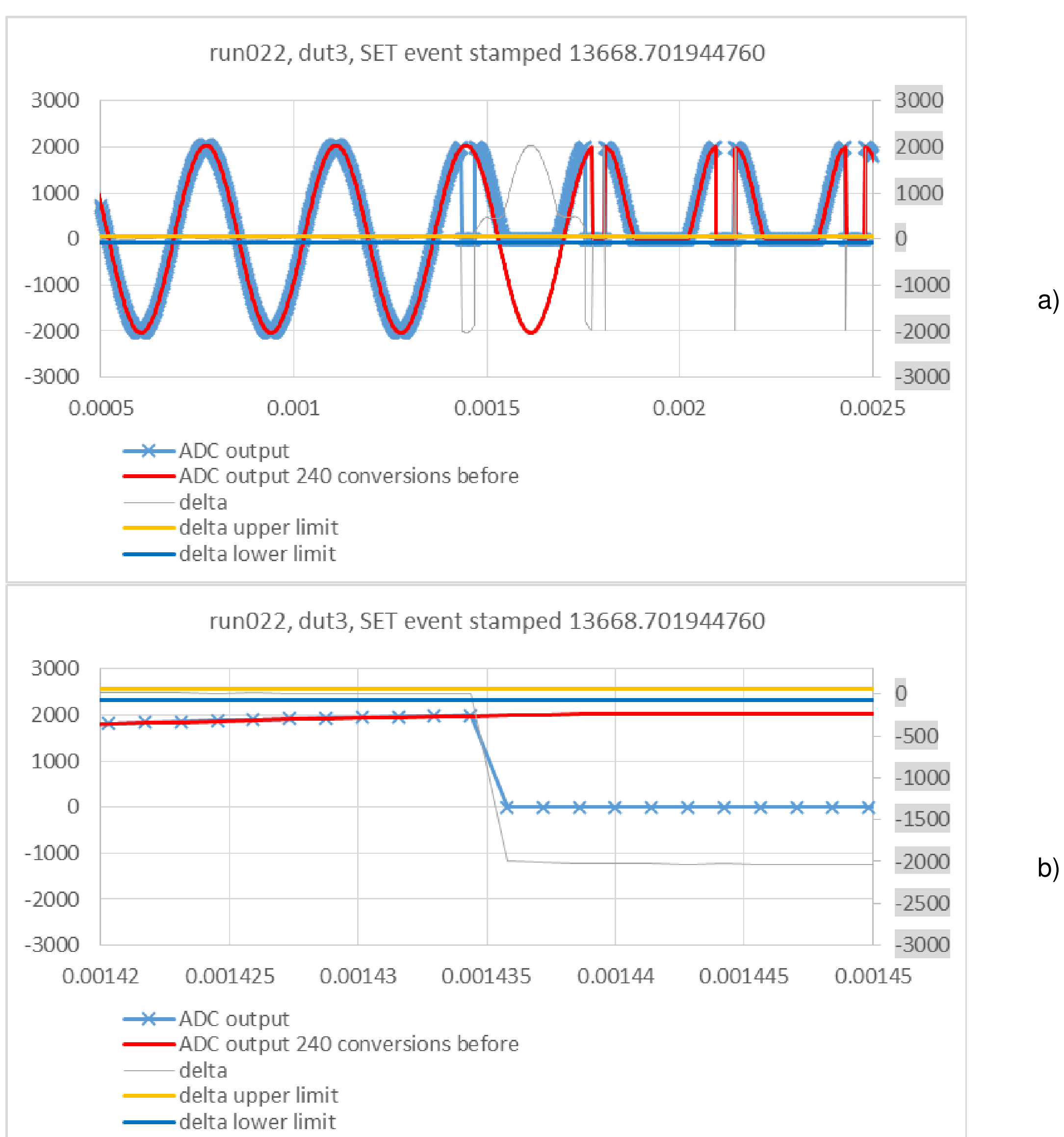
- In figure b, zoom of the event which shows that 1 conversion only is affected

Figure 9 – run022, dut3, very large SET event stamped 13848.985332260



- In figure b, zoom of the event which shows that multiple successive concersions are affected

Figure 10 – run022, dut3, SET event with multiple successive errors stamped 13594.627771000



- In figure a one can see the delta value that triggered the event recording. The error is present for the consecutive periods which explains why the delta value may be inside the limits during the remaining record length
- In figure b, zoom allows to see the change

Figure 11 – run022, dut3, SEFI event stamped 13668.701944760

9 Conclusion

With SEL bias conditions (V=3.6V), SEL events have been recorded on VA supply with Xenon at a LET of 60MeV/(mg/cm²) and higher, recorded SEL current being of about 180mA magnitude.
Step current increases have been detected with krypton LET, 32 MeV/(mg/cm²) and higher, step currents magnitude well below the SEL detection value for VA. These step currents are associated with the presence of SEFIs at the ADC output. A manual power reset is needed to both cure the current step and the SEFI. These errors could be due to conflicts in the logic blocks.
SET events have been recorded and are all single conversion error with the exception of one event recorded during run022.