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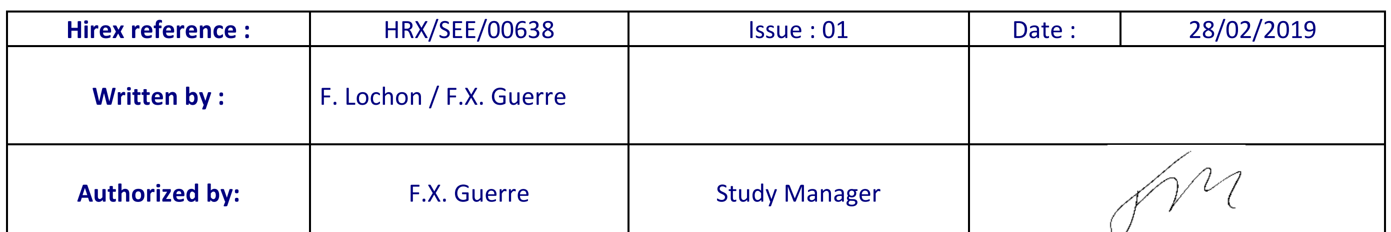
**Single Event Effects**

**Heavy Ion Test Report**

| | |
|---|---|
| Test type | Single-Event Upset, Single Event Latchup, SEFI |
| Part Reference | K4B4G0846Q |
| Tested function | DDR3L SDRAM |
| Chip manufacturer | Samsung |
| Test Facility | RADEF, University of Jyväskylä |
| Test Date | December 2017, January 2018 |
| Customer | ESA ESTEC |

**Esa Estec Purchase Order N° 4000112477/14/NL/HB dated December 4th, 2014**

BCE 5524



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# 1 Introduction

This report presents results of SEE heavy ion test campaigns for the Samsung DDR3L SDRAM K4B4G0846Q. 4 parts were used with 2 parts per test mode, high speed and low speed. The test campaign took place at RADEF, University of in December 2017 and January 2018.

# 2 Applicable and Reference Documents

### Applicable Documents

AD-1 Samsung K4B4G0846Q 4Gb DDR3L SDRAM Datasheet, Rev. 1.0, Jun. 2013

AD-2 K4B4G0846Q physical analysis HRX/RCA/00105

### Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

# 3 Device Information

Device description

K4B4G0846Q, DDR3L SDRAM

| | | |
|---|---|---|
| Manufacturer: | Samsung | |
| Package: | 78-Ball FBGA 11 x 10 mm | |
| Marking: | SEC 510 HYKO K4B4G0846Q | EKA3R9GDC |
| Date code | 1510 | |
| Technology: | CMOS | |
| Die dimensions: | 7.3 x 8.6 mm | |

This 4Gb memory is composed of 1 die with 8 banks of 1024 rows by 65536 columns of 8 bits words.

Device and die identification

Figure 1: Package, top.

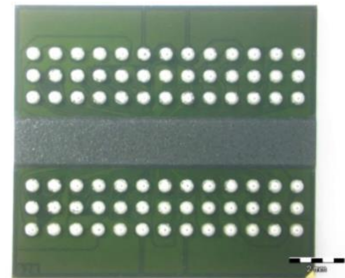


Figure 2: Package, bottom.

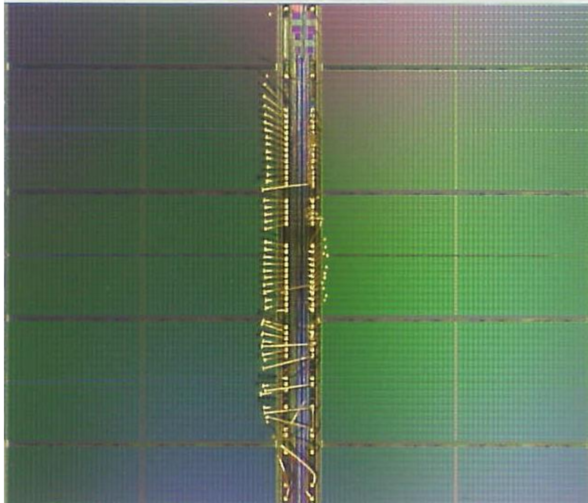


Figure 3: Die view.

Figure 4: Die marking.

Sample preparation

Each DUT has been prepared by die back thinning. The table here below gives the results of this preparation step.

| Board # | Mean thickness (µm) | Max (µm) | Min (µm) |
|---|---|---|---|
| 1 | 61.5 | 69 | 50 |
| 2 | 69 | 77 | 59 |
| 6 | 78 | 84 | 67 |
| 7 | 83 | 90 | 67 |
| 8 | 68 | 75 | 58 |

# 4 Test Setup

Figure 5 shows the principle of the single event test system.
The test system is based on a Kintex7 FPGA (Xilinx).
The test board includes 2 slots for high speed and low speed SODDIMM daughter boards on which is mounted one DUT memory.
The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 24 independent channels.
The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.
One DUT (low speed or high speed) is exposed at a time

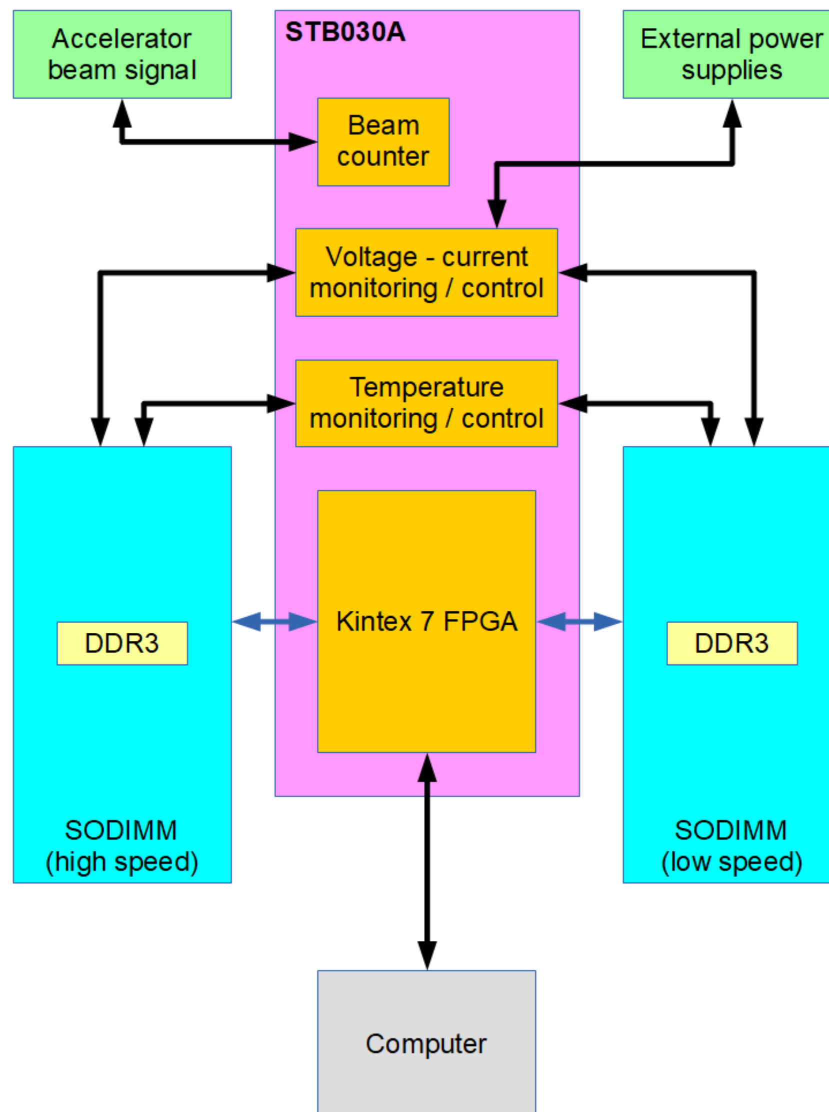



**Figure 5: Hirex SEE test setup**

# 5 Test sequences

Low speed mode is performed at a DUT clock frequency of 325MHz while high speed is performed at 700MHz. Refresh time is set to 6.8µs.

Read/Write sequence

- Repeat cycles:
  - Write memory with 0x55 /0xAA
  - Wait 1s
  - First Read memory (R1)
  - Second Read memory (R2)

Before the test campaigns, the following has been checked:

- Write the entire memory
- Then repeat cycles
  - Load register step or a Reset DDR3
  - Read memory

No error could be detected

That is why the basic Read/Write sequence have been modified to create 2 new test sequences.

Read/Write with load registers sequence

- Repeat cycles:
  - Load MRS
  - Wait 0.1s
  - Write memory with 0x55 /0xAA
  - Wait 0.5s
  - Load MRS
  - Wait 0.1s
  - First Read memory (R1)
  - Second Read memory (R2)

Read/Write with DUT reset sequence

- Repeat cycles:
  - Reset DDR3
  - Wait 0.1s
  - Write memory with 0x55 /0xAA
  - Wait 0.5s
  - Reset DDR3
  - Wait 0.1s
  - First Read memory (R1)
  - Second Read memory (R2)

The two functions Load MRS and Reset DDR3 are detailed here below

**Load MRS**
re-program mode registers MR0-MR3 of the DDR3 memory via MRS command

**Reset DDR3**
used to clear all state information in the DDR3 memory device.
The reset sequence as preconized by devices datasheets and JEDEC standard No. 79-3F is the following:

1- Physical reset (Warm reset) using DDR3 RESET# pin
2- Load mode registers via MRS command
3- ZQ Calibration used to calibrate the DDR3 memory output drivers and ODT (On-Die Termination) values via ZQCL command

# 6 RADEF facility

The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.

The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula,

$$130\ Q^2/M,$$

where Q is the ion charge state and M is the mass in Atomic Mass Units.

## 6.1 Test chamber

Irradiation of components is performed in a vacuum chamber with an inside diameter of 75 cm and a height of 81 cm.

The vacuum in the chamber is achieved after 15 minutes of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the X, Y and Z directions. The possibility of rotation around the Y-axis is provided by a round table. The free movement area reserved for the components is 25 cm x 25 cm, which allows one to perform several consecutive irradiations for several different components without breaking the vacuum. The assembly is equipped with a standard mounting fixture. The adapters required to accommodate the special board configurations and the vacuum feed-throughs can also be made in the laboratory's workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components.

A CCD camera with a magnifying telescope is located at the other end of the beam line to determine accurate positioning of the components. The coordinates are stored in the computer's memory allowing fast positioning of various targets during the test.

## 6.2 Beam quality control

For measuring beam uniformity at low intensity, a CsI(Tl) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis.

A set of four collimated PIN-CsI(Tl) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.

Two beam wobblers and/or a 0.5 microns diffusion Gold foil can be used to achieve good beam homogeneity. The foil is placed 3 m in front of the chamber. The wobbler-coils vibrate the beam horizontally and vertically, the proper sweeping area being attained with the adjustable coil-currents.

## 6.3 Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI(Tl) detectors. Three collimators of different size and shape are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.

At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(Tl) detectors.

## 6.4 Used ions

| Ion | $LET^{SRIM}$ at surface [MeV.cm$^2$.mg$^{-1}$] | Range [µm] | Beam energy [MeV] |
|---|---|---|---|
| $^{15}N^{4+}$ | 1.83 | 202 | 139 |
| $^{20}Ne^{6+}$ | 3.63 | 146 | 186 |
| $^{40}Ar^{12+}$ | 10.2 | 118 | 372 |
| $^{56}Fe^{15+}$ | 18.5 | 97 | 523 |
| $^{82}Kr^{22+}$ | 32.1 | 94 | 768 |
| $^{131}Xe^{35+}$ | 60.0 | 89 | 1217 |

SRIM-2003.26

**Table 1 - Ion beam setting**

# 7 Test conditions.

SEU tests were carried out closed to Vddmin at 1.30V and room temperature (1.35V and room temperature during January 2018 campaign).
Each memory present 8 banks of 65536 columns by 1024 rows of 8-bit words.
Each memory plane is traversed by bank, column, row which means that bank0, column0, row 0 to row 1023 is read, then bank0, column1, row 0 to row 1023, etc.
Read is done by burst which corresponds to 8 words. Each time at least 1 word is in error among the 8 words, the burst is recorded.

# 8 Detailed results

## 8.1 Read/write sequence

Results are summarized in. Table 2

The meaning of the different column headers of Table 2 are explicided here below.
Pre-run errors
Stuck bits present before exposure. They could have been created during previous runs on the DUT.
R1 bit errors
Number of errors detected during READ1 but not during READ2. These errors which represent reading errors are very few and affect only a limited number of READ1 steps.
R1/R2 bit errors
Number of errors detected during READ1 and during READ2. These errors represent SEU WRITE bit errors or SEU cells errors occurring during the time the cell is not written (as for instance during WAIT step but not only).
R2 bit errors
Number of errors detected during READ2 only: These errors represent reading errors which are expected to be quite few as for R1 bit errors and the SEU cells errors occurring during the time the cell is not read.
Persistent bit errors
Bit errors that last more than one sequence iteration. Part of these errors can persist up to the end of the run and are then counted as post-run bit errors (stuck bits). Pre-run errors have been subtracted from the persistent bit error count.
Colum error
Likely an error in the logic. A column error can affect two banks at a time.
Row errors
Likely an error in the logic. Consist in a portion of row in error in a bank.
SEFI
These errors consist mainly in column errors that persist during several sequence iterations. Most of them induce a count clamped to the limit set at 50000. Only a few involved only a single column. The vast majority have been cured by a manual power reset. Some have disappeared under exposure without any external action.
Post-run bit errors
The errors are stuck bits. All affected words are single bit upset.

Figure 6 shows the SEU bit error cross-section for the 2 test modes, low speed and high speed. Depending on test campaign dates, test was performed with a DUT bias of 1.30V or 1.35V.
No significant difference is observed between the two test modes.

In Figure 6, the points with Xenon are too high to plot a single Weibull Plot.

Figure 7 shows the logic error cross-section per device. Again, no significant difference is observed between the two test modes.

Figure 8 shows the stuck bit error cross-section per bit

| Test campaign date | Facility | dut_medium | run_number | Facility_run_number | board_id | power_config | bias_config | test_mode | temperature | Ion | tilt | Average silicon die thickness | LET at die silicon back | Effective LET at active die surface | run_duration | entered_fluence | eff. Fluence | pre-run errors | R1 | R1R2 | R2 | persistent | post run errors | total cells error | capacity | Cell error cross-section | col error | row error | Large error clamped to limit | Large event type2 | sefi | total logic error | Logic error cross-section | Stuck bit cross-section j bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W50-2017 | RADEF | vacuum | 34 | 59 | S1 | 1.3 | HS | read write | room | N | 0 | 61 | 1.83 | 2 | 274 | 2.0E+06 | 2.0E+06 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4.3E+09 | | 0 | 0 | 0 | 0 | 0 | 0 | | |
| W50-2017 | RADEF | vacuum | 38 | 63 | S1 | 1.3 | HS | read write | room | Fe | 0 | 61 | 18.5 | 26.54 | 412 | 2.0E+05 | 2.0E+05 | 0 | 8 | 3 | 2 | 13 | 0 | 26 | 4.3E+09 | 3.0E-14 | 3 | 7 | 0 | 0 | 0 | 10 | 5.0E-05 | |
| W50-2017 | RADEF | vacuum | 61 | 84 | S1 | 1.3 | HS | read write | room | Kr | 0 | 61 | 32.2 | 37 | 360 | 2.0E+05 | 2.0E+05 | 0 | 7 | 4 | 1 | 12 | 0 | 24 | 4.3E+09 | 2.8E-14 | 5 | 2 | 0 | 0 | 1 | 8 | 4.0E-05 | |
| W50-2017 | RADEF | vacuum | 33 | 58 | S2 | 1.3 | HS | read write | room | N | 0 | 69 | 1.83 | 2 | 232 | 2.0E+06 | 2.0E+06 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4.3E+09 | | 1 | 0 | 0 | 0 | 0 | 1 | 5.0E-07 | |
| W50-2017 | RADEF | vacuum | 62 | 85 | S2 | 1.3 | HS | read write | room | Kr | 0 | 69 | 32.2 | 41 | 344 | 2.0E+05 | 2.0E+05 | 0 | 12 | 12 | 0 | 24 | 0 | 48 | 4.3E+09 | 5.6E-14 | 4 | 9 | 0 | 0 | 2 | 15 | 7.5E-05 | |
| W06-2018 | RADEF | vacuum | 5 | 42 | s6 | 1.35 | HS | read write | room | Ar | 0 | 78 | 10.2 | 15.26 | 920 | 2.0E+06 | 2.0E+06 | 0 | 1 | 47 | 44 | 1 | 0 | 93 | 4.3E+09 | 1.1E-14 | 15 | 34 | 0 | 2 | 2 | 53 | 2.7E-05 | |
| W06-2018 | RADEF | vacuum | 23 | 57 | s6 | 1.35 | HS | reset ddr3 | room | Kr | 0 | 78 | 32.2 | 37 | 679 | 2.0E+06 | 2.0E+06 | 24 | | | | | 23 | 787 | 4.3E+09 | 9.2E-14 | 41 | 48 | 2 | 1 | **0** | 92 | 4.6E-05 | 2.7E-15 |
| W06-2018 | RADEF | vacuum | 1 | 39 | s7 | 1.35 | HS | read write | room | Ar | 0 | 83 | 10.2 | 15.86 | 1050 | 2.0E+06 | 2.0E+06 | 0 | 0 | 24 | 20 | 0 | 0 | 44 | 4.3E+09 | 5.1E-15 | 21 | 49 | 1 | 4 | 0 | 75 | 3.8E-05 | |
| W06-2018 | RADEF | vacuum | 28 | 62 | s7 | 1.35 | HS | reset ddr3 | room | Kr | 0 | 83 | 32.2 | 32 | 1009 | 2.0E+06 | 2.0E+06 | 8 | 6 | 242 | 236 | 219 | | 703 | 4.3E+09 | 8.2E-14 | 43 | 82 | 2 | 1 | **0** | 128 | 6.4E-05 | |
| W17-2018 | RADEF | vacuum | 6 | 6 | s8 | 1.35 | HS | reset ddr3 | room | Kr | 0 | 68 | 32.2 | 41 | 944 | 1.0E+06 | 1.0E+06 | 0 | 5 | 141 | 176 | 26 | | 348 | 4.3E+09 | 8.1E-14 | 27 | 67 | 1 | 0 | **0** | 95 | 9.5E-05 | |
| W17-2018 | RADEF | vacuum | 12 | 12 | s8 | 1.35 | HS | read write | room | Xe | 0 | 68 | 60 | 59.2 | 589 | 1.0E+06 | 1.0E+06 | 4 | | | | | 406 | 5709 | 4.3E+09 | 1.3E-12 | 74 | 54 | 1 | 0 | 8 | 137 | 1.4E-04 | 9.5E-14 |
| W50-2017 | RADEF | vacuum | 32 | 57 | S1 | 1.3 | LS | read write | room | N | 0 | 61 | 1.83 | 2 | 222 | 2.0E+06 | 2.0E+06 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4.3E+09 | | 0 | 0 | 0 | 0 | 0 | 0 | | |
| W50-2017 | RADEF | vacuum | 63 | 86 | S1 | 1.3 | LS | read write | room | Kr | 0 | 61 | 32.2 | 37 | 356 | 2.0E+05 | 2.0E+05 | 0 | 17 | 4 | 2 | 23 | 1 | 46 | 4.3E+09 | 5.4E-14 | 10 | 5 | 0 | 0 | 0 | 15 | 7.5E-05 | 1.2E-15 |
| W50-2017 | RADEF | vacuum | 35 | 60 | S2 | 1.3 | LS | read write | room | N | 0 | 69 | 1.83 | 2 | 293 | 2.0E+06 | 2.0E+06 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 4.3E+09 | 1.2E-16 | 0 | 2 | 0 | 0 | 0 | 2 | 1.0E-06 | |
| W50-2017 | RADEF | vacuum | 37 | 62 | S2 | 1.3 | LS | read write | room | Fe | 0 | 69 | 18.5 | 28.18 | 189 | 1.0E+06 | 1.0E+06 | 1 | 18 | 19 | 5 | 43 | 0 | 85 | 4.3E+09 | 2.0E-14 | 6 | 28 | 0 | 0 | 1 | 35 | 3.5E-05 | |
| W50-2017 | RADEF | vacuum | 60 | 83 | S2 | 1.3 | LS | read write | room | Kr | 0 | 69 | 32.2 | 41 | 356 | 2.0E+05 | 2.0E+05 | 0 | 30 | 7 | 2 | 39 | 0 | 78 | 4.3E+09 | 9.1E-14 | 5 | 6 | 0 | 0 | 0 | 11 | 5.5E-05 | |
| W06-2018 | RADEF | vacuum | 27 | 61 | s6 | 1.35 | LS | reset ddr3 | room | Kr | 0 | 78 | 32.2 | 37 | 1371 | 2.0E+06 | 2.0E+06 | 26 | 5 | 253 | 274 | 175 | | 707 | 4.3E+09 | 8.2E-14 | 51 | 67 | 4 | 0 | **0** | 122 | 6.1E-05 | |
| W06-2018 | RADEF | vacuum | 6 | 43 | s7 | 1.35 | LS | read write | room | Ar | 0 | 83 | 10.2 | 15.86 | 1002 | 2.0E+06 | 2.0E+06 | 0 | 0 | 29 | 31 | 1 | 0 | 61 | 4.3E+09 | 7.1E-15 | 12 | 29 | 1 | 1 | 2 | 45 | 2.3E-05 | |
| W06-2018 | RADEF | vacuum | 24 | 58 | s7 | 1.35 | LS | reset ddr3 | room | Kr | 0 | 83 | 32.2 | 32 | 692 | 2.0E+06 | 2.0E+06 | 0 | | | | | 12 | 380 | 4.3E+09 | 4.4E-14 | 28 | 56 | 4 | 3 | **0** | 91 | 4.6E-05 | 1.4E-15 |
| W06-2018 | RADEF | vacuum | 2 | 40 | s8 | 1.35 | LS | read write | room | Ar | 0 | 68 | 10.2 | 14.15 | 535 | 1.2E+06 | 2.0E+06 | 0 | 0 | 8 | 26 | 0 | 0 | 34 | 4.3E+09 | 4.0E-15 | 8 | 33 | 0 | 0 | 0 | 41 | 3.5E-05 | |
| W06-2018 | RADEF | vacuum | 3 | 41 | s8 | 1.35 | LS | read write | room | Ar | 0 | 68 | 10.2 | 14.15 | 662 | 2.0E+06 | 2.0E+06 | 0 | 0 | 16 | 46 | 0 | 0 | 62 | 4.3E+09 | 7.2E-15 | 14 | 52 | 1 | 1 | 1 | 69 | 3.5E-05 | |
| W17-2018 | RADEF | vacuum | 4 | 4 | s8 | 1.35 | LS | reset ddr3 | room | Kr | 0 | 68 | 32.2 | 41 | 1608 | 1.0E+06 | 9.7E+05 | 1 | 6 | 125 | 175 | 24 | 13 | 375 | 4.3E+09 | 9.0E-14 | 48 | 64 | 3 | 0 | **1** | 116 | 1.2E-04 | 3.0E-15 |
| W17-2018 | RADEF | vacuum | 16 | 15 | s8 | 1.35 | LS | read write | room | Xe | 0 | 68 | 60 | 59.2 | 743 | 1.0E+06 | 2.5E+05 | 305 | | | | | 765 | 2385 | 4.3E+09 | 2.2E-12 | 17 | 11 | 0 | 0 | 3 | 31 | 1.2E-04 | 1.8E-13 |

**Table 2: Detailed SEE results.**

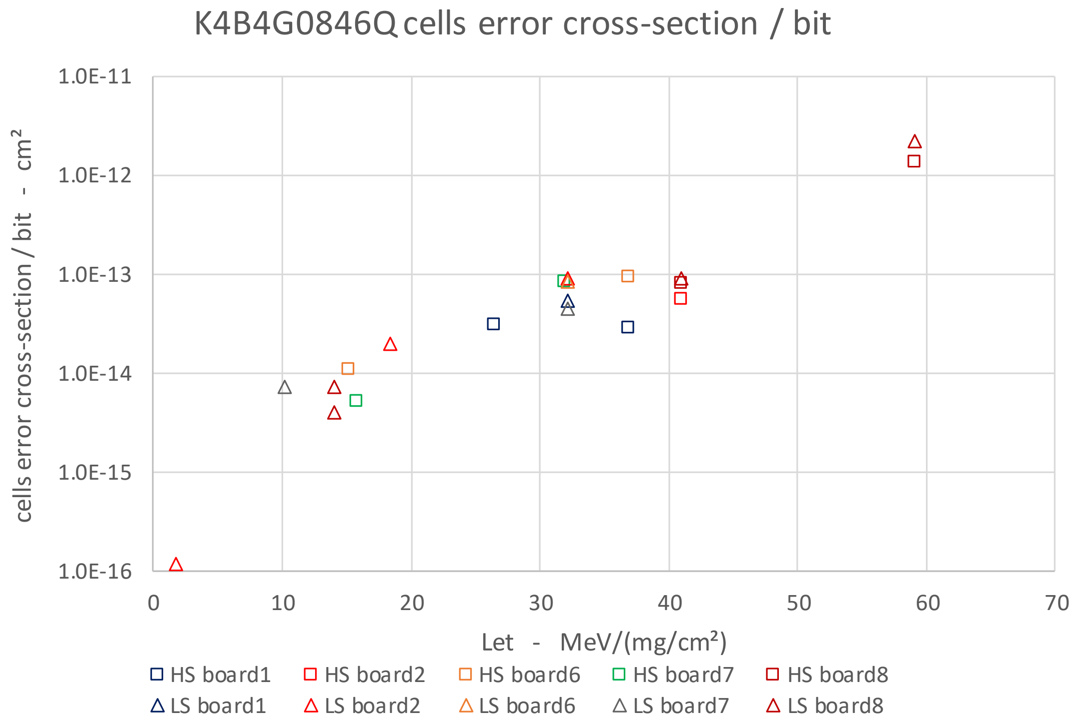



**Figure 6 – H5TC4G83CFR, High Speed and Low Speed Read Write, SEU bit error cross-section / bit**

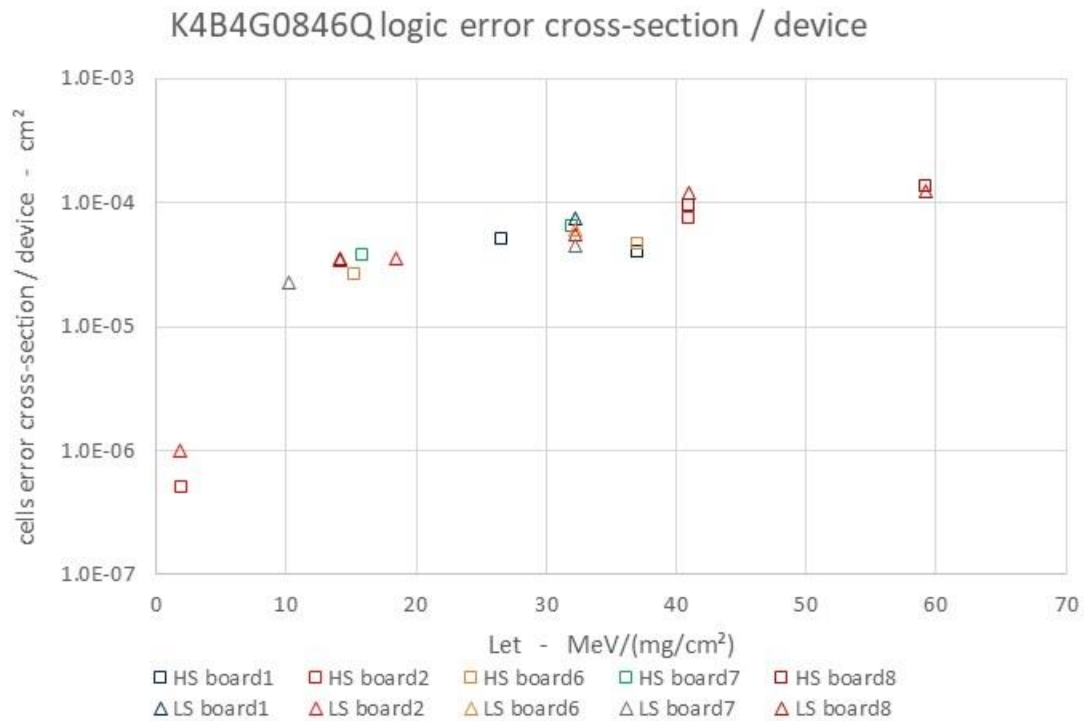



**Figure 7 – Cumulated Logic error cross-section plot**

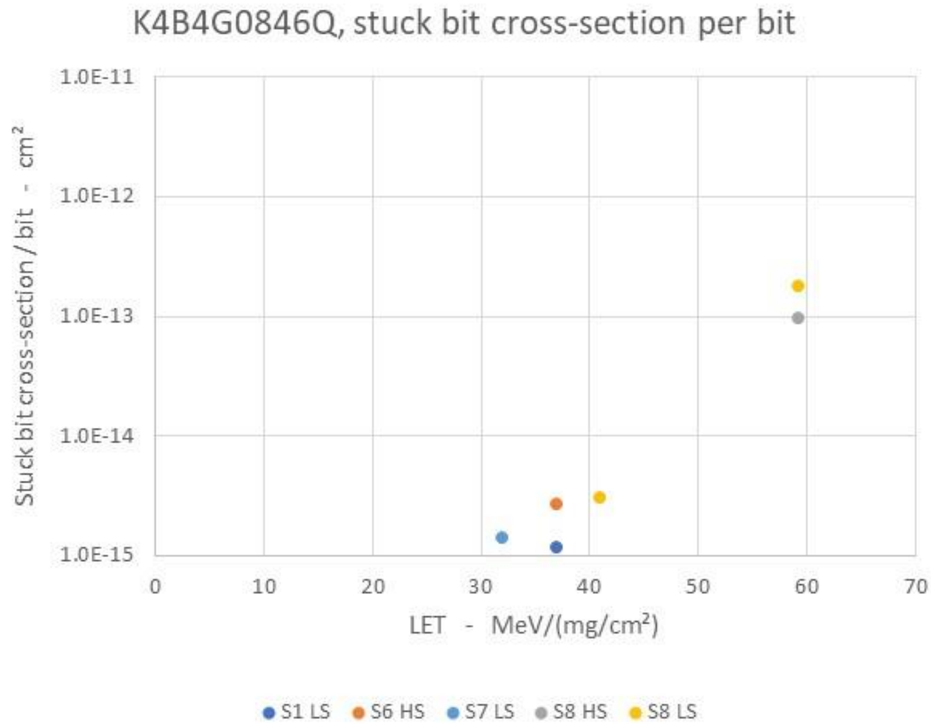



**Figure 8 –stuck bit error cross-section per bit plot**

## 8.2 Read/Write with load registers or DUT reset sequences

Purpose of these sequences was to evaluate the addition in the read/write sequence of steps for either reloading the DUT register content or doing a DUT reset, in SEFI occurrence.
No power reset was performed during these runs to clear SEFI if any.
The corresponding table of runs is shown in Table 3.

The run chronograms are shown in Figure 9 and Figure 10.
The insertion of DRR3 resets in the read write sequence look to help to avoid SEFI occurrence while insertion of load registers steps is not sufficient to avoid any SEFI. However, in Figure 11, with ddr3 reset sequence, one can see the persistence of an error even after beam stop.Figure 1

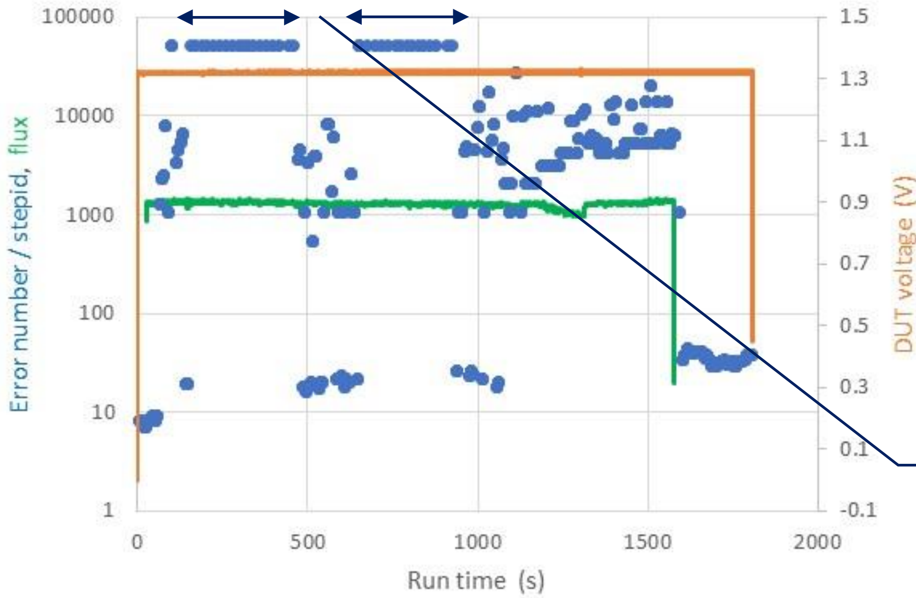
| | Facility | dut_medium | run_number | Facility_run_number | board_id | power_config | bias_config | test_mode | temperature | Ion | tilt | LET at die back sisde | run_duration | entered_fluence |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W06-2018 | RADEF | vacuum | 21 | 55 | s6 | 1.35 | HS | load mrs | room | Kr | 0 | 32.2 | 294 | 7.99E+05 |
| W06-2018 | RADEF | vacuum | 22 | 56 | s6 | 1.35 | HS | load mrs | room | Kr | 0 | 32.2 | 1209 | 2.00E+06 |
| W06-2018 | RADEF | vacuum | 23 | 57 | s6 | 1.35 | HS | reset ddr3 | room | Kr | 0 | 32.2 | 679 | 2.00E+06 |
| **W06-2018** | **RADEF** | **vacuum** | **24** | **58** | **s7** | **1.35** | **LS** | **reset ddr3** | **room** | **Kr** | **0** | **32.2** | **692** | **2.00E+06** |
| W06-2018 | RADEF | vacuum | 25 | 59 | s7 | 1.35 | LS | load mrs | room | Kr | 0 | 32.2 | 1438 | 2.00E+06 |
| W06-2018 | RADEF | vacuum | 26 | 60 | s6 | 1.35 | LS | load mrs | room | Kr | 0 | 32.2 | 1550 | 2.00E+06 |
| **W06-2018** | **RADEF** | **vacuum** | **27** | **61** | **s6** | **1.35** | **LS** | **reset ddr3** | **room** | **Kr** | **0** | **32.2** | **1371** | **2.00E+06** |
| W06-2018 | RADEF | vacuum | 28 | 62 | s7 | 1.35 | HS | reset ddr3 | room | Kr | 0 | 32.2 | 1009 | 2.00E+06 |
| W06-2018 | RADEF | vacuum | 29 | 63 | s7 | 1.35 | HS | load mrs | room | Kr | 0 | 32.2 | 1337 | 2.00E+06 |
| **W17-2018** | **RADEF** | **vacuum** | **1** | **1** | **s7** | **1.35** | **HS** | **reset** | **room** | **Kr** | **0** | **32.2** | **1198** | **1.00E+06** |
| W17-2018 | RADEF | vacuum | 2 | 2 | s7 | 1.35 | HS | load mrs | room | Kr | 0 | 32.2 | 1485 | 1.00E+06 |
| W17-2018 | RADEF | vacuum | 3 | 3 | s8 | 1.35 | LS | load mrs | room | Kr | 0 | 32.2 | 1330 | 1.00E+06 |
| **W17-2018** | **RADEF** | **vacuum** | **4** | **4** | **s8** | **1.35** | **LS** | **reset** | **room** | **Kr** | **0** | **32.2** | **1608** | **1.00E+06** |
| **W17-2018** | **RADEF** | **vacuum** | **5** | **5** | **s7** | **1.35** | **LS** | **reset** | **room** | **Kr** | **0** | **32.2** | **1475** | **1.00E+06** |
| W17-2018 | RADEF | vacuum | 6 | 6 | s8 | 1.35 | HS | reset | room | Kr | 0 | 32.2 | 944 | 1.00E+06 |
| W17-2018 | RADEF | vacuum | 7 | 7 | s8 | 1.35 | HS | load mrs | room | Kr | 0 | 32.2 | 1350 | 1.00E+06 |

**Table 3 – Runs table for Read/write with load registers or DUT reset sequences**

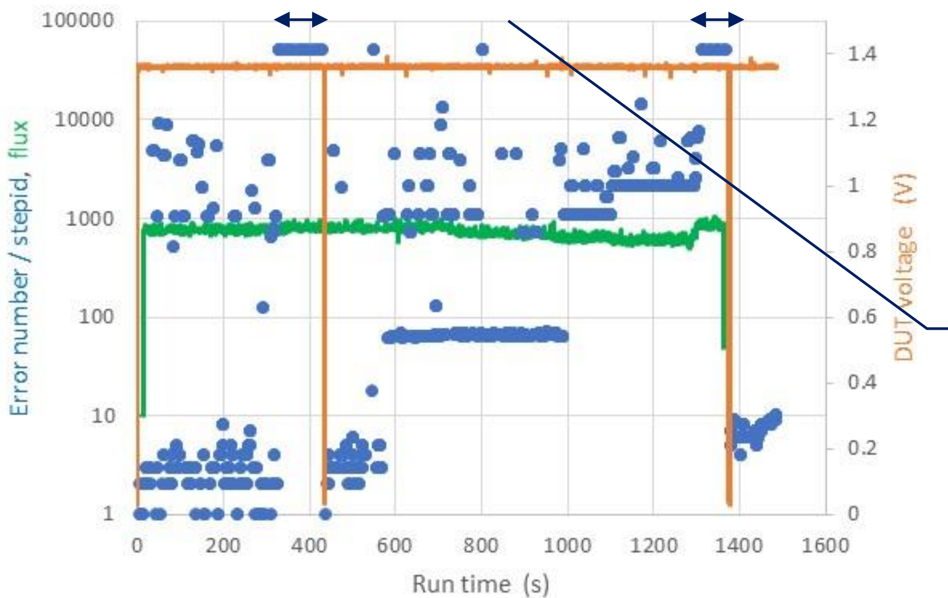
Read/Write sequence including load registers steps

W06Run026 and W17Run07 have been performed with the read/write sequence including load registers and the run chronograms are shown here below.

SEFis are present and are not immediately cured by the reloading of memory registers



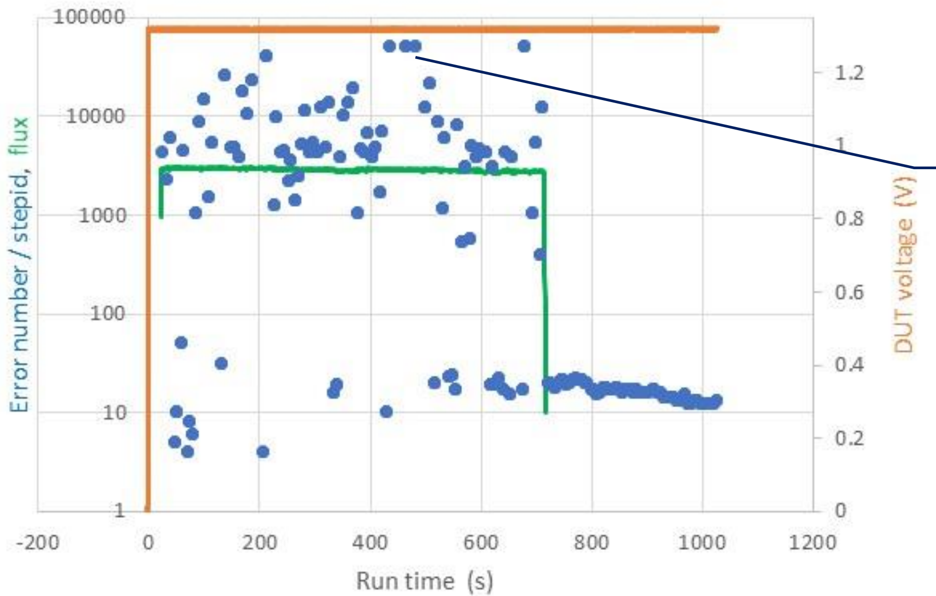

2 Series of clamped (50000) large errors with the same signature healed under beam exposure




2 Series of clamped (50000) large errors with the same signature healed by a power resete

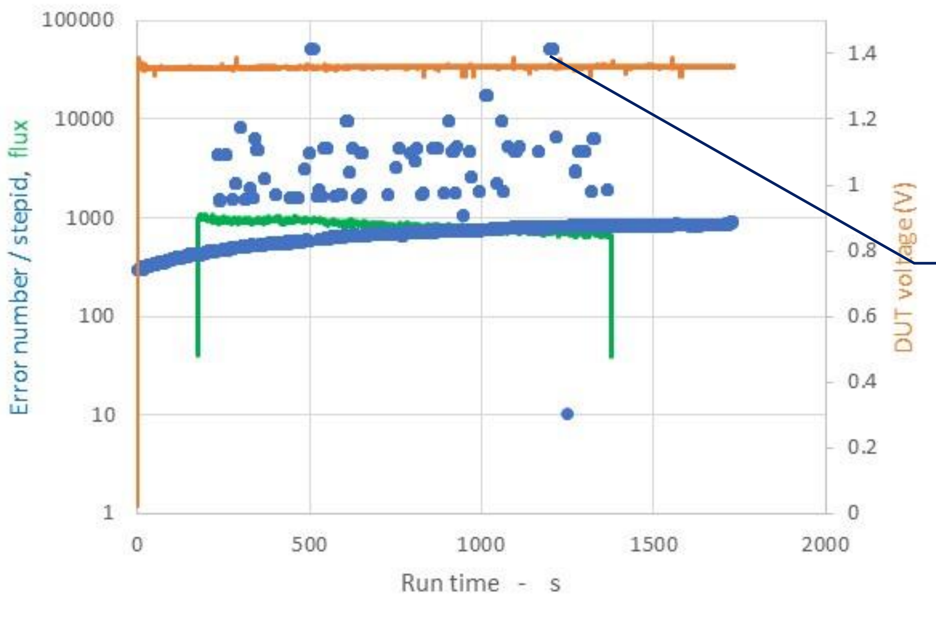
**Figure 9 – Run chronograms for read/write with load registers sequence**

Read/Write sequence including DUT reset steps




No Serie of clamped (50000) large errors.
Only R1 stepid followed by R2 stepid

Not a SEFI




Large event during R1 and R2
Not a SEFI

**Figure 10 – Run chronograms for read/write with DUT reset sequence**

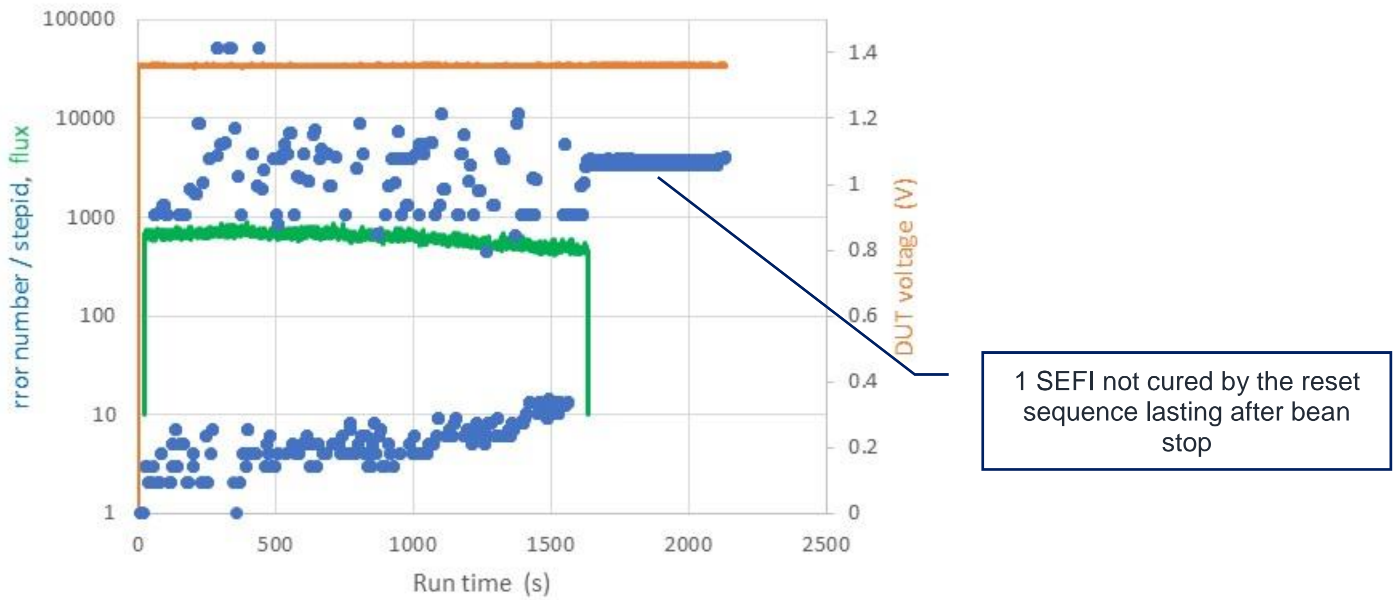



**Figure 11 – Run chronograms for read/write with SEFI during DUT reset sequence**

### 8.3 SEL test runs

During test campaign 2018 W06, 2 runs have been performed with Xenon at 1.45V and a temperature of 85°C.
During SEL testing, read/write sequence was executed with a very low clamp limit for each stepid.
Table 4 list the SEL runs performed.

| Facility | dut_medium | run_number | Facility_run_number | board_id | die silicon thickness µm | power_config | bias_config | test_mode | temperature | Ion | tilt | run_duration | entered_fluence |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RADEF | vacuum | 44 | 74 | s6 | 78 | 1.45 | LS | SEL | 85 | Xe | 0 | 549 | 1.00E+07 |
| RADEF | vacuum | 45 | 75 | s7 | 83 | 1.45 | LS | SEL | 85 | Xe | 0 | 530 | 1.00E+07 |

**Table 4 – Runs table for SEL test runs**

No latch has been observed. However some steps currents can be observed.

The corresponding runs chronograms are shown in Figure 13 and Figure 12.

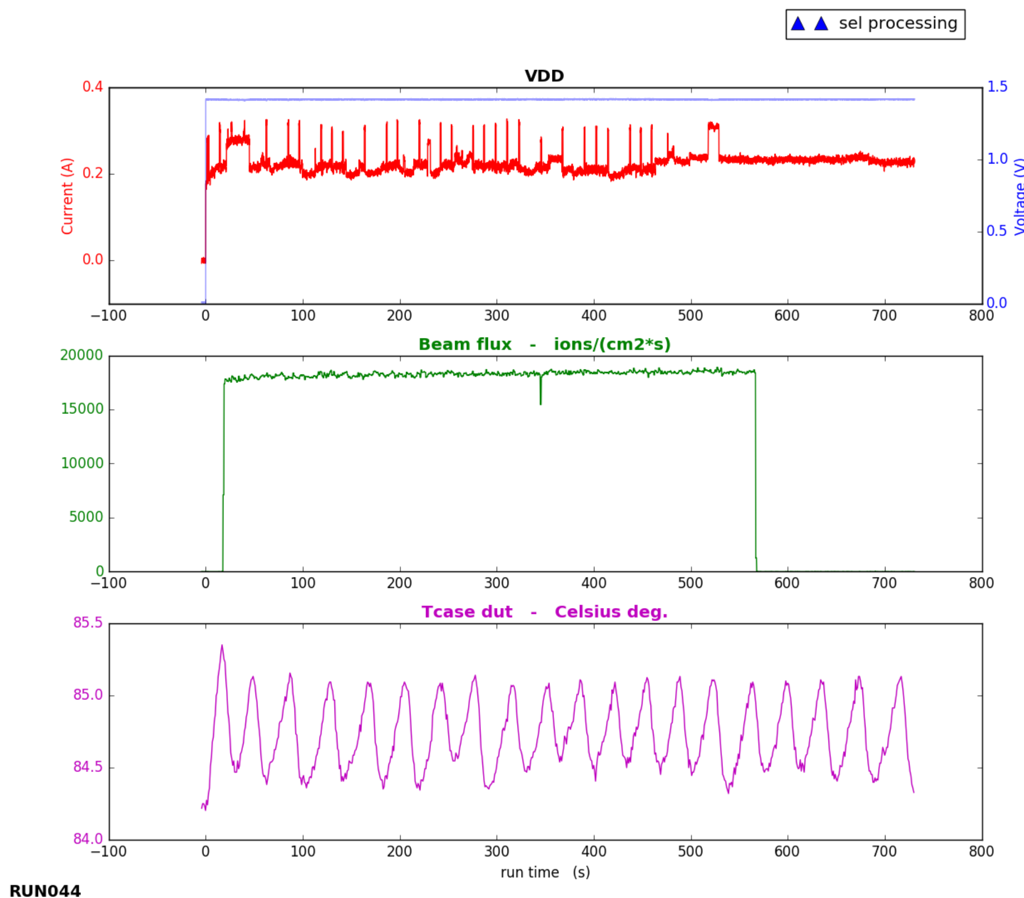



**Figure 12 – K4B4G0846Q, SEL test board 6, Low Speed, Run044 chronogram**

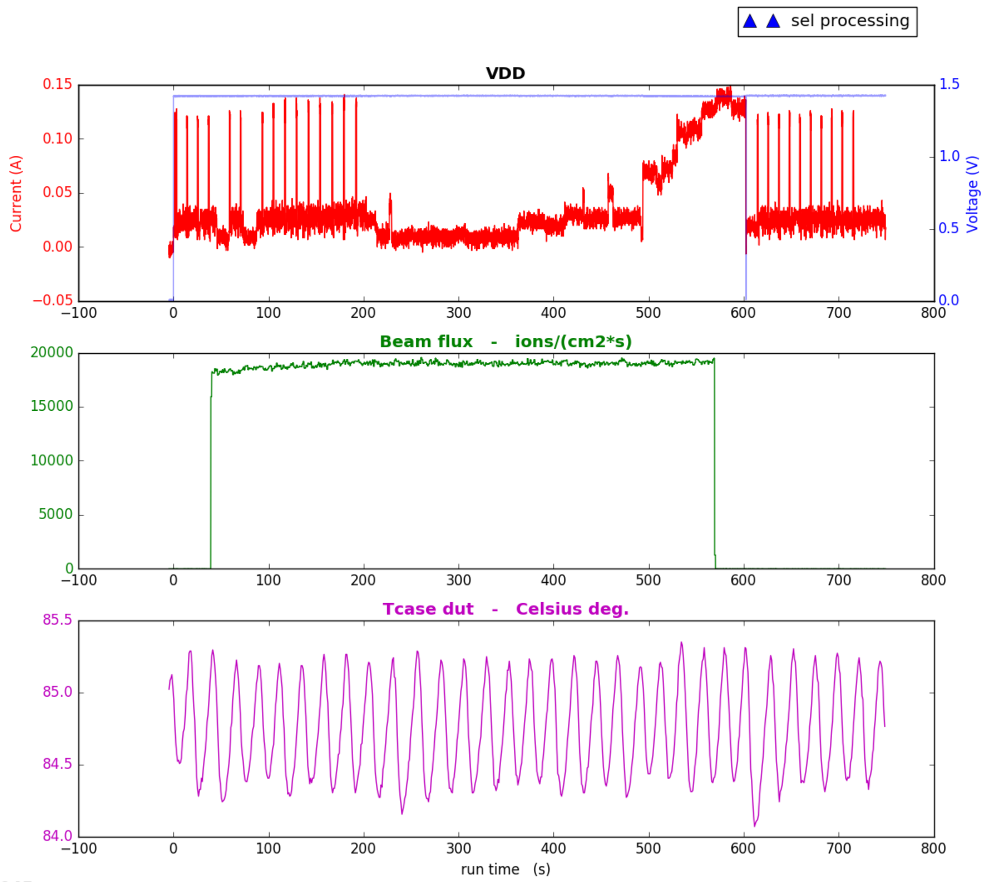



**Figure 13 – K4B4G0846Q, SEL test board 7, Low Speed, Run045 chronogram**

# 9 Glossary

**DUT**: Device under test.

**Fluence** (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.
In this document, Fluence is expressed in ions per cm².

**Flux**: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.
In this document, Flux is expressed in ions per cm².s.

**Single-Event Effect** (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.
Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL).

**Single Event Gate Rupture** (SEGR) **/ Single Event Dielectric Rupture (**SEDR**):** Destructive rupture of the gate oxide layer or dielectric layer by a single ion strike. This leads to leakage currents under bias and can be observed as stuck bits in digitals devices

**Single-Event Upset** (SEU)**:** A soft error caused by the transient signal induced by a single energetic particle strike.

**Single-Event Transient** (SET): A transient signal induced by a single energetic particle strike.

**Single-Event Latch-up** (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.
SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.
An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

**Single-Event Functional Interrupt** (SEFI): A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single-event burnout (SEB).
A SEFI is often associated with an upset in a control bit or register.

**Error cross-section**: the number of errors per unit fluence. For device error cross-section, the dimensions are cm² per device. For bit error cross-section, the dimensions are cm² per bit.

**Tilt angle**: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis

**Weibull fit:** $F(x) = A\,(1- \exp\{-[(x-x_0)/W]^s\})$ with:

x = effective LET in MeV/(mg/cm$^2$);
F(x) = SEE cross-section in cm$^2$;
A = limiting or plateau cross-section;
$x_0$ = onset parameter, such that F(x) = 0 for $x < x_0$;
W = width parameter;
s = a dimensionless exponent.

**Error bars:** error bars are computed using a confidence level of 95% and a beam flux uncertainty of +/-10% as recommended by Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100.

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