Single Event Effects

Proton Test Report	
Test type	Single-Event Upset, Single Event Latchup
Part Reference	H5TC4G83CFR
Tested function	DDR3L SDRAM
Chip manufacturer	Hynix
Test Facility	PIF, Paul Scherrer Institute (PSI), Villigen, Switzerland
Test Date	May 2018
Customer	ESA ESTEC

Esa Estec Purchase Order N° 4000112477/14/NL/HB dated December 4th, 2014

BCE 5524

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1 Introduction

This report presents results of SEE proton test campaign for the Hynix DDR3L SDRAM H5TC4G83CFR. 4 parts were used with 2 parts per test mode. The test campaign took place at PIF, Paul Scherrer Institute (PSI), Villigen, Switzerland in May 2018.
This test has been performed after the heavy ion test of the device which shows no SEL event with high LET (Xenon) ion. This is why SEL testing was not repeated during this proton test.

2 Applicable and Reference Documents

Applicable Documents

AD-1 Hynix H5TC4G83CFR 4Gb DDR3L SDRAM Datasheet, Rev. 1.4/ Oct. 2015

AD-2 H5TC4G83CFR physical analysis HRX/RCA/00106

Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

RD-2. Proton Irradiation Facility at the PROSCAN project of the Paul Scherrer Institute PIF facility at PSI, Ulrike Grossner, Wojtek Hajdas, Ken Egli, Roger Brun, and Reno Harboe-Sorensen, RADECS 2009.

3 Device Information

Device description

H5TC4G83CFR, DDR3L SDRAM

Manufacturer:	Hynix
Package:	78-Ball FBGA 7.5 x 11 mm
Marking:	SKhynix H5TC4G83CFR PBA 517A DWMG0900XH2
Date code	1517
Technology:	CMOS
Die dimensions:	5.2 x 6.5 mm

This 4Gb memory is composed of 1 die with 8 banks of 1024 rows by 65536 columns of 8 bits words.

Device and die identification

Figure 1: Package, top.

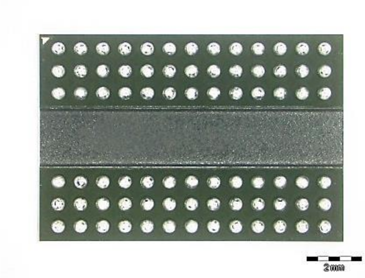

Figure 2: Package, bottom.

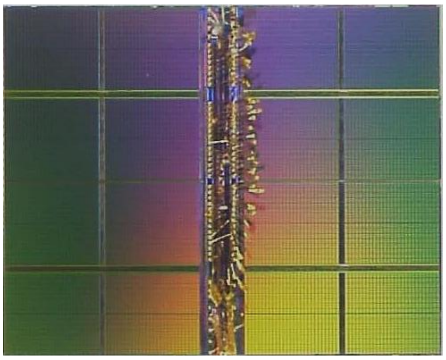

Figure 3: Die view.

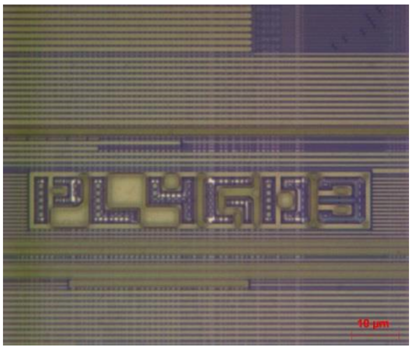

Figure 4: Die marking.

4 Test Setup

Figure 5 shows the principle of the single event test system.
The test system is based on a Kintex7 FPGA (Xilinx).
The test board includes 2 slots for high speed and low speed SODDIMM daughter boards on which is mounted one DUT memory.
The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 24 independent channels.
The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.
One DUT (low speed or high speed) is exposed at a time

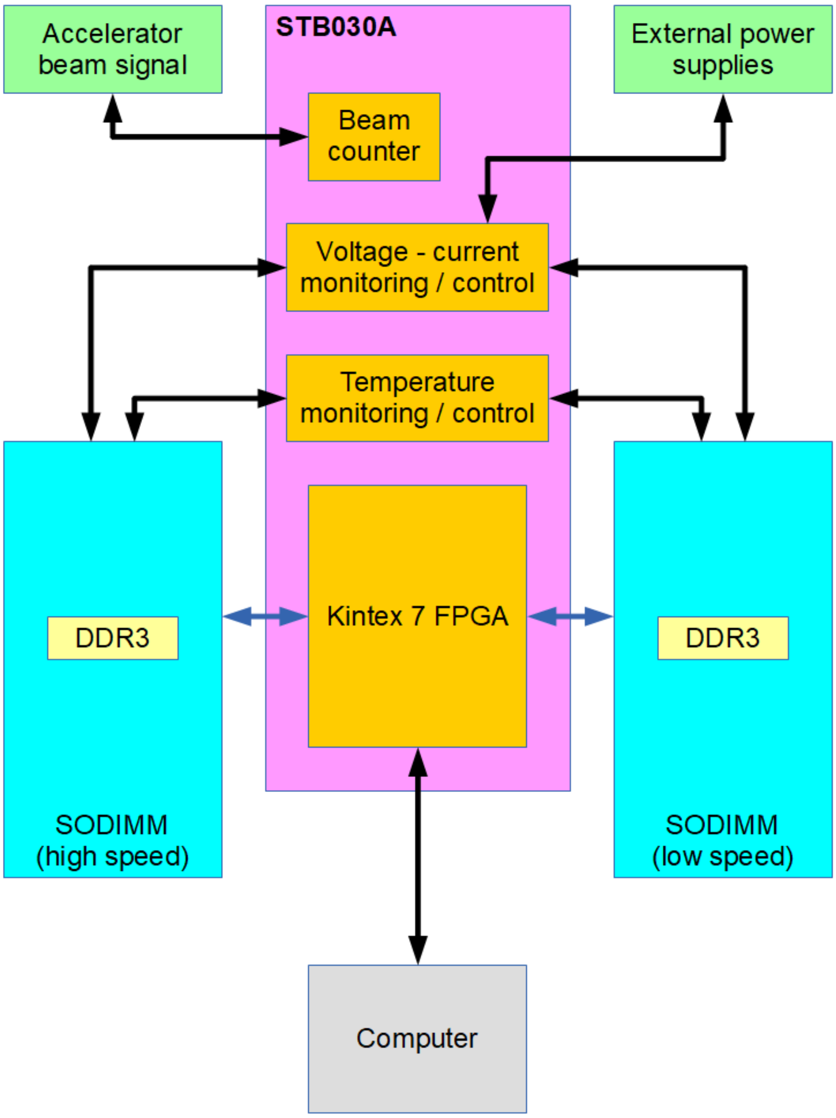

Figure 5: Hirex SEE test setup

5 Test sequence

Low speed mode is performed at a DUT clock frequency of 325MHz while high speed is performed at 700MHz.

Read/Write sequence

- Repeat cycles:
  - Write memory with 0x55 /0xAA
  - First Read memory (R1)
  - Second Read memory (R2)

6 PIF Test Facility

A description of PIF test facility can be found in RD-2. As shown in Figure 6, proton beam from COMET cyclotron is delivered to the experimental PIF cave with an input energy that can be varied from few MeVs up to 250 MeV. Then in PIF room, local copper degraders can be inserted into the beam to obtain the different user energies.

200 MeV input beam's energy was selected and calibrated. Figure 7 show an example of calibration together with the X and Y beam profiles.

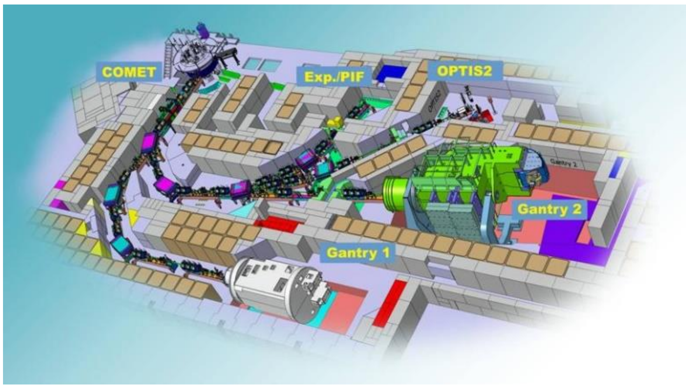

Figure 6 - Proscan facility

E0=200	Energy	Degr.	Plastic	IC-target	IC-degr	Target(1) Fac. 20nA	Degr(2) Fac. 20nA	Target(1) Fac. 200nA	Degr(2) Fac. 200nA	Target(1) Fac. 2 uA	Degr(2) Fac. 2 uA	5.0cm collimator PL6 10cm distance to DUT-Collimator	FLUX	IC-curent	IC-deg	PROSCAN	RPOSCAN MAX [nA]	FLUX(max) [p/cm/s]	IC-deg [nA]
	[MeV]	[mm]	[cnt/1s]	[cnt/1s]	[cnt/1s]	[p/cnt/cm2]	[p/cnt/cm2]						[p/cm/s]	[nA]	[nA]	[nA]			
Pos 1	**200**	**0.0**	154136	200	67	12844.7	38342.3						2.57E+06	2.00E+00	6.70E-01	1.50E-01	**1.00E+01**	**1.71E+08**	4.47E+01
1	**200**	**0.0**	169632	227	74	12454.6	38205.4												
	60mV		10	3	2.7	**1.26E+04**	**3.83E+04**	**1.26E+05**	**3.83E+05**	**1.26E+06**	**3.83E+06**								
Pos 1	**180.3**	**7.0**	163897	232	77	11774.2	35475.5						2.73E+06	2.32E+00	7.70E-01	1.50E-01	**1.00E+01**	**1.82E+08**	5.13E+01
1	**180.3**	**7.0**	173136	246	81	11730.1	35624.7												
	60mV		10	3	2.7	**1.18E+04**	**3.56E+04**	**1.18E+05**	**3.56E+05**	**1.18E+06**	**3.56E+06**								
Pos 1	**151.2**	**16.5**	131820	208	68	10562.5	32308.8						2.20E+06	2.08E+00	6.80E-01	1.50E-01	**1.00E+01**	**1.46E+08**	4.53E+01
1	**151.2**	**16.5**	151328	240	78	10508.9	32335.0												
	60mV		10	3	2.7	**1.05E+04**	**3.23E+04**	**1.05E+05**	**3.23E+05**	**1.05E+06**	**3.23E+06**								
Pos 1	**125.2**	**24.0**	132028	248	78	8872.8	28211.1						2.20E+06	2.48E+00	7.80E-01	1.50E-01	**1.00E+01**	**1.47E+08**	5.20E+01
1	**125.2**	**24.0**	126705	239	76	8835.8	27786.2												
	60mV		10	3	2.7	**8.85E+03**	**2.80E+04**	**8.85E+04**	**2.80E+05**	**8.85E+05**	**2.80E+06**								
Pos 1	**101.3**	**30.0**	129616	303	93	7129.6	23228.7						2.16E+06	3.03E+00	9.30E-01	1.50E-01	**1.00E+01**	**1.44E+08**	6.20E+01
1	**101.3**	**30.0**	115130	267	82	7186.6	23400.4												
	60mV		10	3	2.7	**7.16E+03**	**2.33E+04**	**7.16E+04**	**2.33E+05**	**7.16E+05**	**2.33E+06**								
Pos 1	**75.2**	**35.5**	100278	322	86	5190.4	19433.7						1.67E+06	3.22E+00	8.60E-01	1.50E-01	**1.00E+01**	**1.11E+08**	5.73E+01
1	**75.2**	**35.5**	103597	331	89	5216.4	19400.2												
	60mV		10	3	2.7	**5.20E+03**	**1.94E+04**	**5.20E+04**	**1.94E+05**	**5.20E+05**	**1.94E+06**								
Pos 1	**50.8**	**39.5**	75856	375	84	3371.4	15050.8						1.26E+06	3.75E+00	8.40E-01	1.50E-01	**1.00E+01**	**8.43E+07**	5.60E+01
1	**50.8**	**39.5**	69935	342	77	3408.1	15137.4												
	60mV		10	3	2.7	**3.39E+03**	**1.51E+04**	**3.39E+04**	**1.51E+05**	**3.39E+05**	**1.51E+06**								
Pos 1	**29.3**	**42.0**	42198	462	71	1522.3	9905.6						7.03E+05	4.62E+00	7.10E-01	1.50E-01	**1.00E+01**	**4.69E+07**	4.73E+01
1	**29.3**	**42.0**	41396	450	69	1533.2	9999.0												
	60mV		10	3	2.7	**1.53E+03**	**9.95E+03**	**1.53E+04**	**9.95E+04**	**1.53E+05**	**9.95E+05**								

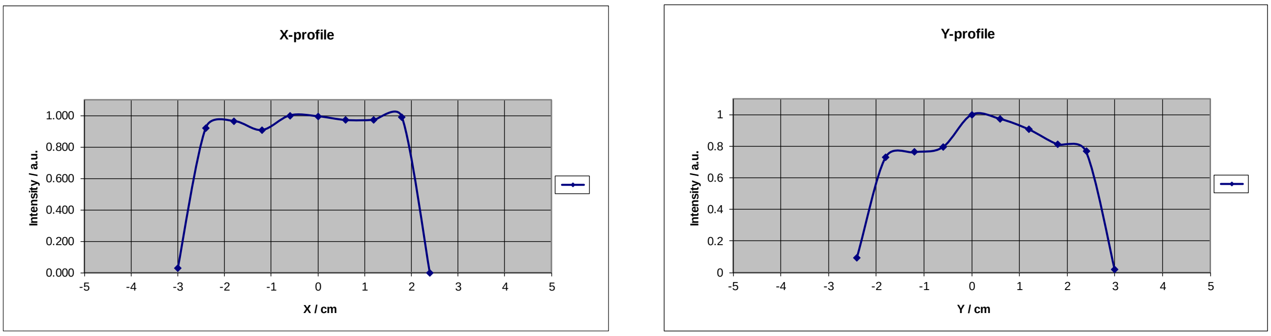

Figure 7 – 200MeV calibration results and beam profile

7 Test conditions.

SEU tests were carried out closed to Vddmin at 1.30V and room temperature.
Each memory present 8 banks of 65536 columns by 1024 rows of 8-bit words.
Each memory plane is traversed by bank, column, row which means that bank0, column0, row 0 to row 1023 is read, then bank0, column1, row 0 to row 1023, etc.
Read is done by burst which corresponds to 8 words. Each time at least 1 word is in error among the 8 words, the burst is recorded.

8 Detailed results

Runs results are summarized in Table 1.

Table 1: Detailed SEE results.

Facility	dut_medium	run_number	Facility_run_number	board_name	test_mode	Proton energy	run_duration	entered_fluence	row/column errors			address in error pre-exposure	address in error post-exposure	Comment	Column	Row	sefi	address in error during exposure	seu bit error cross-section /bit (*)	row/col error cross-section / device
									R1	R1R2	R2									
PIF	air	41	41	LS - H22	read write	200 MeV	482	1.00E+11	0	4	5	3	6		0	9	1	20	3.96E-20	9.00E-11
PIF	air	32	33	LS - H21	read write	200 MeV	785	9.70E+10	0	1	6	0	-		0	6	1	14	3.36E-20	6.19E-11
PIF	air	35	36	HS - H22	read write	200 MeV	496	1.00E+11	0	3	6	0	-	sefi at the end of the run	0	9	1	13	3.03E-20	9.00E-11
PIF	air	38	39	HS - H21	read write	200 MeV	489	1.00E+11	0	3	6	3	6		0	9	0	23	4.66E-20	9.00E-11
PIF	air	42	42	LS - H22	read write	100 MeV	916	5.00E+10	0	4	3	4	5		0	7	0	18	6.52E-20	1.40E-10
PIF	air	33	34	LS - H21	read write	100 MeV	779	4.42E+10	0	2	3	3	-		0	5	0	14	5.79E-20	1.13E-10
PIF	air	34	35	LS - H21	read write	100 MeV	912	5.00E+10	0	4	2	4	-	sefi at the end of the run	1	5	1	12	3.73E-20	1.20E-10
PIF	air	37	38	HS - H22	read write	100 MeV	927	5.00E+10	0	4	3	4	4		0	7	1	15	5.12E-20	1.40E-10
PIF	air	39	40	HS - H21	read write	100 MeV	958	5.00E+10	0	2	4	5	7		0	6	0	22	7.92E-20	1.20E-10

(*): for the computation of the cross section the address errors present at the beginning of exposure are subtracted. All address errors are single bit word errors.

For 200MeV and 100MeV protons with both high speed and low speed test modes, 3 types of errors have been recorded:

- Row/column errors are mostly row errors. These errors can consist of multi-bit word errors and are cleared at the next sequence iteration.
- Address errors: these errors can persist along the test sequence iterations and some of them can be present after beam exposure. All recorded address errors are single bit word error.
- SEFI: these large errors (multi bit word errors) are mainly columns errors and are persistent until a power reset is performed.

The fact that there is no first read error R1 not confirmed by the second read (R2) means that there are no or very few pure read errors.

9 Glossary

DUT: Device under test.

Fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.
In this document, Fluence is expressed in ions per cm^2.

Flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.
In this document, Flux is expressed in ions per cm^2.s.

Single-Event Effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.
Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL).

Single Event Gate Rupture (SEGR) **/ Single Event Dielectric Rupture (**SEDR**):** Destructive rupture of the gate oxide layer or dielectric layer by a single ion strike. This leads to leakage currents under bias and can be observed as stuck bits in digitals devices

Single-Event Upset (SEU)**:** A soft error caused by the transient signal induced by a single energetic particle strike.

Single-Event Transient (SET): A transient signal induced by a single energetic particle strike.

Single-Event Latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.
SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.
An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

Single-Event Functional Interrupt (SEFI): A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single-event burnout (SEB).
A SEFI is often associated with an upset in a control bit or register.

Error cross-section: the number of errors per unit fluence. For device error cross-section, the dimensions are cm^2 per device. For bit error cross-section, the dimensions are cm^2 per bit.

Tilt angle: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis

Weibull fit: $F(x) = A\ (1- \exp\{-[(x-x_0)/W]^s\})$ with:

> x = effective LET in MeV/(mg/cm^2);
> F(x) = SEE cross-section in cm^2;
> A = limiting or plateau cross-section;
> x_0 = onset parameter, such that F(x) = 0 for $x < x_0$;
> W = width parameter;
> s = a dimensionless exponent.

Error bars: error bars are computed using a confidence level of 95% and a beam flux uncertainty of +/-10% as recommended by Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100.