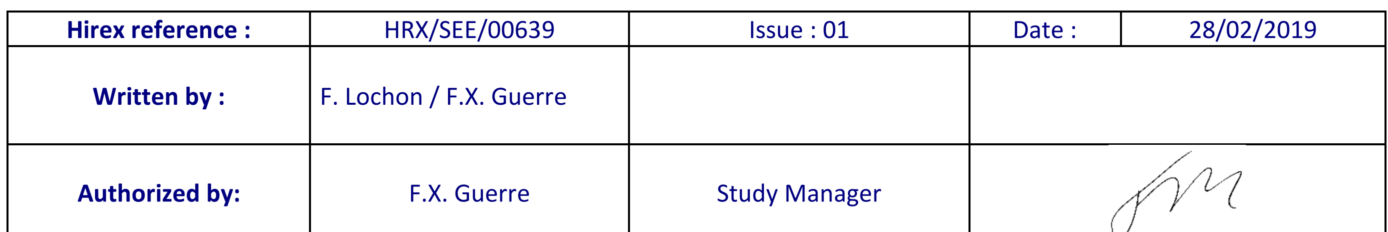
Single Event Effects

Heavy Ion Test Report

Test type	Single-Event Upset, Single Event Latchup, SEFI
Part Reference	MT41K512M8RH
Tested function	DDR3L SDRAM
Chip manufacturer	Micron
Test Facility	RADEF, University of Jyväskylä
Test Date	December 2017, January 2018, April 2018
Customer	ESA ESTEC

Esa Estec Purchase Order N° 4000112477/14/NL/HB dated December 4th, 2014

BCE 5524



Hirex reference :	HRX/SEE/00639	Issue : 01	Date :	28/02/2019
Written by :	F. Lochon / F.X. Guerre			
Authorized by:	F.X. Guerre	Study Manager		

DOCUMENTATION CHANGE NOTICE

Issue	Date	Page	Change Item	
01	28/02/2019		Original issue	

Contributors to this work

Frédéric Lochon — Hirex Engineering
Bendy Tanios — Hirex Engineering

TABLE OF CONTENTS

1 INTRODUCTION 4

2 APPLICABLE AND REFERENCE DOCUMENTS 4

Applicable Documents 4
Reference Documents 4

3 DEVICE INFORMATION 5

Device description 5
Device and die identification 5

4 SAMPLE PREPARATION 5

5 TEST SETUP 6

6 TEST SEQUENCES 7

Read/Write sequence 7
Read/Write with load registers sequence 7
Read/Write with DUT reset sequence 7

7 RADEF FACILITY 8

7.1 Test chamber 8
7.2 Beam quality control 8
7.3 Dosimetry 8
7.4 Used ions 8

8 TEST CONDITIONS. 9

9 DETAILED RESULTS 9

9.1 Read/write sequence 9
9.2 Read/Write with load registers or DUT reset sequences 12
Read/Write sequence including load registers steps 13
Read/Write sequence including DUT reset steps 15
9.3 SEL test runs 18

10 GLOSSARY 20

LIST OF TABLES

Table 1 - Ion beam setting 8
Table 2: Detailed SEE results. 9
Table 3 Cumulated logic errors per ion 11
Table 4 – Runs table for Read/write with load registers or DUT reset sequences 12
Table 5 – Runs table for SEL test runs 18

LIST OF FIGURES

Figure 1: Package, top. 5
Figure 2: Package, bottom. 5
Figure 3: Die view. 5
Figure 4: Die marking. 5
Figure 5: Hirex SEE test setup 6
Figure 6 – MT41K512M8RH, High Speed and Low Speed Read Write, SEU bit error cross-section / bit 10
Figure 7 – Cumulated Logic error cross-section plot 11
Figure 8 – Run chronograms for read/write with load registers sequence 14
Figure 9 – Run chronograms for read/write with DUT reset sequence 17
Figure 10 – MT41K512M8RH, SEL test board 3, Low Speed, Run042 chronogram 18
Figure 11 – MT41K512M8RH, SEL test board 4, Low Speed, Run043 chronogram 19

1 Introduction

This report presents results of SEE heavy ion test campaigns for the Micron DDR3L SDRAM MT41K512M8RH. 4 parts were used with 2 parts per test mode, high speed and low speed. The test campaign took place at RADEF, University of in December 2017, January 2018 and April 2018.

2 Applicable and Reference Documents

Applicable Documents

AD-1 Micron MT41K512M8RH 4Gb DDR3L SDRAM Datasheet 4Gb_DDR3L_2133.pdf - Rev. L 9/14 EN

AD-2 MT41K512M8RH physical analysis HRX/RCA/00104

Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

3 Device Information

Device description

MT41K512M8RH, DDR3L SDRAM

Manufacturer:	Micron
Package:	78-Ball FBGA 9 x 10.5 mm
Marking:	5AE77 D9QBJ logo JJQZ, xxxJ6VQ, xxxJGK4
Date code	1502
Technology:	CMOS
Die dimensions:	8.1 x 8.7 mm

This 4Gb memory is composed of 1 die with 8 banks of 1024 rows by 65536 columns of 8 bits words.

Device and die identification

Figure 1: Package, top.

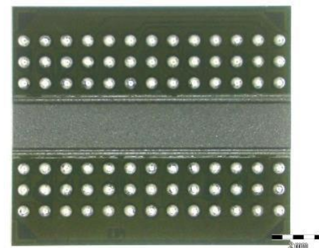


Figure 2: Package, bottom.

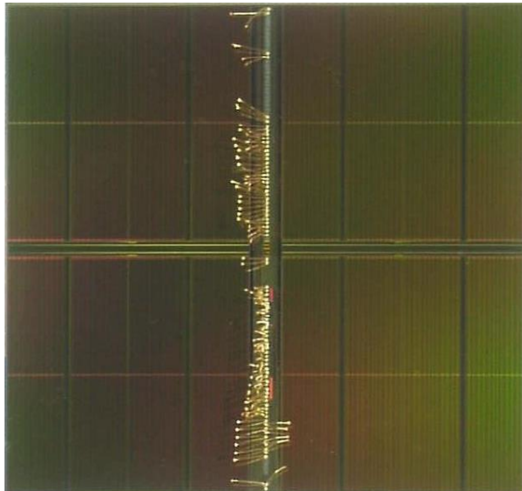


Figure 3: Die view.

Figure 4: Die marking.

4 Sample preparation

Each DUT has been prepared by die back thinning down to a die thickness lower or equal to 50 microns.

5 Test Setup

Figure 5 shows the principle of the single event test system.
The test system is based on a Kintex7 FPGA (Xilinx).
The test board includes 2 slots for high speed and low speed SODDIMM daughter boards on which is mounted one DUT memory.
The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 24 independent channels.
The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.
One DUT (low speed or high speed) is exposed at a time

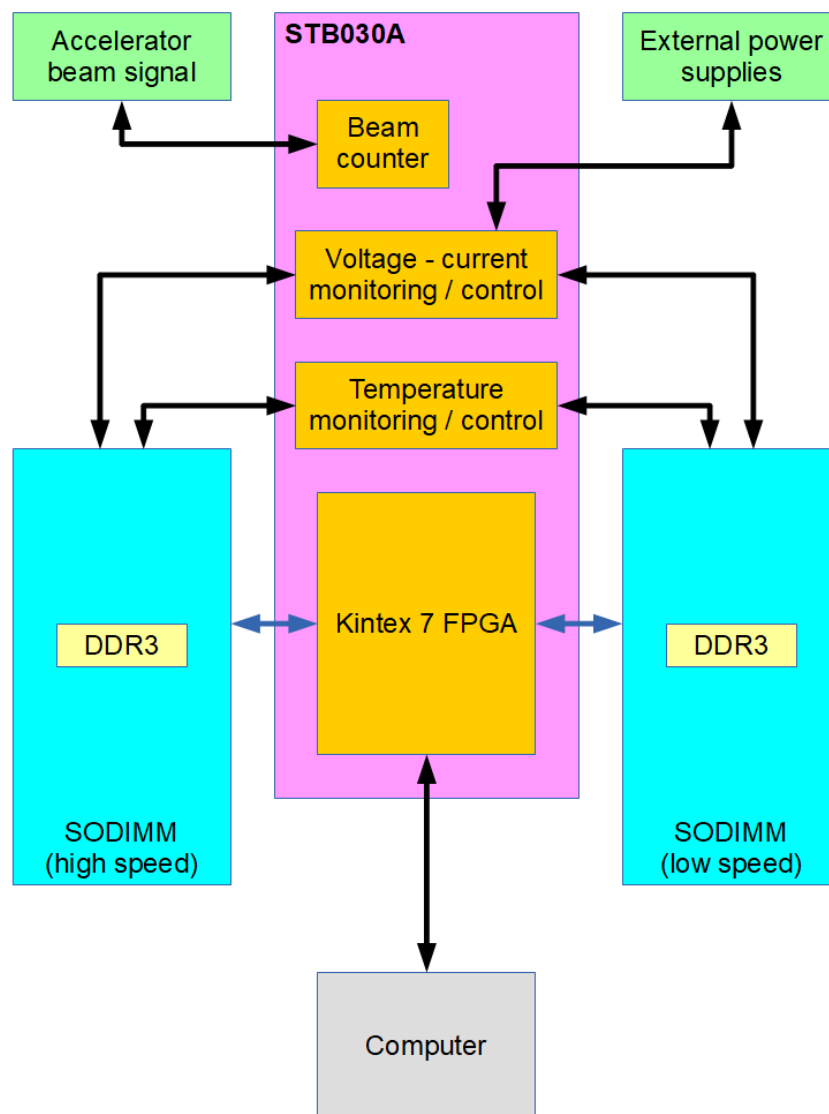


Figure 5: Hirex SEE test setup

6 Test sequences

Low speed mode is performed at a DUT clock frequency of 325MHz while high speed is performed at 700MHz. Refresh time is set to 6.8µs.

Read/Write sequence

- Repeat cycles:
  - Write memory with 0x55 /0xAA
  - Wait 1s
  - First Read memory (R1)
  - Second Read memory (R2)

Before the test campaigns, the following has been checked:

- Write the entire memory
- Then repeat cycles
  - Load register step or a Reset DDR3
  - Read memory

No error could be detected

That is why the basic Read/Write sequence have been modified to create 2 new test sequences.

Read/Write with load registers sequence

- Repeat cycles:
  - Load MRS
  - Wait 0.1s
  - Write memory with 0x55 /0xAA
  - Wait 0.5s
  - Load MRS
  - Wait 0.1s
  - First Read memory (R1)
  - Second Read memory (R2)

Read/Write with DUT reset sequence

- Repeat cycles:
  - Reset DDR3
  - Wait 0.1s
  - Write memory with 0x55 /0xAA
  - Wait 0.5s
  - Reset DDR3
  - Wait 0.1s
  - First Read memory (R1)
  - Second Read memory (R2)

The two functions Load MRS and Reset DDR3 are detailed here below

Load MRS
re-program mode registers MR0-MR3 of the DDR3 memory via MRS command

Reset DDR3
used to clear all state information in the DDR3 memory device.
The reset sequence as preconized by devices datasheets and JEDEC standard No. 79-3F is the following:

1- Physical reset (Warm reset) using DDR3 RESET# pin
2- Load mode registers via MRS command
3- ZQ Calibration used to calibrate the DDR3 memory output drivers and ODT (On-Die Termination) values via ZQCL command

7 RADEF facility

The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.
The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula,

$$130\ Q^2/M,$$

where Q is the ion charge state and M is the mass in Atomic Mass Units.

7.1 Test chamber

Irradiation of components is performed in a vacuum chamber with an inside diameter of 75 cm and a height of 81 cm.
The vacuum in the chamber is achieved after 15 minutes of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the X, Y and Z directions. The possibility of rotation around the Y-axis is provided by a round table. The free movement area reserved for the components is 25 cm x 25 cm, which allows one to perform several consecutive irradiations for several different components without breaking the vacuum.
The assembly is equipped with a standard mounting fixture. The adapters required to accommodate the special board configurations and the vacuum feed-throughs can also be made in the laboratory’s workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components.
A CCD camera with a magnifying telescope is located at the other end of the beam line to determine accurate positioning of the components. The coordinates are stored in the computer’s memory allowing fast positioning of various targets during the test.

7.2 Beam quality control

For measuring beam uniformity at low intensity, a CsI(Tl) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis.
A set of four collimated PIN-CsI(Tl) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.
Two beam wobblers and/or a 0.5 microns diffusion Gold foil can be used to achieve good beam homogeneity. The foil is placed 3 m in front of the chamber. The wobbler-coils vibrate the beam horizontally and vertically, the proper sweeping area being attained with the adjustable coil-currents.

7.3 Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI(Tl) detectors. Three collimators of different size and shape are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.
At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(Tl) detectors.

7.4 Used ions

Ion	LET^{SRIM} at surface [$MeV.cm^2.mg^{-1}$]	Range [µm]	Beam energy [MeV]
$^{15}N^{4+}$	1.83	202	139
$^{20}Ne^{6+}$	3.63	146	186
$^{40}Ar^{12+}$	10.2	118	372
$^{56}Fe^{15+}$	18.5	97	523
$^{82}Kr^{22+}$	32.1	94	768
$^{131}Xe^{35+}$	60.0	89	1217

SRIM-2003.26

Table 1 - Ion beam setting

8 Test conditions.

SEU tests were carried out closed to Vddmin at 1.30V and room temperature (1.35V and room temperature during January and April 2018 campaigns).

Each memory present 8 banks of 65536 columns by 1024 rows of 8-bit words.

Each memory plane is traversed by bank, column, row which means that bank0, column0, row 0 to row 1023 is read, then bank0, column1, row 0 to row 1023, etc.

Read is done by burst which corresponds to 8 words. Each time at least 1 word is in error among the 8 words, the burst is recorded.

9 Detailed results

9.1 Read/write sequence

Results are summarized in Table 2.

Test campaign	Facility	dut_medium	run_number	Facility_run_number	board_id	power_config	bias_config	test_mode	Ion	tilt	LET	run_duration	capacity	entered_fluence	eff. Fluence	pre	R1	R1R2	R2	persistent	total cell errors	Cell errors cross -section / bit	col	row	LE	LE2	sefi	total logic errors	logic errors cross-section / device	post
W017	RADEF	vacuum	19	18	3	1.3	HS	read write	N	0	1.83	267	4.29E+09	2.00E+06	2.00E+06	0	0	0	0	0	0		0	0	0	0	0	0		0
W017	RADEF	vacuum	20	19+20	3	1.3	HS	read write	Ar	0	10.2	2206	4.29E+09	4.64E+05	4.64E+05	0	0	0	2	0	2	1.00E-15	7	34	0	0	2	43	9.27E-05	1
W017	RADEF	vacuum	21	21	3	1.3	HS	read write	Fe	0	18.5	413	4.29E+09	2.00E+05	2.00E+05	0	0	4	3	0	7	8.15E-15	2	36	1	0	2	41	2.05E-04	0
W017	RADEF	vacuum	18	17	3	1.3	HS	read write	Kr	0	32.2	356	4.29E+09	2.00E+05	2.00E+05	0	38	274	496	1	809	9.42E-13	6	40	2	0	2	50	2.50E-04	0
W050	RADEF	vacuum	5	31	4	1.3	HS	read write	N	0	1.83	334	4.29E+09	2.00E+06	2.00E+06	0	0	0	0	0	0		0	0	0	0	0	0		0
W050	RADEF	vacuum	12	38	4	1.3	HS	read write	Ar	0	10.2	846	4.29E+09	1.00E+05	1.00E+05	0	0	0	0	0	0		1	7	0	0	0	8	8.00E-05	0
W050	RADEF	vacuum	43	67	4	1.3	HS	read write	Fe	0	18.5	441	4.29E+09	2.00E+05	2.00E+05	0	0	4	3	0	7	8.15E-15	5	37	0	0	1	43	2.15E-04	0
W050	RADEF	vacuum	44	68	4	1.3	HS	read write	Kr	0	32.2	387	4.29E+09	2.00E+05	2.00E+05	0	39	309	299	0	647	7.53E-13	4	31	2	0	1	38	1.90E-04	0
W050	RADEF	vacuum	58	81	4	1.35	hs	read write	Xe	0	60	2235	4.29E+09	5.00E+05	5.00E+05	1374	106	3650	4778	3404	10564	4.92E-12	20	139		3	5	167	3.34E-04	524
W050	RADEF	vacuum	57	80	6	1.35	hs	read write	Xe	0	60	2014	4.29E+09	5.07E+05	5.07E+05	459	191	3631	4209	2447	10019	4.60E-12	28	106				134	2.64E-04	647
W050	RADEF	vacuum	28	54	3	1.3	LS	read write	N	0	1.83	289	4.29E+09	2.00E+06	2.00E+06	0	0	0	0	0	0		0	0	0	0	0	0		0
W050	RADEF	vacuum	27	53	3	1.3	LS	read write	Ar	0	10.2	784	4.29E+09	1.00E+05	1.00E+05	0	0	0	0	0	0		0	10	0	0	1	11	1.10E-04	0
W050	RADEF	vacuum	4	30	3	1.3	LS	read write	Ar	0	10.2	645	4.29E+09	1.00E+05	1.00E+05	0	0	0	0	0	0		2	10	0	0	0	12	1.20E-04	0
W050	RADEF	vacuum	13	39	3	1.3	LS	read write	Fe	0	18.5	424	4.29E+09	2.00E+05	2.00E+05	0	0	10	10	2	22	2.56E-14	3	31	0	0	1	35	1.75E-04	0
W050	RADEF	vacuum	14	40	3	1.3	LS	read write	Kr	0	32.2	348	4.29E+09	2.00E+05	1.00E+05	0	1	191	258	2	452	1.05E-12	5	15	0	0	1	21	2.10E-04	0
W050	RADEF	vacuum	26	52	4	1.3	LS	read write	N	0	1.83	232	4.29E+09	2.00E+06	2.00E+06	0	0	0	0	0	0		0	0	0	0	0	0		0
W050	RADEF	vacuum	29	55	4	1.3	LS	read write	Ar	0	10.2	676	4.29E+09	5.49E+05	2.00E+05	0	0	0	0	0	0		5	7	0	0	1	13	6.50E-05	
W050	RADEF	vacuum	42	66	4	1.3	LS	read write	Fe	0	18.5	426	4.29E+09	2.00E+05	2.00E+05	0	0	2	7	0	9	1.05E-14	2	35	0	0	0	37	1.85E-04	0
W050	RADEF	vacuum	45	69	4	1.3	LS	read write	Kr	0	32.2	348	4.29E+09	2.00E+05	1.00E+05	0	411	155	217	50	833	1.94E-12	4	22	1	0	2	29	2.90E-04	0
W050	RADEF	vacuum	56	79	4	1.35	ls	read write	Xe	0	60	858	4.29E+09	2.00E+05	2.00E+05	1878	191	1273	1519	1392	2497	2.91E-12	6	42				48	2.40E-04	303
W050	RADEF	vacuum	59	82	6	1.35	ls	read write	Xe	0	60	2354	4.29E+09	5.00E+05	5.00E+05	767	491	3678	5728	1984	11114	5.18E-12	33	123				156	3.12E-04	31

Table 2: Detailed SEE results.

<u>Pre-run errors</u>

Stuck bits present before exposure. They could have been created during previous runs on the DUT.

<u>R1 bit errors</u>

Number of errors detected during READ1 but not during READ2. These errors which represent reading errors are very few and affect only a limited number of READ1 steps.

<u>R1/R2 bit errors</u>

Number of errors detected during READ1 and during READ2. These errors represent SEU WRITE bit errors or SEU cells errors occurring during the time the cell is not written (as for instance during WAIT step but not only).

<u>R2 bit errors</u>

Number of errors detected during READ2 only: These errors represent reading errors which are expected to be quite few as for R1 bit errors and the SEU cells errors occurring during the time the cell is not read.

<u>Persistent bit errors</u>

Bit errors that last more than one sequence iteration. Part of these errors can persist up to the end of the run and are then counted as post-run bit errors (stuck bits). Pre-run errors have been subtracted from the persistent bit error count.

<u>Colum error</u>

Likely an error in the logic. A column error can affect two banks at a time.

<u>Row errors</u>

Likely an error in the logic. Consist in a portion of row in error in a bank.

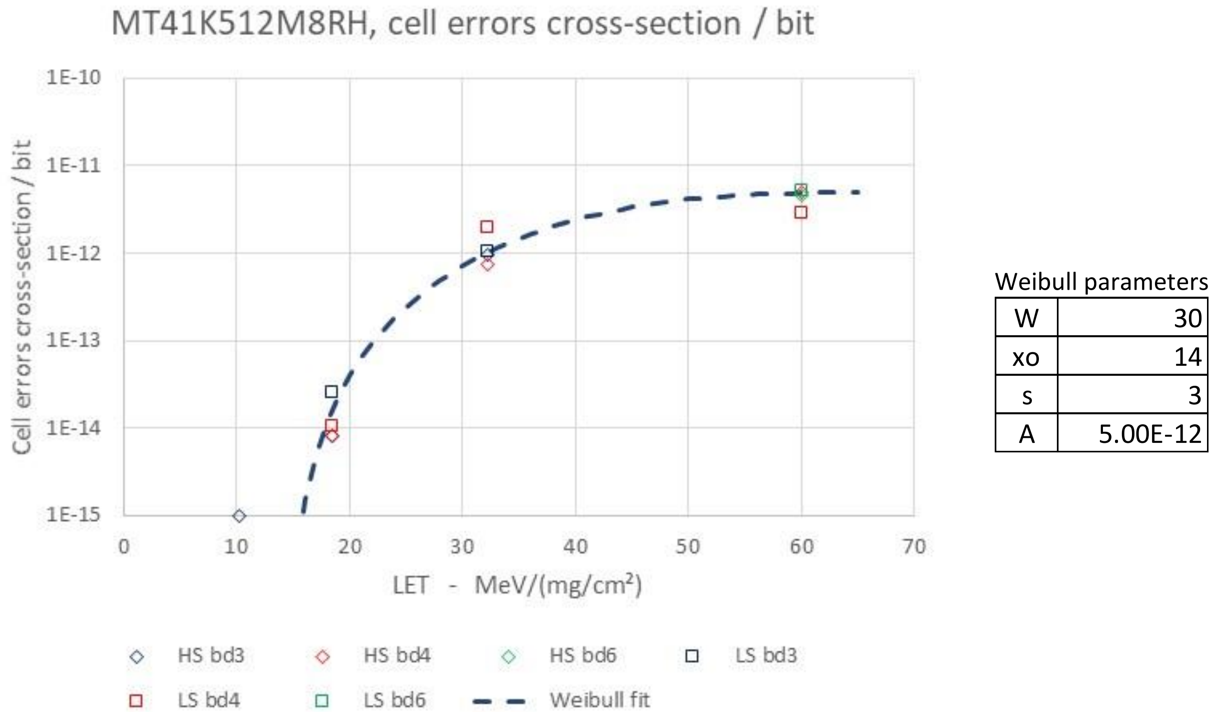
<u>SEFI</u>

These errors consist mainly in column errors that persist during several sequence iterations. Most of them induce a count clamped to the limit set at 50000. Only a few involved only a single column. The vast majority have been cured by a manual power reset. Some have disappeared under exposure without any external action.

<u>Post-run bit errors</u>

The errors are stuck bits. All affected words are single bit upset.

Figure 6 shows the SEU bit error cross-section for the 2 test modes, low speed and high speed. Test with Xenon was performed with a DUT bias of 1.35V while the tests with the other ions were performed at 1.30V.
No significant difference is observed between the two test modes.
With Argon only two R2 errors have been counted while no cell error was detected for all the other runs which explained why the LET threshold was taken to 14 MeV/(mg/cm²) for the Weibull plot.



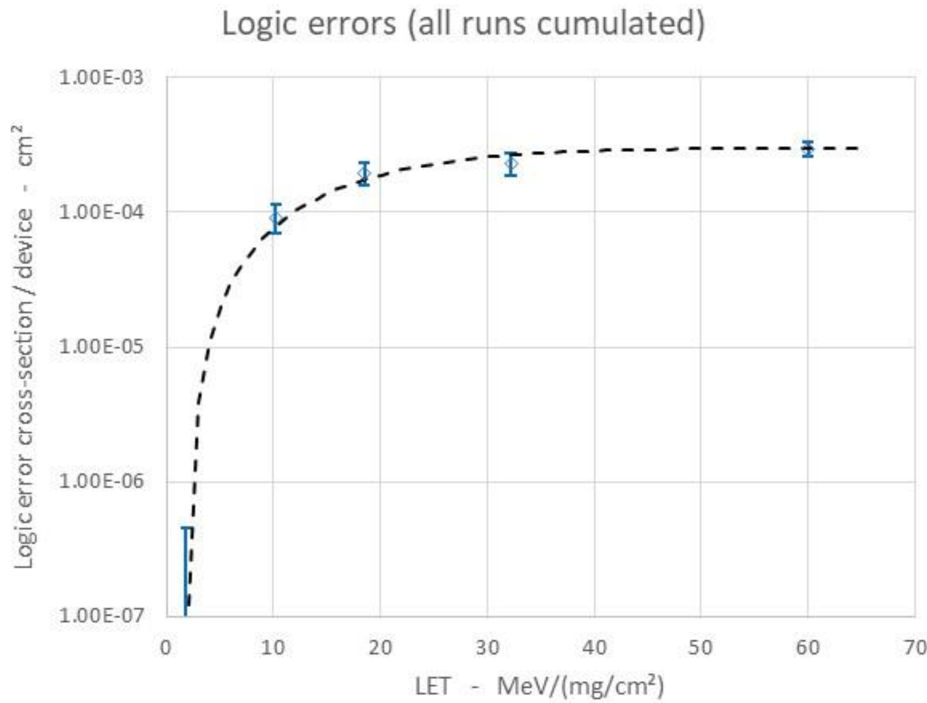
W	30
xo	14
s	3
A	5.00E-12

Figure 6 – MT41K512M8RH, High Speed and Low Speed Read Write, SEU bit error cross-section / bit

For the logic errors, column, row and SEFI, all runs have been cumulated for each ion as shown in Table 3. The corresponding Logic error cross-section is plot in Figure 7.

Ion	LET	Total fluence	total errors	Logic errors cross-section / device
Ar	10.2	9.64E+05	87	9.02E-05
Fe	18.5	8.00E+05	156	1.95E-04
Kr	32.2	6.00E+05	138	2.30E-04
N	1.83	8.00E+06	0	1.00E-08
Xe	60	1.71E+06	505	2.96E-04

Table 3 Cumulated logic errors per ion



Weibull parameters

W	18
xo	2
s	1.5
A	3.00E-04

Figure 7 – Cumulated Logic error cross-section plot

For the stuck bit errors, only stuck bits have been counted with Xenon with an associated mean cross-section of 8 8 10-04 cm2.

9.2 Read/Write with load registers or DUT reset sequences

Purpose of these sequences was to evaluate the addition in the read/write sequence of steps for either reloading the DUT register content or doing a DUT reset, in SEFI occurrence.
No power reset was performed during these runs to clear SEFI if any.
The corresponding table of runs is shown in Table 4.

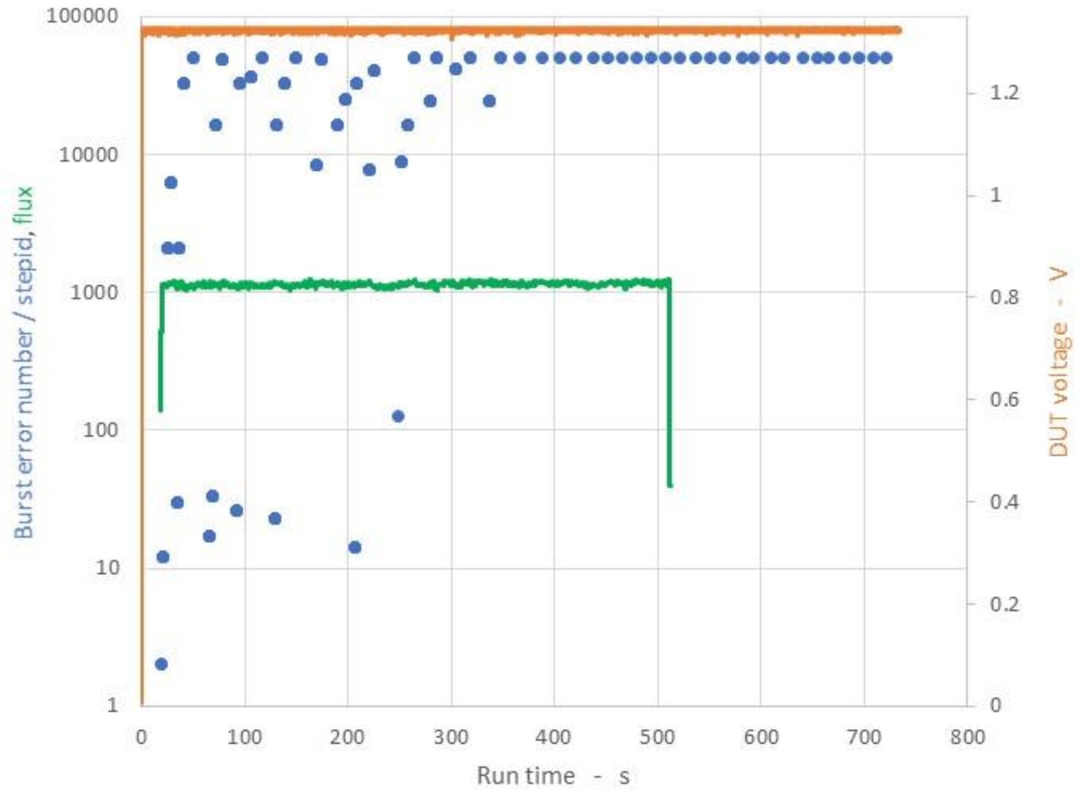
The run chronograms are shown in Figure 8 and Figure 9.

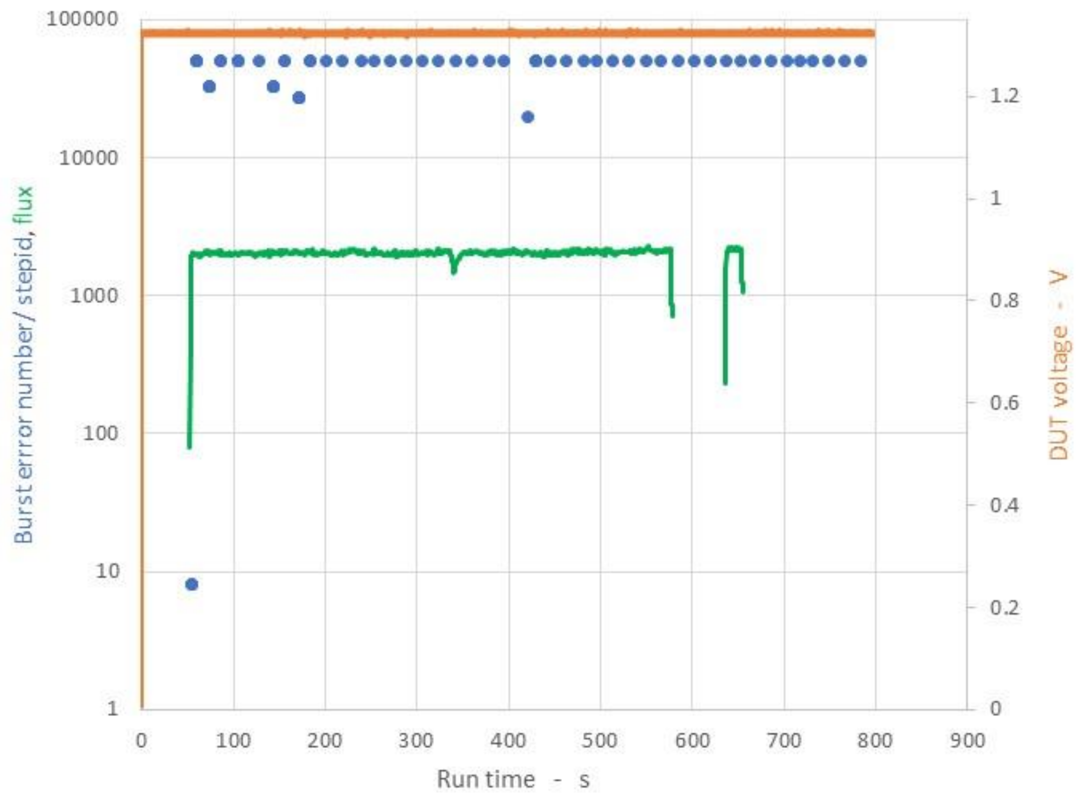
Test capaign	Facility	dut_ediu	run_nuber	Facility_run_nuber	board_id	bias_config	power_config	test_ode	teperature	Ion	tilt	run_duration	entered_fluence
2018 W06	RADEF	vacuu	9	46	4	HS	1.35	load rs	room	Kr	0	492	5.64E+05
2018 W06	RADEF	vacuu	11	47	4	HS	1.35	reset ddr3	room	Kr	0	827	1.19E+06
2018 W06	RADEF	vacuu	12	48	4	HS	1.35	reset ddr3	room	Kr	0	1157	2.00E+06
2018 W06	RADEF	vacuu	13	49	3	LS	1.35	load rs	room	Kr	0	601	1.11E+06
2018 W06	RADEF	vacuu	14	50	3	LS	1.35	reset ddr3	room	Kr	0	943	2.00E+06
2018 W06	RADEF	vacuu	16	51	4	LS	1.35	load rs	room	Kr	0	448	1.08E+06
2018 W06	RADEF	vacuu	18	52	4	LS	1.35	reset ddr3	room	Kr	0	785	2.00E+06

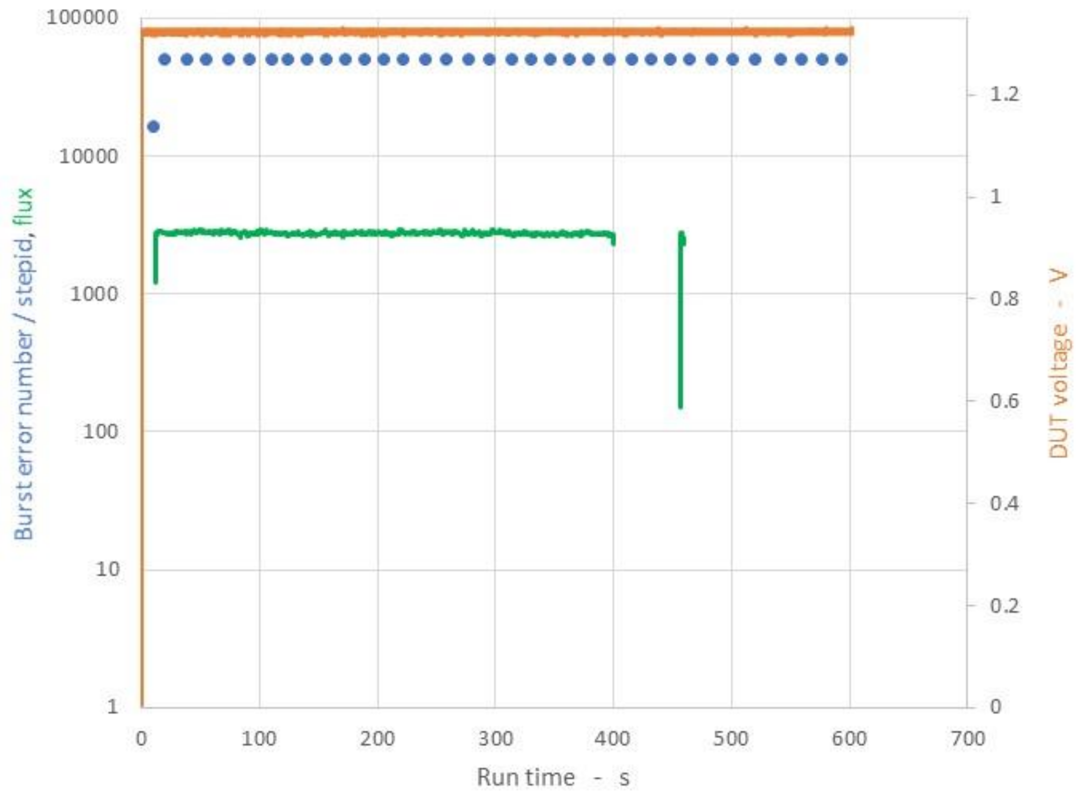
Table 4 – Runs table for Read/write with load registers or DUT reset sequences

Unfortunately, because of a high flux many stepids are clamped to the limit (50000) whatever a SEFI or a Large Ereror (LE) that lasts only one sequence iteration.
However, one can observed that with the load mrs sequence, clamped stepids values are still present even when beam is halted. This demonstrates that loading the memory registers is not sufficient to heal potential SEFIs.
On the other hand, with the reset ddr3 sequence, as soon as the beam is lowered or halted the number of burst errors per stepid decreases or goes down to the persistent error number which militates in favour of a good action of this sequence towards the SEFI curing

Read/Write sequence including load registers steps







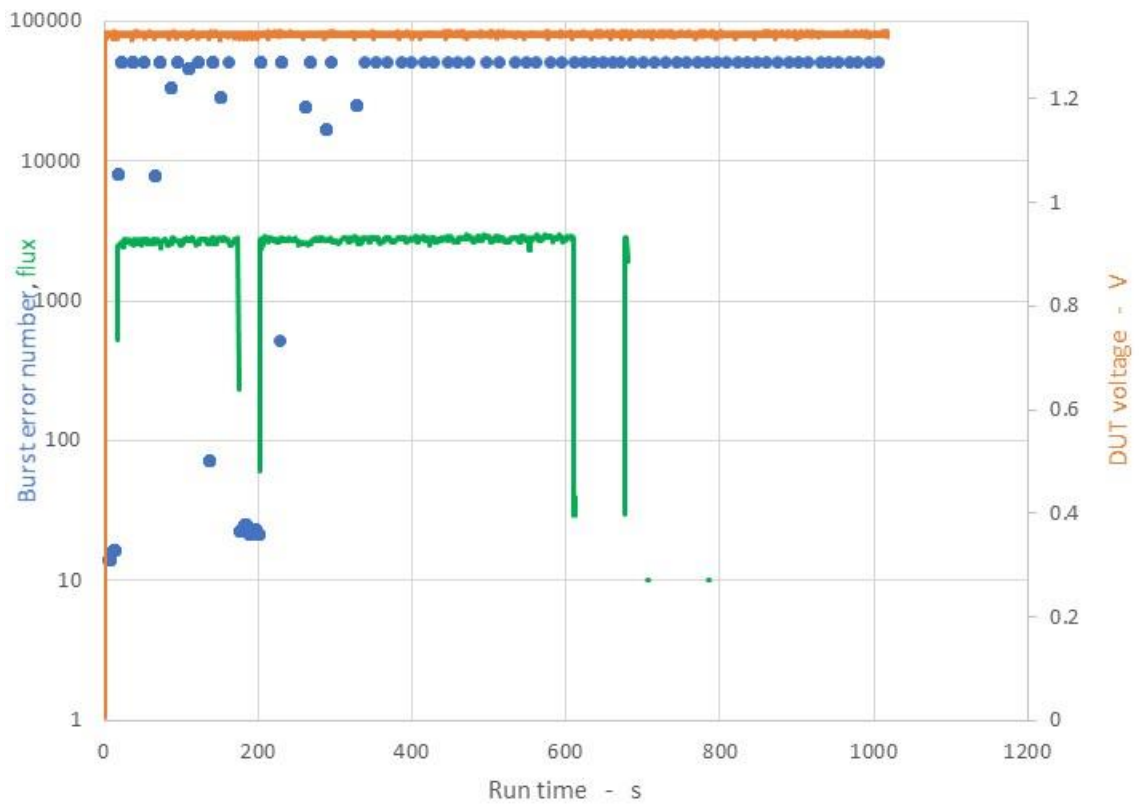
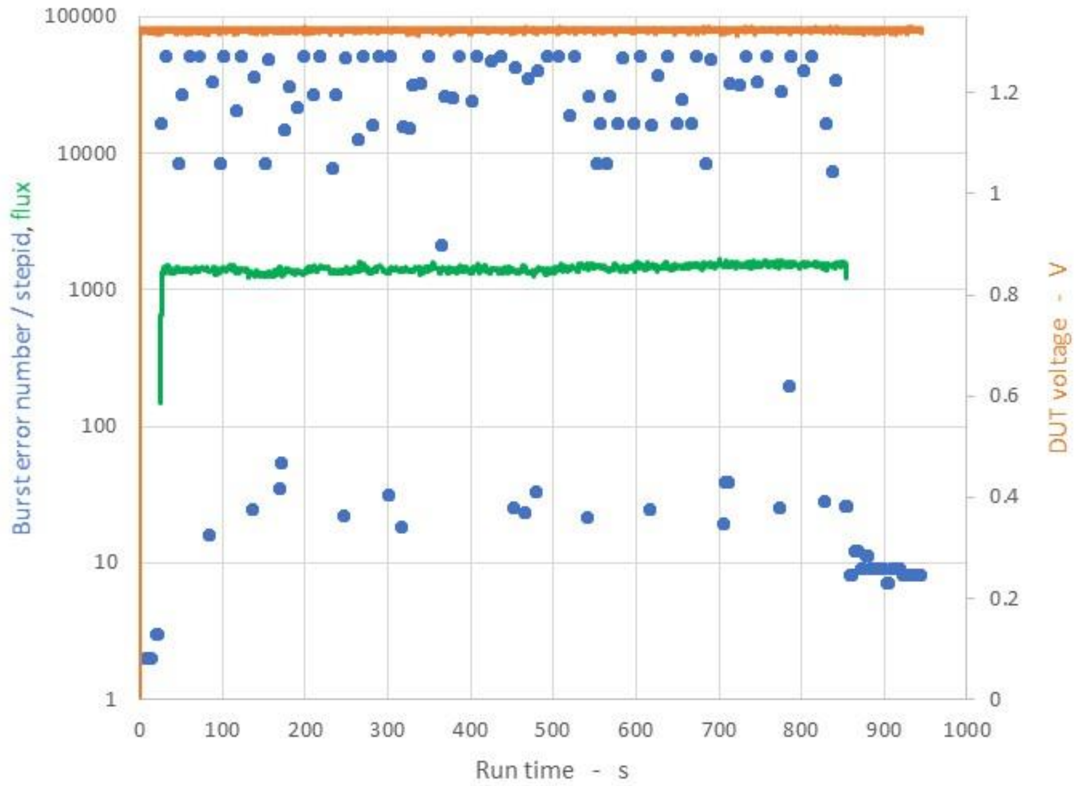
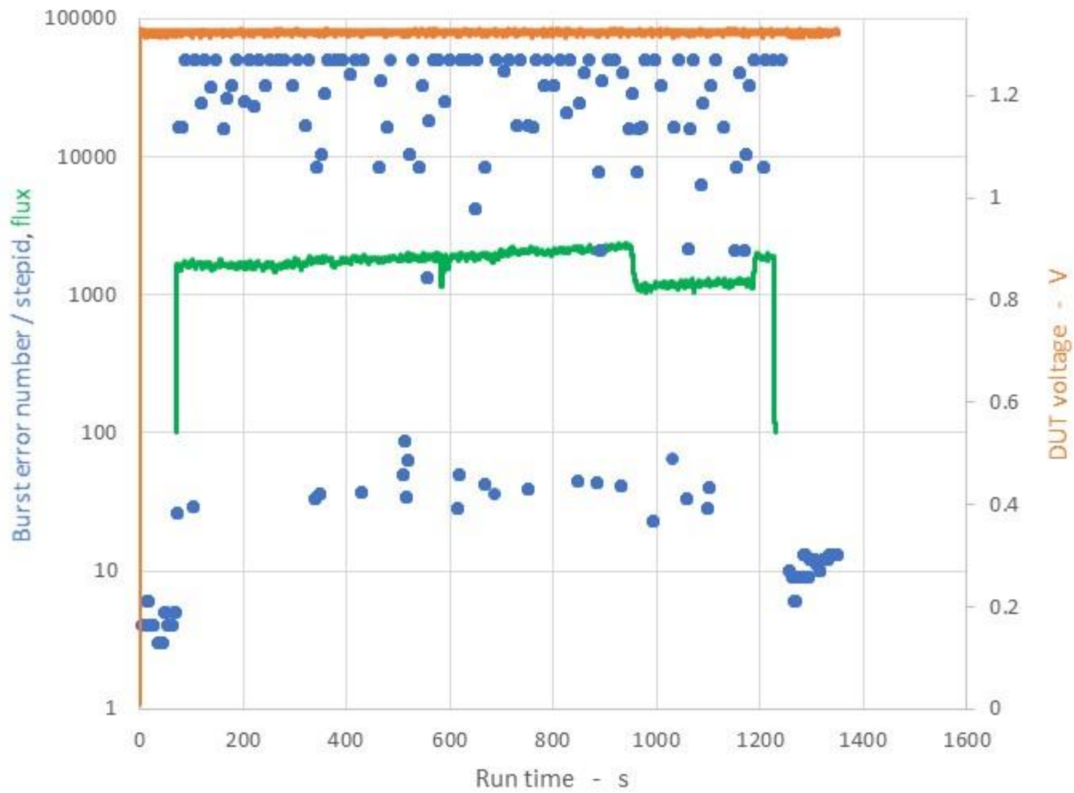
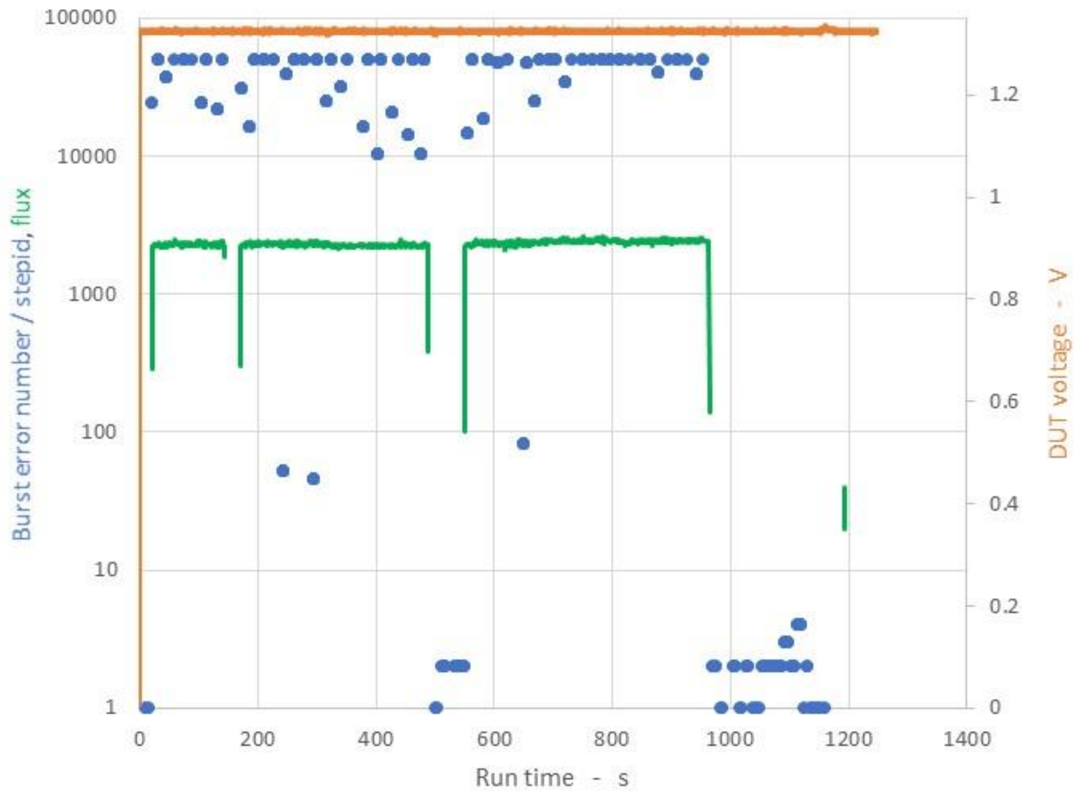


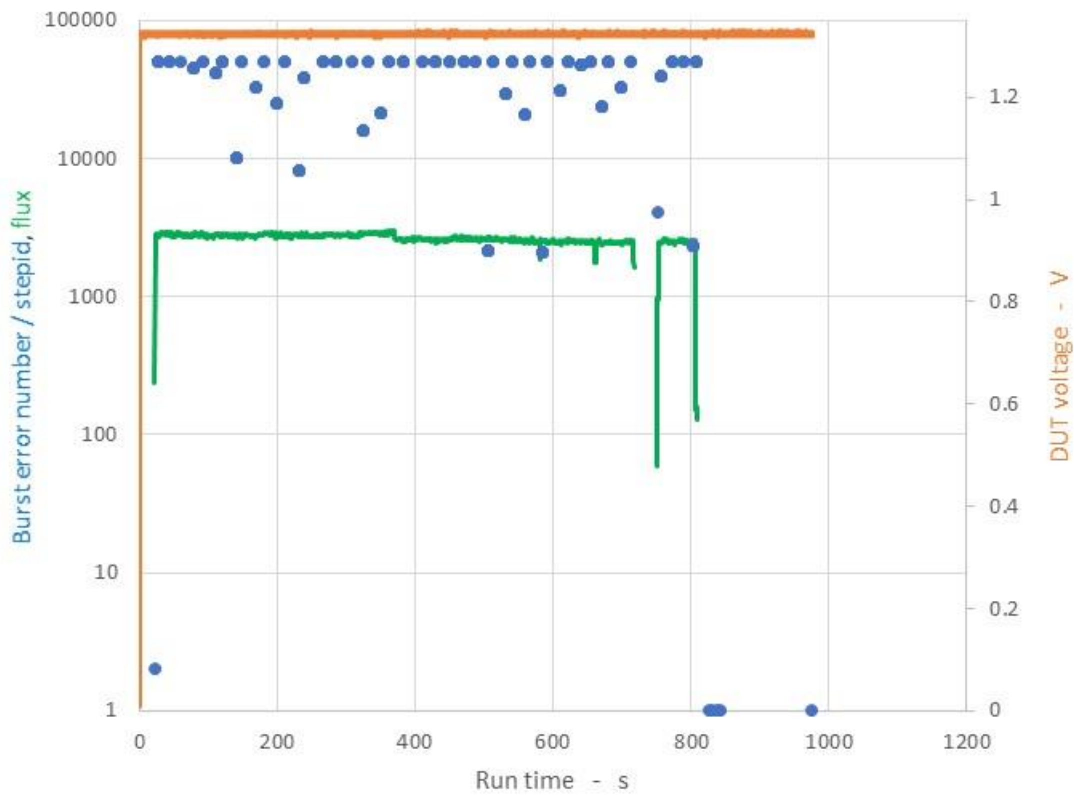
Figure 8 – Run chronograms for read/write with load registers sequence

Read/Write sequence including DUT reset steps






Run014 LS bd3 reset ddr3
Burst error number / stepid, flux
DUT voltage - V
Run time - s
100000
10000
1000
100
10
1
0
200
400
600
800
1000
1200
1400
1.2
1
0.8
0.6
0.4
0.2
0


Run018 LS bd4 reset ddr3
Burst error number / stepid, flux
DUT voltage - V
Run time - s
100000
10000
1000
100
10
1
0
200
400
600
800
1000
1200
1.2
1
0.8
0.6
0.4
0.2
0

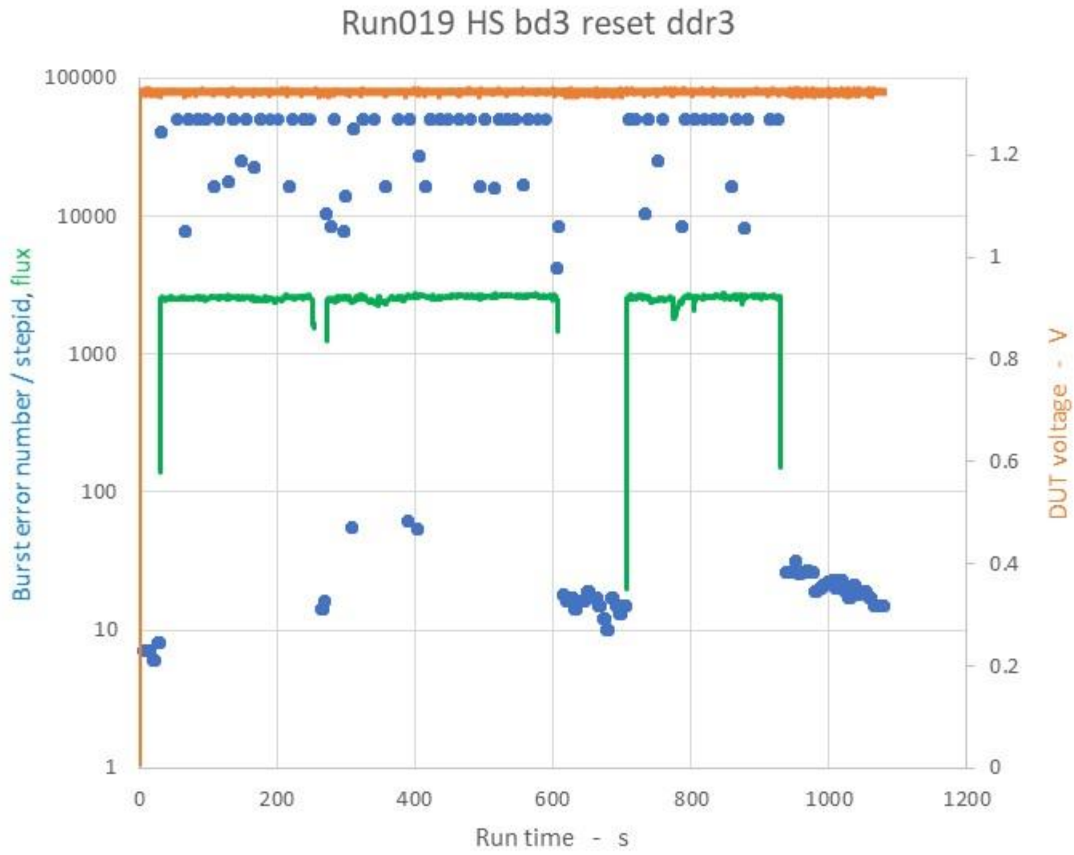


Figure 9 – Run chronograms for read/write with DUT reset sequence

9.3 SEL test runs

During test campaign 2018 W06, 2 runs have been performed with Xenon at 1.45V and a temperature of 85°C.
During SEL testing, read/write sequence was executed with a very low clamp limit for each stepid.
No SEL has been observed on the 2 samples.
Table 5 list the SEL runs performed.

Test campaign	Facility	dut_medium	run_number	Facility_run_number	board_id	bias_config	power_config	test_mode	temperature	Ion	tilt	LET	run_duration	entered_fluence
2018 W06	RADEF	vacuum	42	72	3	LS	1.45	SEL	85	Xe	0	60	501	1.00E+07
2018 W06	RADEF	vacuum	43	73	4	LS	1.45	SEL	85	Xe	0	60	479	1.00E+07

Table 5 – Runs table for SEL test runs

The corresponding runs chronograms are shown in Figure 10 and Figure 11.

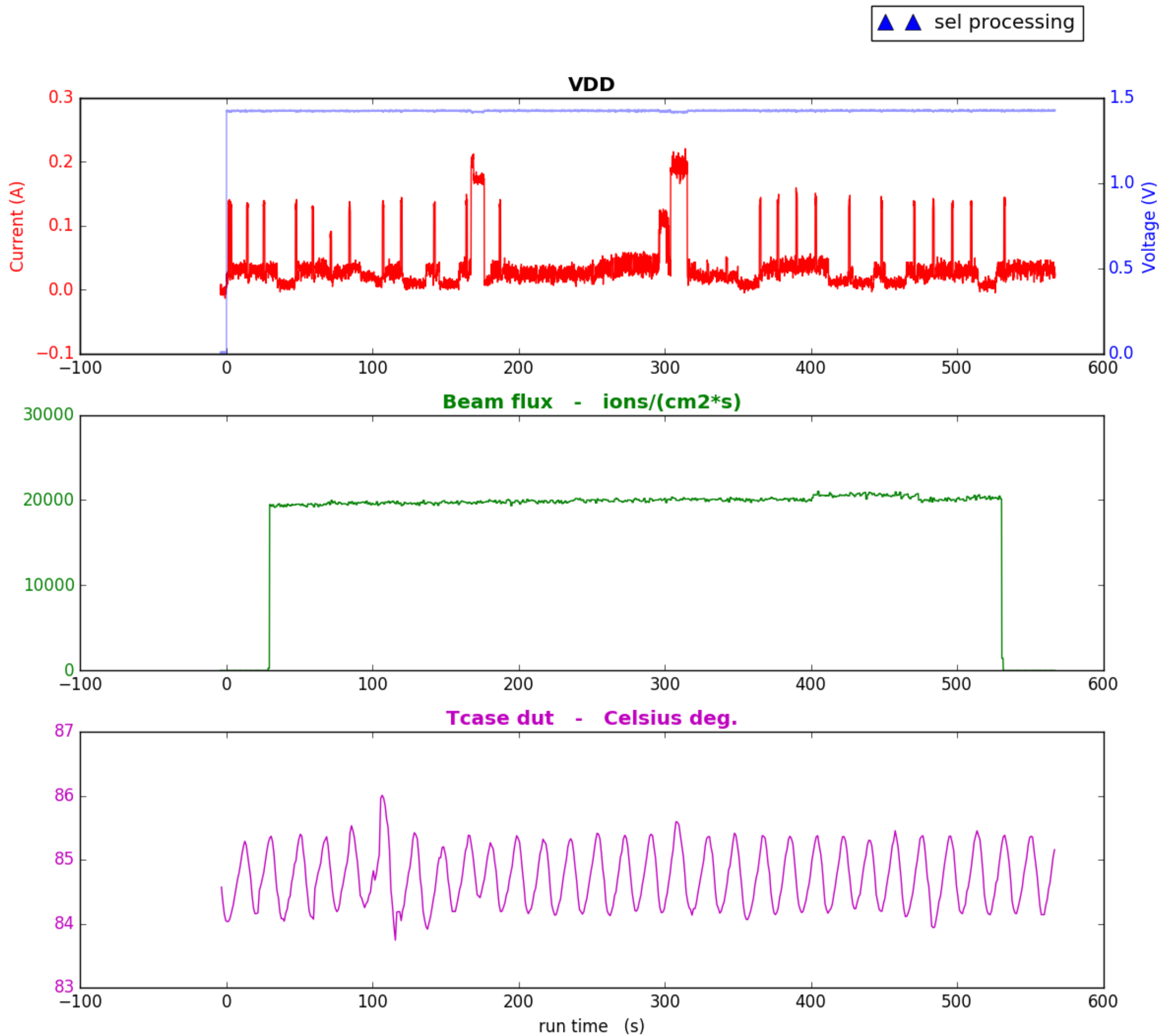


Figure 10 – MT41K512M8RH, SEL test board 3, Low Speed, Run042 chronogram

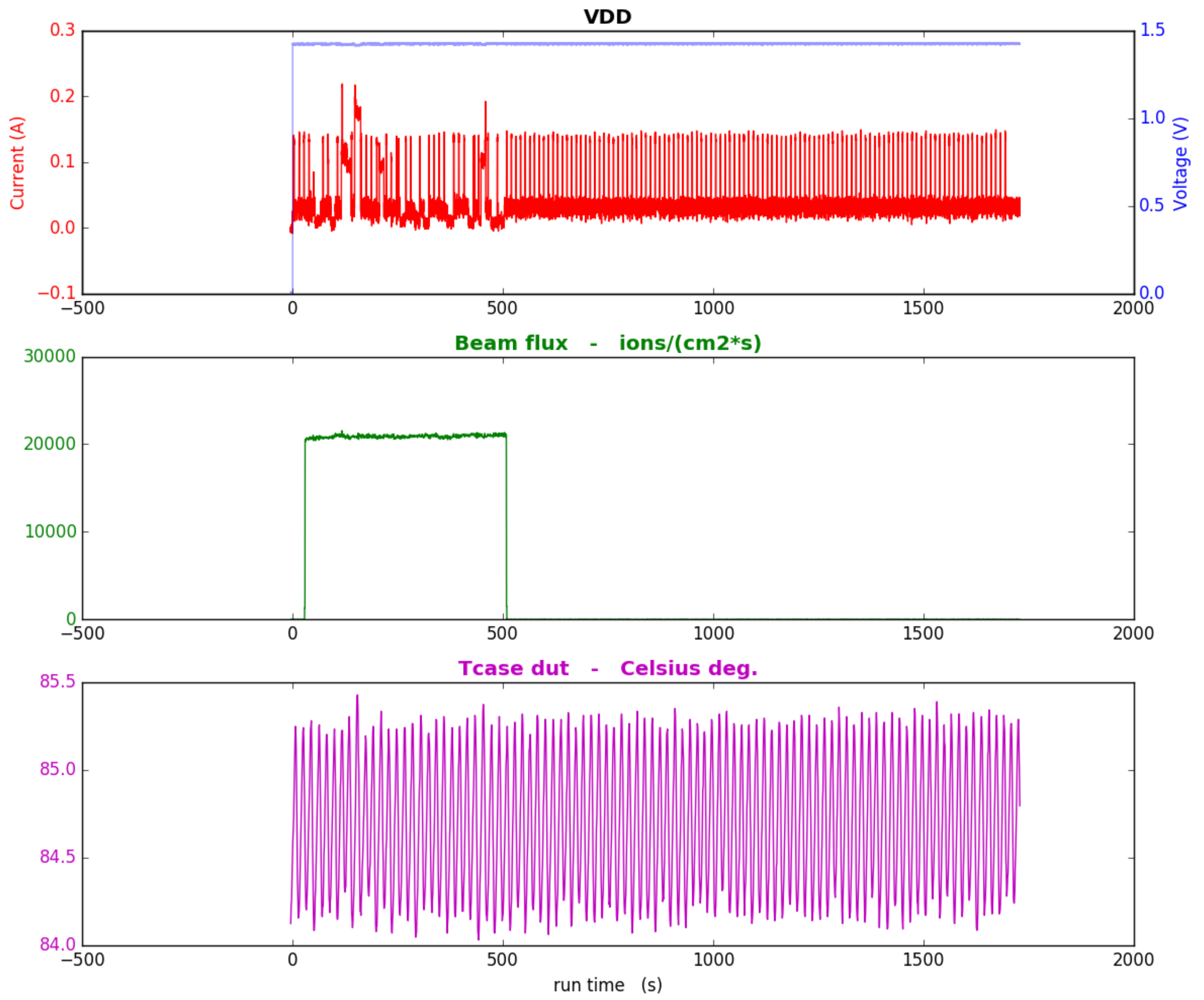


Figure 11 – MT41K512M8RH, SEL test board 4, Low Speed, Run043 chronogram

10 Glossary

DUT: Device under test.

Fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.
In this document, Fluence is expressed in ions per cm².

Flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.
In this document, Flux is expressed in ions per cm².s.

Single-Event Effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.
Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL).

Single Event Gate Rupture (SEGR) **/ Single Event Dielectric Rupture (**SEDR**):** Destructive rupture of the gate oxide layer or dielectric layer by a single ion strike. This leads to leakage currents under bias and can be observed as stuck bits in digitals devices

Single-Event Upset (SEU)**:** A soft error caused by the transient signal induced by a single energetic particle strike.

Single-Event Transient (SET): A transient signal induced by a single energetic particle strike.

Single-Event Latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.
SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.
An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

Single-Event Functional Interrupt (SEFI): A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single-event burnout (SEB).
A SEFI is often associated with an upset in a control bit or register.

Error cross-section: the number of errors per unit fluence. For device error cross-section, the dimensions are cm² per device. For bit error cross-section, the dimensions are cm² per bit.

Tilt angle: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis

Weibull fit: $F(x) = A (1- \exp\{-[(x-x_0)/W]^s\})$ with:

> x = effective LET in MeV/(mg/cm²);
> F(x) = SEE cross-section in cm²;
> A = limiting or plateau cross-section;
> x_0 = onset parameter, such that $F(x) = 0$ for $x < x_0$;
> W = width parameter;
> s = a dimensionless exponent.

Error bars: error bars are computed using a confidence level of 95% and a beam flux uncertainty of +/-10% as recommended by Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100.