Single Event Effects

Heavy Ion Test Report

Test type	Single-Event Upset, Single Event Latchup, SEFI
Part Reference	H5TC4G83CFR
Tested function	DDR3L SDRAM
Chip manufacturer	Hynix
Test Facility	RADEF, University of Jyväskylä
Test Date	December 2017, January 2018
Customer	ESA ESTEC

Esa Estec Purchase Order N° 4000112477/14/NL/HB dated December 4th, 2014

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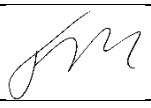
Authorized by:	F.X. Guerre	Study Manager		

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Contributors to this work

Frédéric Lochon — Hirex Engineering
Bendy Tanios — Hirex Engineering

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1 Introduction

This report presents results of SEE heavy ion test campaigns for the Hynix DDR3L SDRAM H5TC4G83CFR. 4 parts were used with 2 parts per test mode, high speed and low speed. The test campaign took place at RADEF, University of in December 2017 and January 2018.

2 Applicable and Reference Documents

Applicable Documents

AD-1 Hynix H5TC4G83CFR 4Gb DDR3L SDRAM Datasheet, Rev. 1.4/ Oct. 2015

AD-2 H5TC4G83CFR physical analysis HRX/RCA/00106

Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

3 Device Information

Device description

H5TC4G83CFR, DDR3L SDRAM

Manufacturer:	Hynix		
Package:	78-Ball FBGA 7.5 x 11 mm		
Marking:	SKhynix H5TC4G83CFR	PBA 517A	DWMG0900XH2
Date code	1517		
Technology:	CMOS		
Die dimensions:	5.2 x 6.5 mm		

This 4Gb memory is composed of 1 die with 8 banks of 1024 rows by 65536 columns of 8 bits words.

Device and die identification

Figure 1: Package, top.

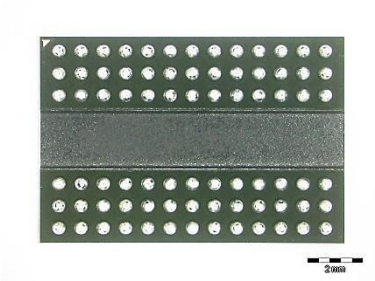


Figure 2: Package, bottom.

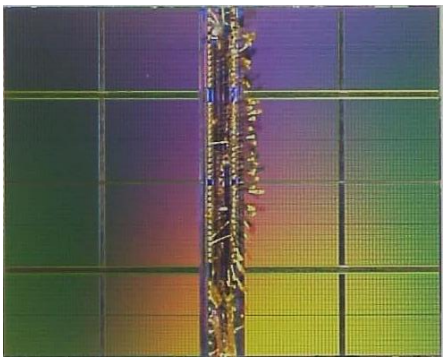


Figure 3: Die view.

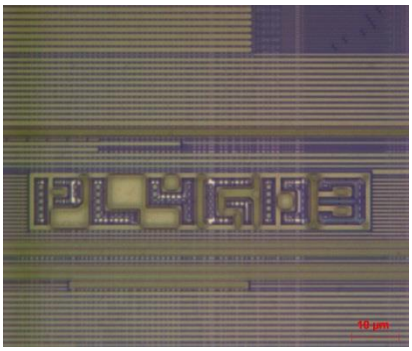


Figure 4: Die marking.

Sample preparation

Each DUT has been prepared by die back thinning down to a die thickness lower or equal to 50 microns.

4 Test Setup

Figure 5 shows the principle of the single event test system.
The test system is based on a Kintex7 FPGA (Xilinx).
The test board includes 2 slots for high speed and low speed SODDIMM daughter boards on which is mounted one DUT memory.
The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 24 independent channels.
The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.
One DUT (low speed or high speed) is exposed at a time

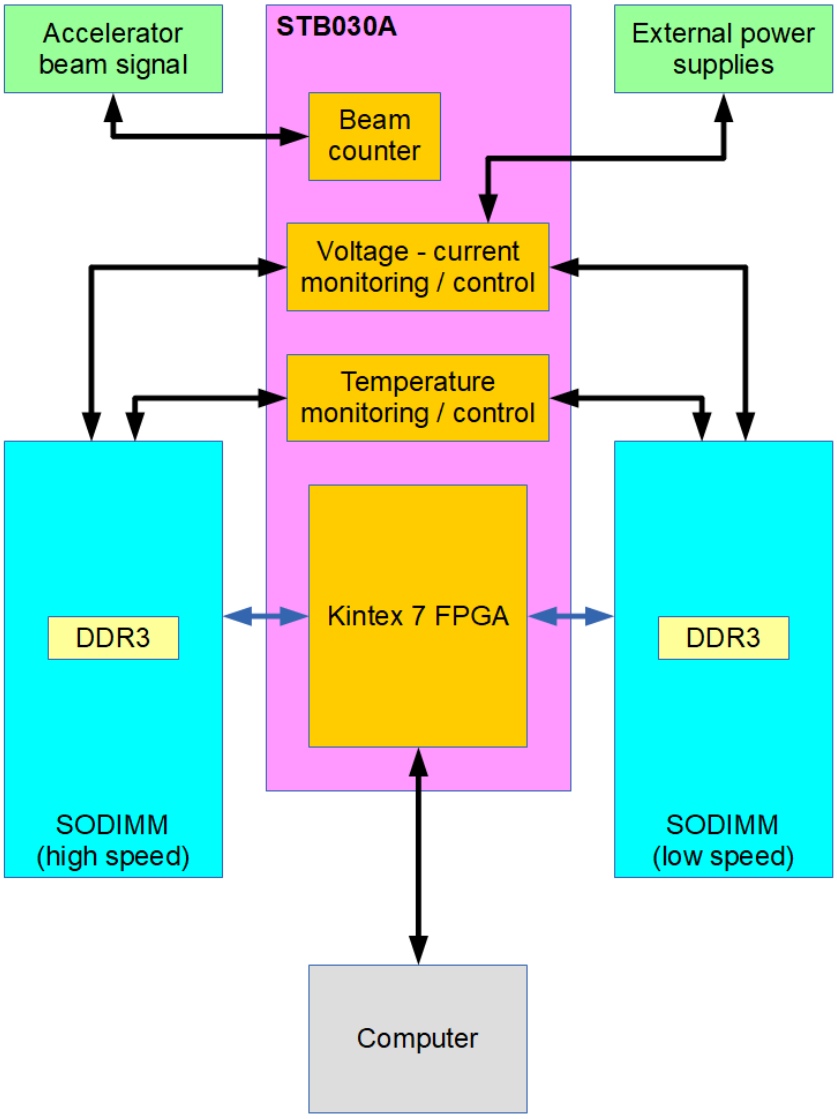


Figure 5: Hirex SEE test setup

5 Test sequences

Low speed mode is performed at a DUT clock frequency of 325MHz while high speed is performed at 700MHz. Refresh time is set to 6.8µs.

Read/Write sequence

- Repeat cycles:
  - Write memory with 0x55 /0xAA
  - Wait 1s
  - First Read memory (R1)
  - Second Read memory (R2)

Before the test campaigns, the following has been checked:

- Write the entire memory
- Then repeat cycles
  - Load register step or a Reset DDR3
  - Read memory

No error could be detected

That is why the basic Read/Write sequence have been modified to create 2 new test sequences.

Read/Write with load registers sequence

- Repeat cycles:
  - Load MRS
  - Wait 0.1s
  - Write memory with 0x55 /0xAA
  - Wait 0.5s
  - Load MRS
  - Wait 0.1s
  - First Read memory (R1)
  - Second Read memory (R2)

Read/Write with DUT reset sequence

- Repeat cycles:
  - Reset DDR3
  - Wait 0.1s
  - Write memory with 0x55 /0xAA
  - Wait 0.5s
  - Reset DDR3
  - Wait 0.1s
  - First Read memory (R1)
  - Second Read memory (R2)

The two functions Load MRS and Reset DDR3 are detailed here below

Load MRS
re-program mode registers MR0-MR3 of the DDR3 memory via MRS command

Reset DDR3
used to clear all state information in the DDR3 memory device.
The reset sequence as preconized by devices datasheets and JEDEC standard No. 79-3F is the following:

1- Physical reset (Warm reset) using DDR3 RESET# pin
2- Load mode registers via MRS command
3- ZQ Calibration used to calibrate the DDR3 memory output drivers and ODT (On-Die Termination) values via ZQCL command

6 RADEF facility

The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.
The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula,

$$130\ Q^2/M,$$

where Q is the ion charge state and M is the mass in Atomic Mass Units.

6.1 Test chamber

Irradiation of components is performed in a vacuum chamber with an inside diameter of 75 cm and a height of 81 cm.
The vacuum in the chamber is achieved after 15 minutes of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the X, Y and Z directions. The possibility of rotation around the Y-axis is provided by a round table. The free movement area reserved for the components is 25 cm x 25 cm, which allows one to perform several consecutive irradiations for several different components without breaking the vacuum.
The assembly is equipped with a standard mounting fixture. The adapters required to accommodate the special board configurations and the vacuum feed-throughs can also be made in the laboratory's workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components.
A CCD camera with a magnifying telescope is located at the other end of the beam line to determine accurate positioning of the components. The coordinates are stored in the computer's memory allowing fast positioning of various targets during the test.

6.2 Beam quality control

For measuring beam uniformity at low intensity, a CsI(Tl) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis.
A set of four collimated PIN-CsI(Tl) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.
Two beam wobblers and/or a 0.5 microns diffusion Gold foil can be used to achieve good beam homogeneity. The foil is placed 3 m in front of the chamber. The wobbler-coils vibrate the beam horizontally and vertically, the proper sweeping area being attained with the adjustable coil-currents.

6.3 Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI(Tl) detectors. Three collimators of different size and shape are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.
At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(Tl) detectors.

6.4 Used ions

Ion	LET^{SRIM} at surface [$MeV.cm^2.mg^{-1}$]	Range [µm]	Beam energy [MeV]
$^{15}N^{4+}$	1.83	202	139
$^{20}Ne^{6+}$	3.63	146	186
$^{40}Ar^{12+}$	10.2	118	372
$^{56}Fe^{15+}$	18.5	97	523
$^{82}Kr^{22+}$	32.1	94	768
$^{131}Xe^{35+}$	60.0	89	1217

SRIM-2003.26

Table 1 - Ion beam setting

7 Test conditions.

SEU tests were carried out closed to Vddmin at 1.30V and room temperature (1.35V and room temperature during January 2018 campaign).
Each memory present 8 banks of 65536 columns by 1024 rows of 8-bit words.
Each memory plane is traversed by bank, column, row which means that bank0, column0, row 0 to row 1023 is read, then bank0, column1, row 0 to row 1023, etc.
Read is done by burst which corresponds to 8 words. Each time at least 1 word is in error among the 8 words, the burst is recorded.

8 Detailed results

8.1 Read/write sequence

Results are summarized in Table 2.

Campaign	Medium	board_id	bias_config	power_config	test_mode	Ion	tilt	LET	duration	Fluence	Fluence without clamped steps	pre run errors	R1 bit errors	R1R2 bit errors	R2 bit errors	Persistent bit errors	total bit errors	Column	Row	sefi	total logic error	Post-run bit errors	bit capacity	SEU X-section /bit	Logic errors / device	stcuck errors /bit
w50_2017	vacuum	H2	HS	1.3	R/W	Ar	0	10.2	1140	1.00E+06	8.79E+05	0	0	103	113	0	216	4	51	2	57	0	4.295E+09	5.72E-14	6.49E-05	
w50_2017	vacuum	H2	HS	1.3	R/W	Fe	0	18.5	418	2.00E+05	1.76E+05	0	7	223	212	0	442	1	21	1	23	0	4.295E+09	5.84E-13	1.31E-04	
w50_2017	vacuum	H2	HS	1.3	R/W	Kr	0	32.2	379	2.00E+05	1.87E+05	2	31	1598	1561	40	3230	2	36	2	40	9	4.295E+09	4.02E-12	2.14E-04	1.28E-14
w50_2017	vacuum	H2	HS	1.3	R/W	N	0	1.83	245	2.00E+06	2.00E+06	0	0	0	0	0	0	0	0	0	0	0	4.295E+09			
w06_2018	vacuum	H2	HS	1.35	R/W	Xe	0	60	1611	2.00E+06	1360345	1003	960	12476	15823	11681	40940	6	113	8	127	9079	4.295E+09	7.01E-12	9.34E-05	1.17E-12
w50_2017	vacuum	H3	HS	1.3	R/W	Ar	0	10.2	1128	1.00E+06	7.21E+05	1	8	74	74	0	156	1	36	2	39	0	4.295E+09	5.04E-14	5.41E-05	2.33E-16
w50_2017	vacuum	H3	HS	1.3	R/W	N	0	1.83	206	2.00E+06	2.00E+06	1	0	0	0	0	0	0	0	0	0	0	4.295E+09			1.16E-16
w50_2017	vacuum	H3	HS	1.3	R/W	Fe	0	18.5	434	2.00E+05	7.90E+03	1	0	14	9	0	23	0	0	1	1	0	4.295E+09	6.78E-13	1.27E-04	1.16E-15
w50_2017	vacuum	H3	HS	1.3	R/W	Kr	0	32.2	372	2.00E+05	2.00E+05	1	0	1763	1654	41	3458	2	35	0	37	0	4.295E+09	4.03E-12	1.85E-04	1.16E-15
w06_2018	vacuum	H3	HS	1.35	R/W	Xe	0	60	1752	2.00E+06	6.02E+05	115	447	6136	8424	13358	28365	6	54	6	66	10857	4.295E+09	1.10E-11	1.10E-04	1.28E-12
w50_2017	vacuum	H2	LS	1.3	R/W	Ar	0	10.2	1168	1.00E+06	9.38E+05	0	0	86	104	0	190	4	44	1	49	0	4.295E+09	4.72E-14	5.22E-05	
w50_2017	vacuum	H2	LS	1.3	R/W	N	0	1.83	273	2.00E+06	2.00E+06	0	0	0	0	0	0	0	0	0	0	0	4.295E+09			
w50_2017	vacuum	H2	LS	1.3	R/W	Fe	0	18.5	436	2.00E+05	2.00E+05	0	0	307	345	1	653	0	14	1	15	0	4.295E+09	7.60E-13	7.50E-05	
w50_2017	vacuum	H2	LS	1.3	R/W	Kr	0	32.2	382	2.00E+05	2.00E+05	0	0	1537	1864	46	3447	0	39	0	39	7	4.295E+09	4.01E-12	1.95E-04	8.15E-15
w50_2017	vacuum	H3	LS	1.3	R/W	Ar	0	10.2	613	1.00E+05	1.00E+05	1	0	9	19	0	28	0	4	0	4	0	4.295E+09	6.52E-14	4.00E-05	2.33E-15
w50_2017	vacuum	H3	LS	1.3	R/W	Ar	0	10.2	1008	1.00E+06	7.49E+05	1	3	70	88	0	161	3		4	7	0	4.295E+09	5.01E-14	9.35E-06	2.33E-16
w50_2017	vacuum	H3	LS	1.3	R/W	N	0	1.83	276	2.00E+06	2.00E+06	1	0	0	0	0	0	0	0	0	0	0	4.295E+09			1.16E-16
w50_2017	vacuum	H3	LS	1.3	R/W	Fe	0	18.5	434	2.00E+05	2.00E+05	1	0	405	438	0	843	2	18	0	20	0	4.295E+09	9.81E-13	1.00E-04	1.16E-15
w50_2017	vacuum	H3	LS	1.3	R/W	Kr	0	32.2	384	2.00E+05	2.00E+05	9	0	1703	2036	59	3798	0	26	0	26	3	4.295E+09	4.42E-12	1.30E-04	1.40E-14

Table 2: Detailed SEE results.

Pre-run errors
Stuck bits present before exposure. They could have been created during previous runs on the DUT.
R1 bit errors
Number of errors detected during READ1 but not during READ2. These errors which represent reading errors are very few and affect only a limited number of READ1 steps.
R1/R2 bit errors
Number of errors detected during READ1 and during READ2. These errors represent SEU WRITE bit errors or SEU cells errors occurring during the time the cell is not written (as for instance during WAIT step but not only).
R2 bit errors
Number of errors detected during READ2 only: These errors represent reading errors which are expected to be quite few as for R1 bit errors and the SEU cells errors occurring during the time the cell is not read.
Persistent bit errors
Bit errors that last more than one sequence iteration. Part of these errors can persist up to the end of the run and are then counted as post-run bit errors (stuck bits). Pre-run errors have been subtracted from the persistent bit error count.
Colum error
Likely an error in the logic. A column error can affect two banks at a time.
Row errors
Likely an error in the logic. Consist in a portion of row in error in a bank.
SEFI
These errors consist mainly in column errors that persist during several sequence iterations. Most of them induce a count clamped to the limit set at 50000. Only a few involved only a single column. The vast majority have been cured by a manual power reset. Some have disappeared under exposure without any external action.
Post-run bit errors
The errors are stuck bits. All affected words are single bit upset.

Figure 6 shows the SEU bit error cross-section for the 2 test modes, low speed and high speed. Test with Xenon was performed with a DUT bias of 1.35V while the tests with the other ions were performed at 1.30V.
No significant difference is observed between the two test modes.

Weibull parameters

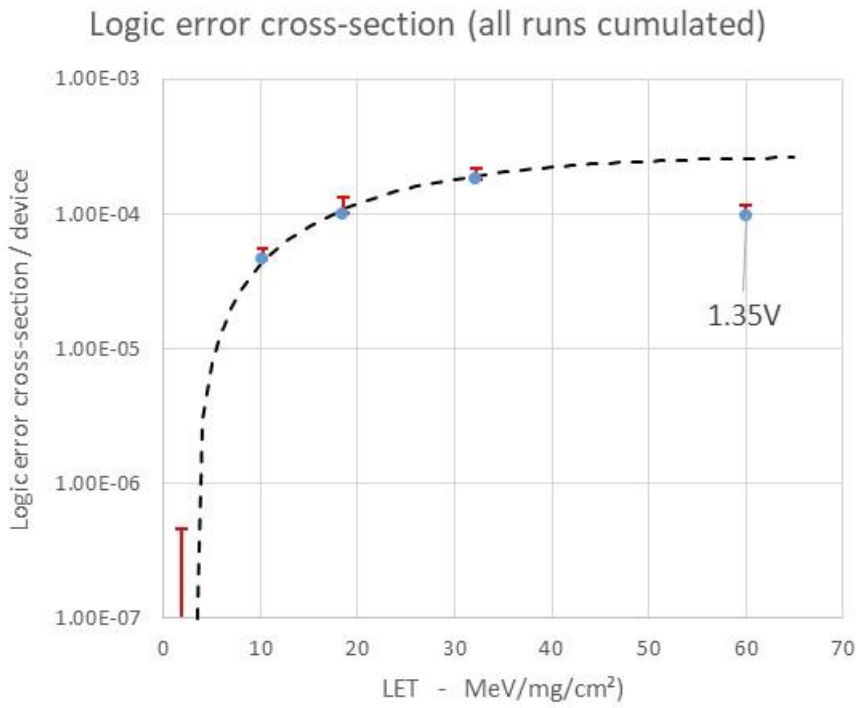
W	45
xo	6
s	2.5
A	1.70E-11

Figure 6 – H5TC4G83CFR, High Speed and Low Speed Read Write, SEU bit error cross-section / bit

For the logic errors, column, row and SEFI, all runs have been cumulated for each ion as shown in Table 3. The corresponding Logic error cross-section is plot in Figure 7.

Power config	Ion	LET	Cumulated effective fluence / ion	Cumulated logic errors
1.3	N	1.83	8.00E+06	0
1.3	Ar	10.2	3.39E+06	156
1.3	Fe	18.5	5.84E+05	59
1.3	Kr	32.2	7.87E+05	142
1.35	Xe	60	1.96E+06	193

Table 3 Cumulated logic errors per ion



Weibull parameters

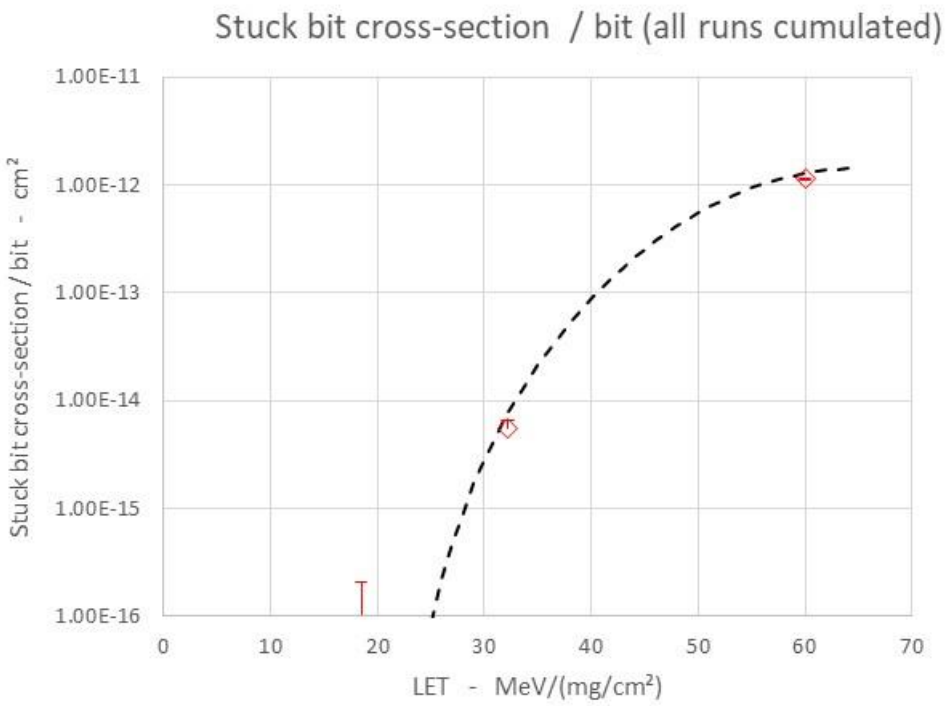
W	25
xo	3
s	1.4
A	2.70E-04

Figure 7 – Cumulated Logic error cross-section plot

For the stuck bit errors, all runs have been cumulated for each ion as shown in Table 4. The corresponding stuck bit cross-section per bit is plot in Figure 8. In this case the total run fluence has been considered and not the effective run fluence.

Power config	Ion	LET	Cumulated fluence / ion	Cumulated stuck bit errors	bit capacity	stuck bit Cross-section / bit
1.3	Ar	10.2	4.10E+06	0	4.29E+09	
1.3	Fe	18.5	8.00E+05	0	4.29E+09	
1.3	Kr	32.2	8.00E+05	19	4.29E+09	5.53E-15
1.35	Xe	60	4.00E+06	19936	4.29E+09	1.16E-12

Table 4 - Cumulated stuck bit errors per ion



Weibull parameters

W	35
xo	20
s	5
A	1.50E-12

Figure 8 – Cumulated stuck bit error cross-section plot

8.2 Read/Write with load registers or DUT reset sequences

Purpose of these sequences was to evaluate the addition in the read/write sequence of steps for either reloading the DUT register content or doing a DUT reset, in SEFI occurrence.
No power reset was performed during these runs to clear SEFI if any.
The corresponding table of runs is shown in Table 5.

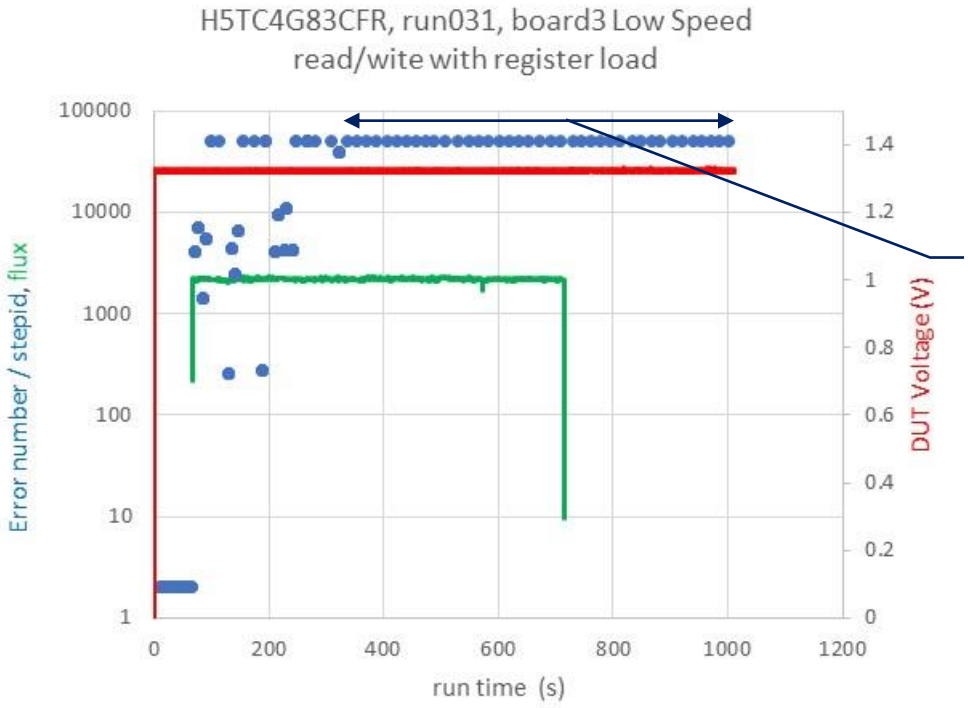
The run chronograms are shown in Figure 9 and Figure 10.
The insertion of DRR3 resets in the read write sequence look to be able to avoid SEFI occurrence while insertion of load registers steps is not sufficient to avoid any SEFI.

Test campaign	Facility	dut_medium	run_number	Facility_run_number	board_id	bias_config	power_config	test_mode	temperature	Ion	tilt	LET	run_duration	entered_fluence
2018 W06	RADEF	vacuum	31	64	3	LS	1.35	load mrs	room	Kr	0	32	834	1.42E+06
2019 W06	RADEF	vacuum	32	65	3	LS	1.35	reset ddr3	room	Kr	0	32	918	2.00E+06
2020 W06	RADEF	vacuum	33	66	2	LS	1.35	reset ddr3	room	Kr	0	32	819	2.00E+06
2021 W06	RADEF	vacuum	34	67	2	LS	1.35	load mrs	room	Kr	0	32	775	2.00E+06

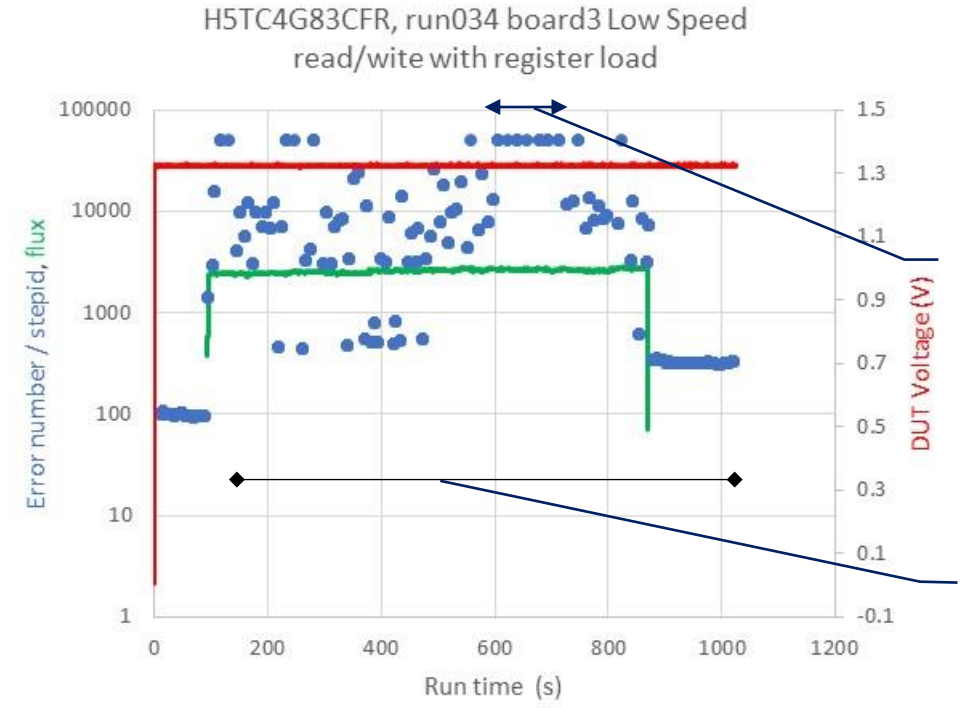
Table 5 – Runs table for Read/write with load registers or DUT reset sequences

Read/Write sequence including load registers steps

Run031 and Run034 have been performed with the read/write sequence including load registers and the run chronograms are shown here below.
At least one SEFI has been observed during run031.



Serie of clamped (50000) large errors with the same signature still permanent after beam stop
=
SEFI



Serie of clamped (50000) large errors not with the same signature disappearing under beam exposure

SEFI ?

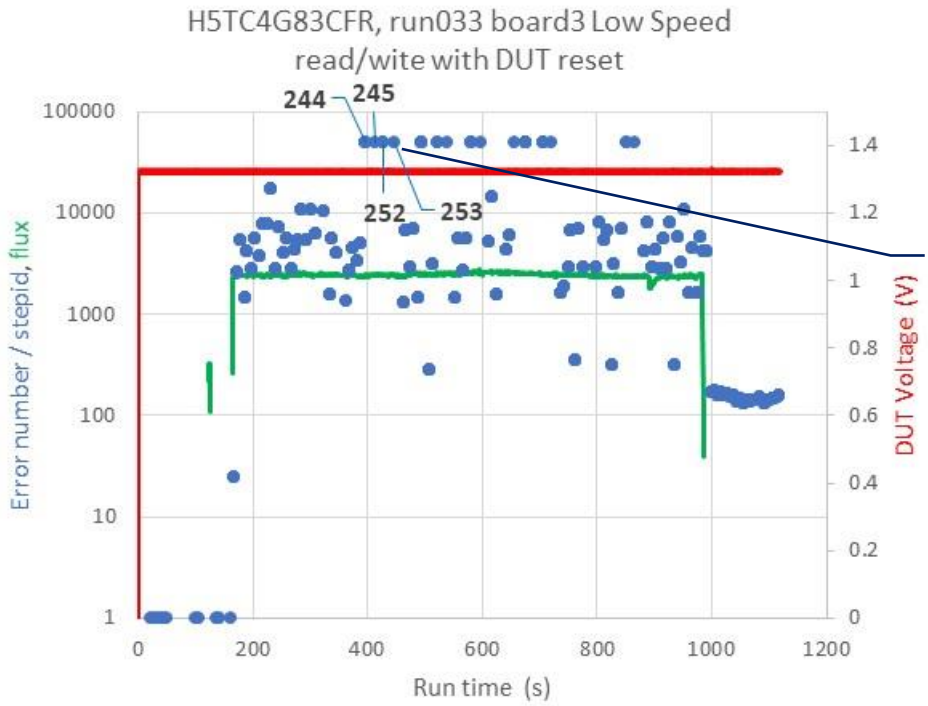
SEFI column
(about 261 cell errors at row=41184)
from
stepid 92 to 514
still permanent after beam stop

Figure 9 – Run chronograms for read/write with load registers sequence

Read/Write sequence including DUT reset steps

No Serie of clamped (50000) large errors.
Only R1 stepid followed by R2 stepid

No SEFI



Error in Stepid
244 (R1) / 245 (R2)
has a different signature than error in Stepids
252 (R1)/ 253(R2)

Very likely not a SEFI

Figure 10 – Run chronograms for read/write with DUT reset sequence

8.3 SEL test runs

During test campaign 2018 W06, 2 runs have been performed with Xenon at 1.45V and a temperature of 85°C.
During SEL testing, read/write sequence was executed with a very low clamp limit for each stepid.
No SEL has been observed on the 2 samples.
Table 6 list the SEl runs performed.

Test campaign	Facility	dut_medium	run_number	Facility_run_number	board_id	bias_config	power_config	test_mode	temperature	Ion	tilt	LET	run_duration	entered_fluence
2018 W06	RADEF	vacuum	40	70	2	LS	1.45	SEL	85	Xe	0	60	1101	1.00E+07
2019 W06	RADEF	vacuum	41	71	3	LS	1.45	SEL	85	Xe	0	60	688	1.00E+07

Table 6 – Runs table for SEL test runs

The corresponding runs chronograms are shown in Figure 11 and Figure 12.

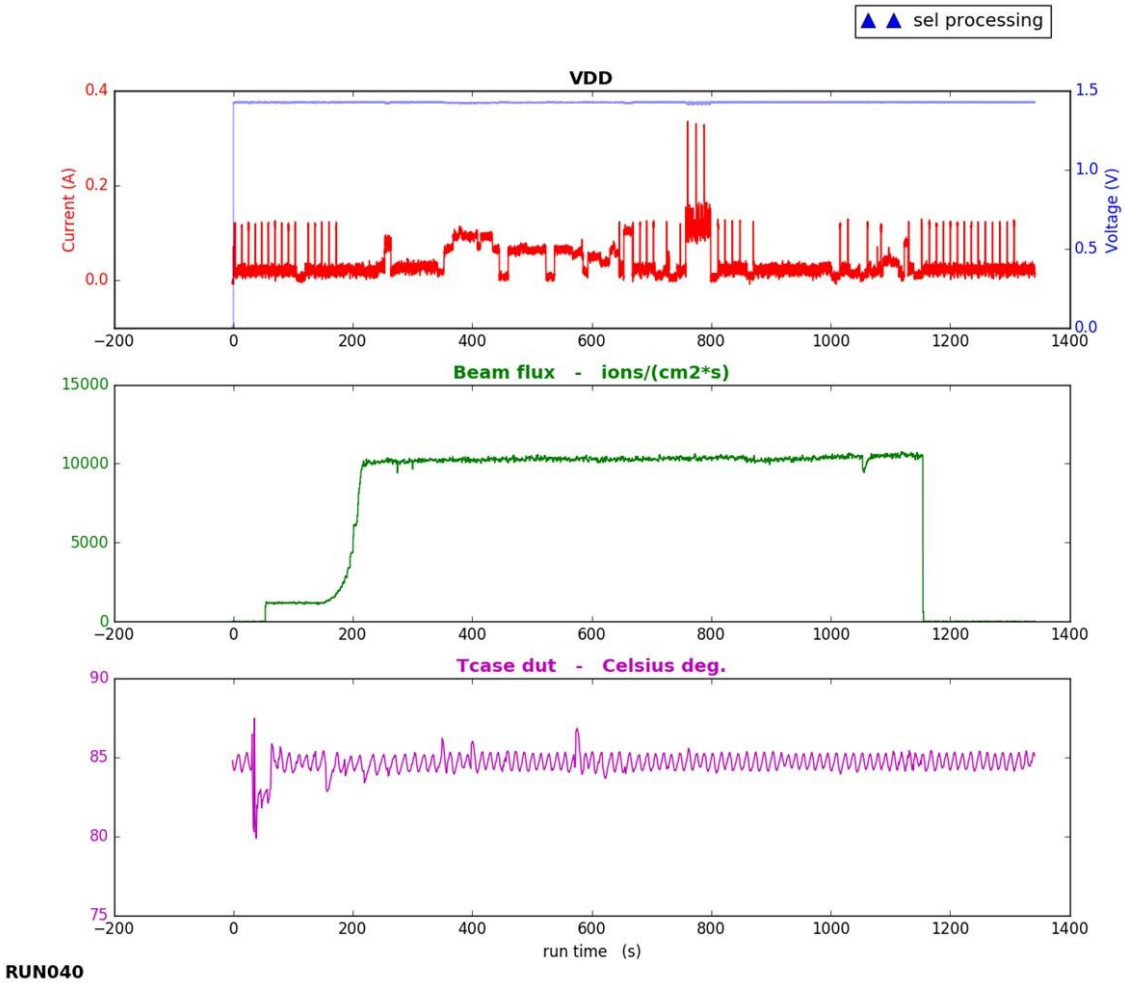


Figure 11 – H5TC4G83CFR, SEL test board 2 , Low Speed, Run040 chronogram

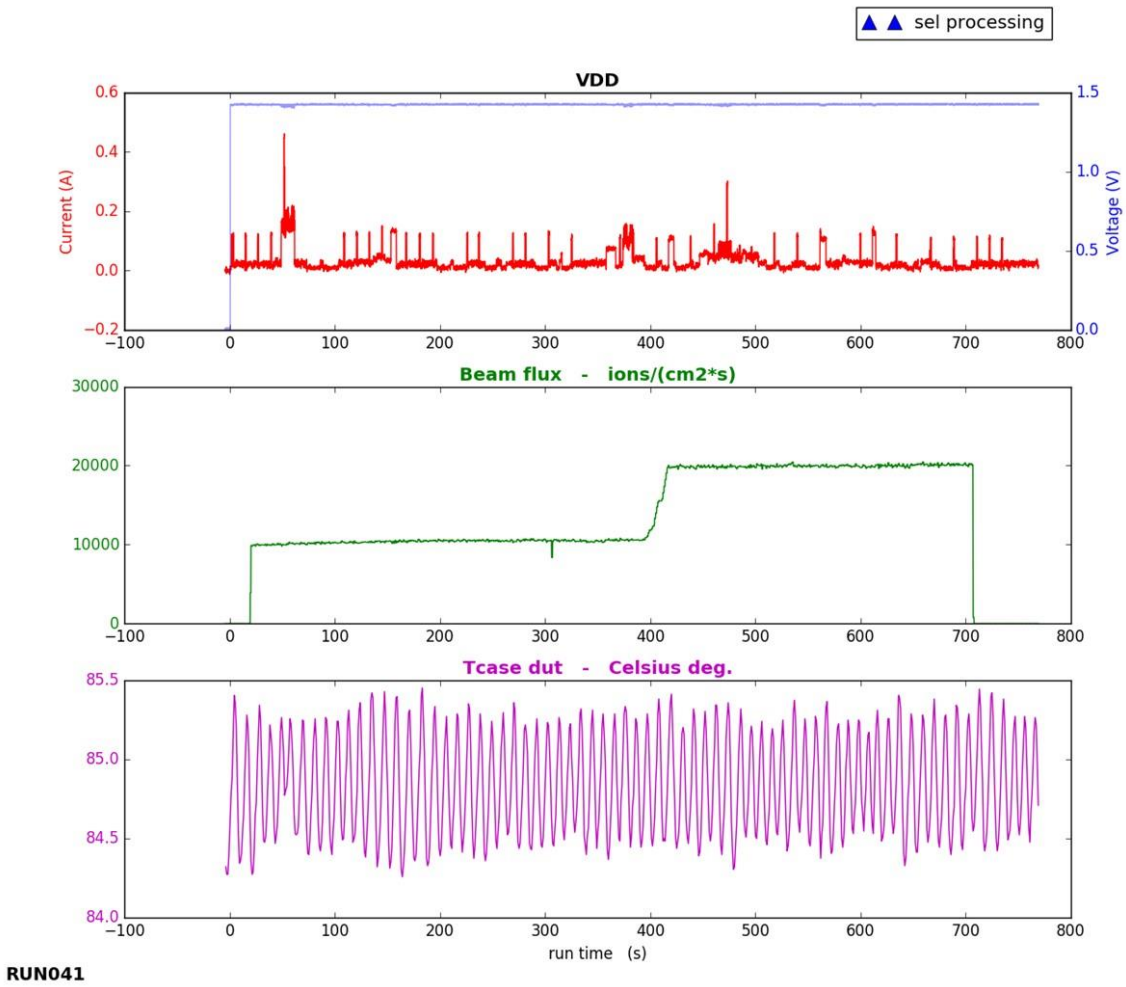


Figure 12 – H5TC4G83CFR, SEL test board 3 , Low Speed, Run041 chronogram

9 Glossary

DUT: Device under test.

Fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.
In this document, Fluence is expressed in ions per cm².

Flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.
In this document, Flux is expressed in ions per cm².s.

Single-Event Effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.
Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL).

Single Event Gate Rupture (SEGR) **/ Single Event Dielectric Rupture (**SEDR**):** Destructive rupture of the gate oxide layer or dielectric layer by a single ion strike. This leads to leakage currents under bias and can be observed as stuck bits in digitals devices

Single-Event Upset (SEU)**:** A soft error caused by the transient signal induced by a single energetic particle strike.

Single-Event Transient (SET): A transient signal induced by a single energetic particle strike.

Single-Event Latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.
SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.
An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

Single-Event Functional Interrupt (SEFI): A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single-event burnout (SEB).
A SEFI is often associated with an upset in a control bit or register.

Error cross-section: the number of errors per unit fluence. For device error cross-section, the dimensions are cm² per device. For bit error cross-section, the dimensions are cm² per bit.

Tilt angle: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis

Weibull fit: $F(x) = A\,(1- \exp\{-[(x-x_0)/W]^s\})$ with:

x = effective LET in MeV/(mg/cm²);
$F(x)$ = SEE cross-section in cm²;
A = limiting or plateau cross-section;
x_0 = onset parameter, such that $F(x) = 0$ for $x < x_0$;
W = width parameter;
s = a dimensionless exponent.

Error bars: error bars are computed using a confidence level of 95% and a beam flux uncertainty of +/-10% as recommended by Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100.