Single Event Effects

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Proton Test Report

Test type	Single-Event Upset, Single Event Latchup
Part Reference	MX68GL1G0G
Tested function	NOR Flash Memory
Chip manufacturer	Macronix
Test Facility	PIF, Paul Scherrer Institute (PSI), Villigen, Switzerland
Test Date	February 2018
Customer	ESA ESTEC

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DOCUMENTATION CHANGE NOTICE

Issue	Date	Page	Change Item	
01	12/06/2018	All	Original issue	
02	10/08/2018	Cover page	Was Heavy Ion Test Report Is Proton Test Report	
		10	Cumulative dose up to DUT failure added	

DUT no	Board	Total dose (X=2) rad (Si)
2	10	3.13E+04
2	11	3.53E+04
2	12	3.14E+04

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1   Introduction

This report presents results of SEE proton test campaign for the Macronix NOR Flash Memory MX68GL1G0G. 8 parts were used with 2 parts per test sequence. The test campaign took place at PIF, Paul Scherrer Institute (PSI), Villigen, Switzerland in February 2018.

2   Applicable and Reference Documents

Applicable Documents

AD-1   Macronix MX68GL1G0G Datasheet, P/N:PM1910, MAY 29, 2014

AD-2   MX68GL1G0G physical analysis HRX/RCA/00108

Reference Documents

RD-1.   Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

RD-2.   Proton Irradiation Facility at the PROSCAN project of the Paul Scherrer Institute PIF facility at PSI, Ulrike Grossner, Wojtek Hajdas, Ken Egli, Roger Brun, and Reno Harboe-Sorensen, RADECS 2009.

3   Device Information

Device description

MX68GL1G0G, NOR Flash Memory

Manufacturer:	Macronix
Package:	FBGA-64
Marking:	MXIC X151927 MX68GL1G0GHXFI-10G 8B18430FBA
Date code	1519
Technology :	CMOS
Die dimensions :	5.4 mm x 7.2 mm
Device assembly :	Top **dual die** on PCB with solder balls

This 1Gb memory is composed of 2 dies of 512 blocks of 65536 x16 bits words. Write Buffer is 256 words while read buffer is 16 words.

Device and die identification

Figure 1: Package, top.
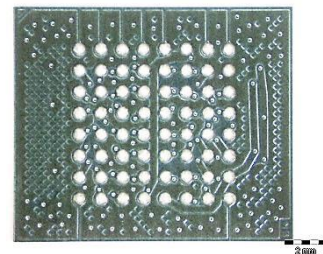
Figure 2: Package, bottom.
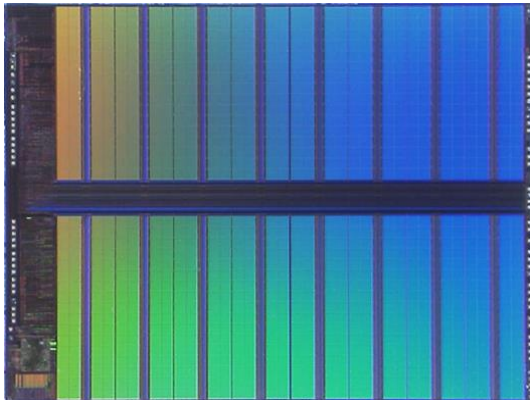
Figure 3: Die view (top die).

Figure 4: Die marking (top die).

4   Test Setup

Figure 5 shows the principle of the single event test system.

The test system is based on a Virtex4 FPGA (Xilinx). It runs at 50 MHz. The test board has 271 I/Os which can be configured using several I/O standards.

The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 24 independent channels.

The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.

SEL event is detected when the supply current is over a configurable threshold (typically 5 to 10 times the nominal current) and processed:

Once detected, SEL state is maintained for typically 1 or 2ms and power supplies are cut off during a wait time of typically 1 s. These times are configurable.

Each power supply under supervision is monitored independently for SEL detection and processing but subsequent cut off is performed on all power supplies.
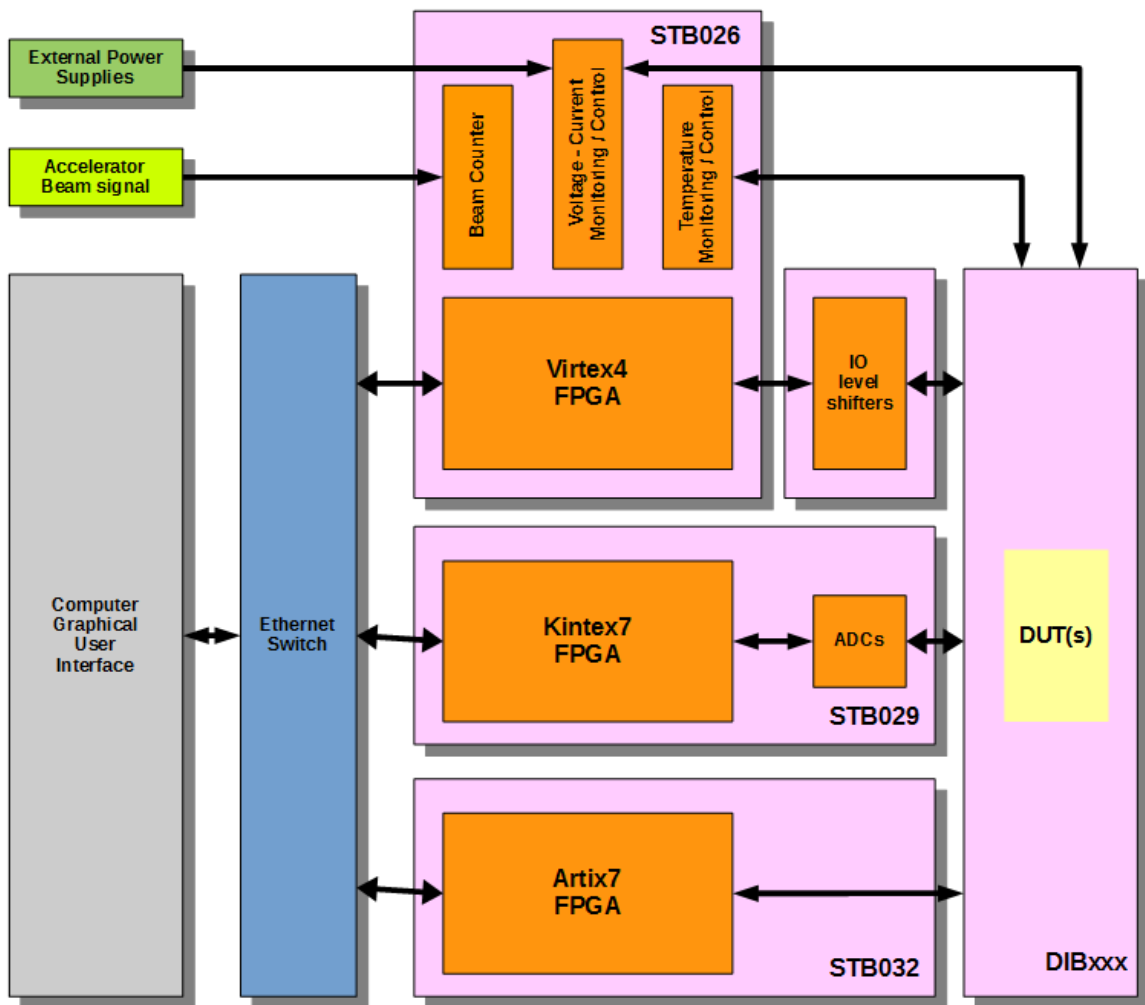
Figure 5: Hirex SEE test setup

A daughter board with 2 samples mounted on it has been designed for this test (DIB294A) and Figure 6 show a picture this board (for proton testing, the DUTs are not opened).

Figure 6 – DIB294A NOR flash daughter board

5 Test sequence

Test modes and their sequence used during the test campaign are summarized in Figure 7. Operations in grey boxes are performed before the irradiation. Operation in blue boxes are performed under irradiation and operations in yellow boxes are performed once the beam is stopped at the end of the run.

Off sequence

The DUT is turned off after the pre-run. It is then turned back on once the total fluence has been reached and the full chip is read (X=1).

Read sequence

The read sequence (X=3) consists in a loop of a read operation followed by a power-cycle and a second read operation. This sequence focuses on the same 10 blocks of the memory. The pattern used is alternatively 0x66 and 0x99 pattern for this dynamic test.

Both static and dynamic results can be extrapolated based on a single run result. This is done by considering 10 blocks for dynamic behaviour (X=3) and 450 blocks of the chip for static behaviour (X=5).

Erase/Write sequence

During the erase/write (E/W) sequence (X=2), the same 10 blocks are erased and then written under the beam flux. The shutter is then closed to power-cycle the DUT and read twice the blocks outside irradiation. These operations are then looped for the duration of the run.

X=1 "DUT off"

Erase
(450 blocks)

Write (0x55 / 0xAA)
(450 blocks)

Power off

Wait
(Fluence)

Power on

Read
(450 blocks)

X=3 "read"

Erase
(10 blocks)

Write (0x66 / 0x99)
(10 blocks)

N iteration times

Power reset
(1s)

Wait
(1s)

First read
10 blocks

Second Read
(10 blocks)

X=5 "DUT off +on"

Read
(450 blocks)

Runs with x=1, x=3 and x=5 are performed in this sequence order

The 450 blocks and the 10 blocks are distinct

X=2 "Erase write"

Erase
(10 blocks)

Write (0x66 / 0x99)
(10 blocks)

N Iteration times

Erase
10 blocks

Fill
10 blocks

Power reset
(1s)

Wait
(1s)

Reset

First read
(10 blocks)

First read
(10 blocks)

Wait
(5s)

X=6 "SEL"

Erase
(450 blocks)

Write (0x55 / 0xAA)
(450 blocks)

N iteration times

Reset

Wait
(2s)

Read (*)
450 blocks

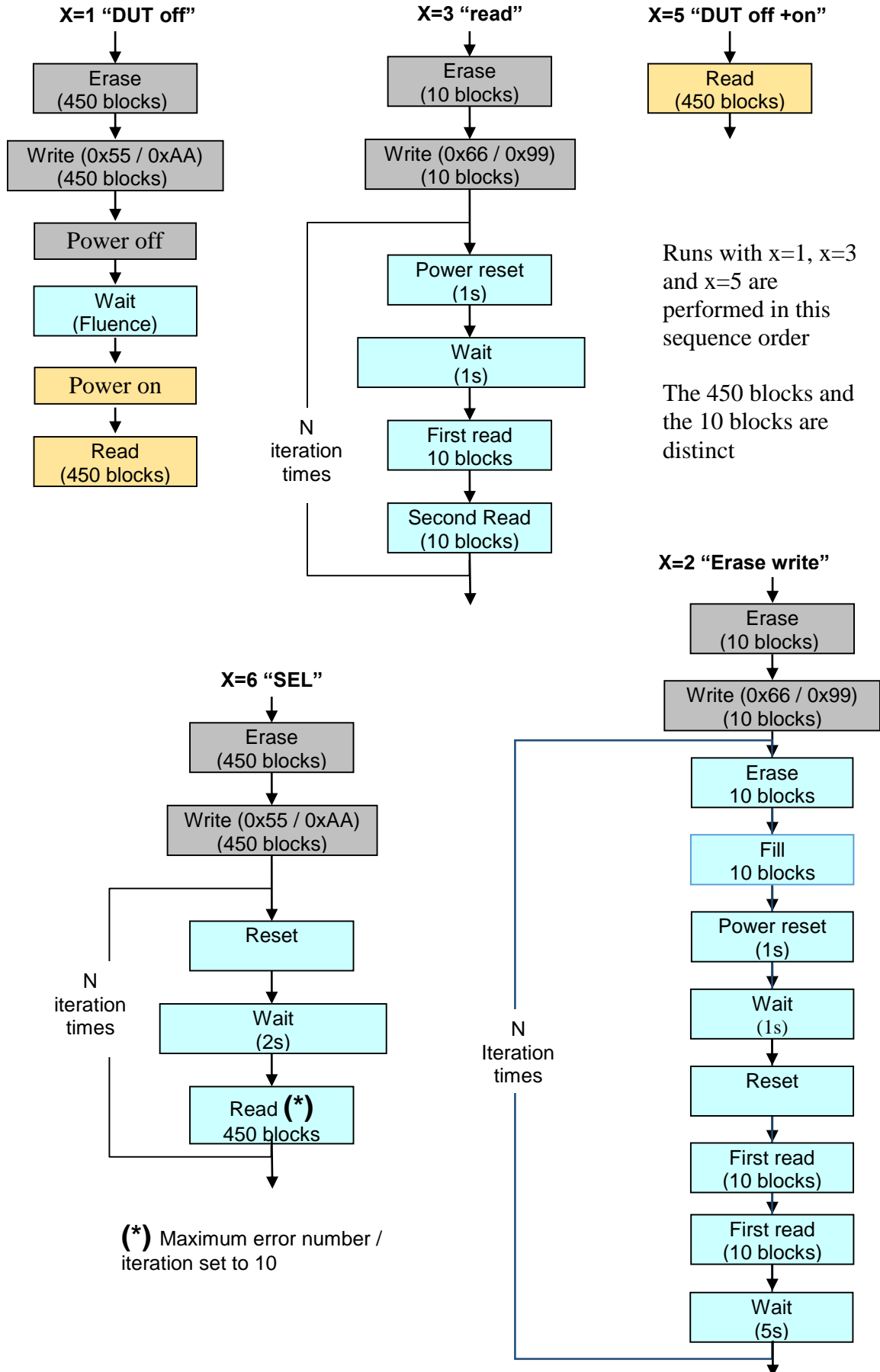(*) Maximum error number / iteration set to 10

Figure 7 - NOR Flash test sequences

6 PIF Test Facility

A description of PIF test facility can be found in RD-2. As shown in Figure 8, proton beam from COMET cyclotron is delivered to the experimental PIF cave with an input energy that can be varied from few MeVs up to 250 MeV. Then in PIF room, local copper degraders can be inserted into the beam to obtain the different user energies.

200 MeV input beam's energy was selected and calibrated. The corresponding calibration result is shown in Figure 9 together with the X and Y beam profiles.
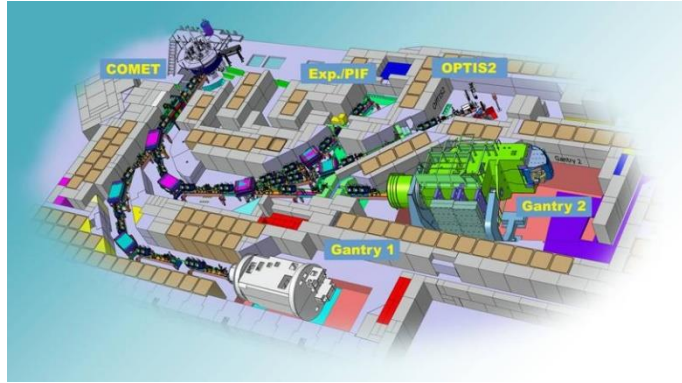

Figure 8 - Proscan facility

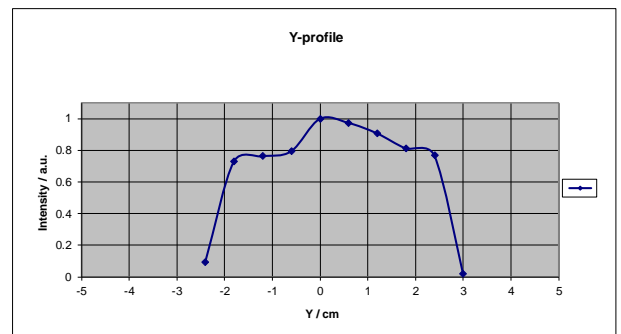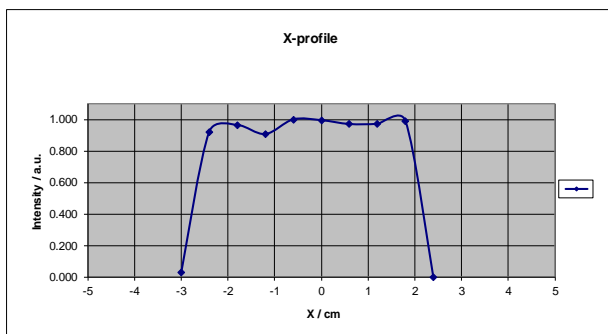| E0=200	Energy [MeV]	Degr. [mm]	Plastic [cnt/1s]	IC-target [cnt/1s]	IC-degr [cnt/1s]	Target(1) Fac. 20nA [p/cnt/cm2]	Degr(2) Fac. 20nA [p/cnt/cm2]	Target(1) Fac. 200nA	Degr(2) Fac. 200nA	Target(1) Fac. 2 uA	Degr(2) Fac. 2 uA	5.0cm collimator PL6 / 10cm distance to DUT-Collimator	FLUX [p/cm/s]	IC-curent [nA]	IC-deg [nA]	PROSCAN [nA]	RPOSCAN MAX [nA]	FLUX(max) [p/cm/s]	IC-deg [nA]
Pos 1	200	0.0	154136	200	67	12844.7	38342.3						2.57E+06	2.00E+00	6.70E-01	1.50E-01	1.00E+01	1.71E+08	4.47E+01
1	200	0.0	169632	227	74	12454.6	38205.4												
	60mV		10	3	2.7	1.26E+04	3.83E+04	1.26E+05	3.83E+05	1.26E+06	3.83E+06								
Pos 1	180.3	7.0	163897	232	77	11774.2	35475.5						2.73E+06	2.32E+00	7.70E-01	1.50E-01	1.00E+01	1.82E+08	5.13E+01
1	180.3	7.0	173136	246	81	11730.1	35624.7												
	60mV		10	3	2.7	1.18E+04	3.56E+04	1.18E+05	3.56E+05	1.18E+06	3.56E+06								
Pos 1	151.2	16.5	131820	208	68	10562.5	32308.8						2.20E+06	2.08E+00	6.80E-01	1.50E-01	1.00E+01	1.46E+08	4.53E+01
1	151.2	16.5	151328	240	78	10508.9	32335.0												
	60mV		10	3	2.7	1.05E+04	3.23E+04	1.05E+05	3.23E+05	1.05E+06	3.23E+06								
Pos 1	125.2	24.0	132028	248	78	8872.8	28211.1						2.20E+06	2.48E+00	7.80E-01	1.50E-01	1.00E+01	1.47E+08	5.20E+01
1	125.2	24.0	126705	239	76	8835.8	27786.2												
	60mV		10	3	2.7	8.85E+03	2.80E+04	8.85E+04	2.80E+05	8.85E+05	2.80E+06								
Pos 1	101.3	30.0	129616	303	93	7129.6	23228.7						2.16E+06	3.03E+00	9.30E-01	1.50E-01	1.00E+01	1.44E+08	6.20E+01
1	101.3	30.0	115130	267	82	7186.6	23400.4												
	60mV		10	3	2.7	7.16E+03	2.33E+04	7.16E+04	2.33E+05	7.16E+05	2.33E+06								
Pos 1	75.2	35.5	100278	322	86	5190.4	19433.7						1.67E+06	3.22E+00	8.60E-01	1.50E-01	1.00E+01	1.11E+08	5.73E+01
1	75.2	35.5	103597	331	89	5216.4	19400.2												
	60mV		10	3	2.7	5.20E+03	1.94E+04	5.20E+04	1.94E+05	5.20E+05	1.94E+06								
Pos 1	50.8	39.5	75856	375	84	3371.4	15050.8						1.26E+06	3.75E+00	8.40E-01	1.50E-01	1.00E+01	8.43E+07	5.60E+01
1	50.8	39.5	69935	342	77	3408.1	15137.4												
	60mV		10	3	2.7	3.39E+03	1.51E+04	3.39E+04	1.51E+05	3.39E+05	1.51E+06								
Pos 1	29.3	42.0	42198	462	71	1522.3	9905.6						7.03E+05	4.62E+00	7.10E-01	1.50E-01	1.00E+01	4.69E+07	4.73E+01
1	29.3	42.0	41396	450	69	1533.2	9999.0												
	60mV		10	3	2.7	1.53E+03	9.95E+03	1.53E+04	9.95E+04	1.53E+05	9.95E+05								

Figure 9 – 200MeV calibration results and beam profile

7 Test conditions.

SEU tests were carried out at Vddmin (2.7 V) and room temperature.

Samples for SEL were tested at Vddmax (3.6 V) and a junction temperature of 85°C while performing a static test.

8 Detailed results

Runs results are summarized in Table 1.

Errors have been only detected with the erase write test sequence (x=2) and consists in very few cells errors (SEUs only) and 4 large errors (2 with few consecutive write buffers in error, 2 with 1 or consecutive write buffer time in error (fill time limit set to 10ms, erase time limit set to 4s).

DUTs failed after several runs performed with the erase write sequence (x=2) and it is likely related to the generated internal high voltage and cumulative dose.

No SEL was detected at Vcc/Vccq max and a temperature of 85°C.

Table 1: Detailed SEE results.

Facility	dut_medium	test_mode	power_config	run_number	Facility_run_number	DUT_under_beam	board_id	interface_comment	temperature	Proton energy MeV	run_duration	entered_fluence	SEL Vcc	SEL Vccq	SEU read	SEU cell	SEU buf_r	bu_fw write	buf_w read	fill error	erase error	Comment
PIF	air	SEU	2.7V	44	29	1	10	x=1	room	200	960	2.00E+11	0	0	0	0	0	0	0	0	0	
PIF	air	SEU	2.7V	45	30	1	10	x=3	room	200	958	2.00E+11	0	0	0	0	0	0	0	0	0	
PIF	air	SEU	2.7V	46		1	10	x=5	room	200		no	0	0	0	0	0	0	0	0	0	
PIF	air	SEU	2.7V	**47**	31	2	10	x=2	room	200	979	2.00E+11	0	0	0	3	0	0	0	0	0	
PIF	air	SEU	2.7V	**48**	32	2	10	x=2	room	150	1163	2.00E+11	0	0	0	1	0	0	0	0	0	
PIF	air	SEU	2.7V	**49**	33	2	10	x=2	room	100	1419	1.74E+11	0	0	0	0	0	0	0	1	0	dut failed at fluence 5.93E+10
PIF	air	SEU	2.7V	55	37	1	11	x=1	room	200	997	2.00E+11	0	0	0	0	0	0	0	0	0	
PIF	air	SEU	2.7V	56	38	1	11	x=3	room	200	992	2.00E+11	0	0	0	0	0	0	0	0	0	
PIF	air	SEU	2.7V	57		1	11	x=5	room	200		no	0	0	0	0	0	0	0	0	0	
PIF	air	SEU	2.7V	**51**	34	2	11	x=2	room	100	1626	2.00E+11	0	0	0	1	0	0	0	0	0	
PIF	air	SEU	2.7V	**52**	35	2	11	x=2	room	150	1174	2.00E+11	0	0	0	1	0	1	0	0	0	
PIF	air	SEU	2.7V	**53**	36	2	11	x=2	room	200	782	1.58E+11	0	0	0	0	0	0	0	0	0	dut failed at fluence 4.36E+10
PIF	air	SEU	2.7V	61	41	1	12	x=2	room	200	988	2.00E+11	0	0	0	0	0	0	0	0	0	
PIF	air	SEU	2.7V	62	42	1	12	x=2	room	150	1174	2.00E+11	0	0	0	0	0	0	0	0	0	
PIF	air	SEU	2.7V	**58**	39	2	12	x=2	room	100	1652	2.00E+11	0	0	0	1	0	1	0	1	0	
PIF	air	SEU	2.7V	**59**	40	2	12	x=2	room	150	1176	2.00E+11	0	0	0	0	0	0	0	0	0	dut failed at fluence 1.8E+11
PIF	air	SEL	3.6V	65	43	1	13	x=6	85	200	990	2.00E+11	0	0	-	-	-	-	-	-	-	
PIF	air	SEL	3.6V	67	44	2	13	x=6	85	200	987	2.00E+11	0	0	-	-	-	-	-	-	-	

The cumulative dose with X=2 (erase/write) received up to DUT failure is provided in the table below

DUT no	Board	Total dose (X=2) rad (Si)
2	10	3.13E+04
2	11	3.53E+04
2	12	3.14E+04

9 Glossary

DUT: Device under test.

Fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.
In this document, Fluence is expressed in ions per cm².

Flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.
In this document, Flux is expressed in ions per cm².s.

Single-Event Effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.
Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL).

Single Event Gate Rupture (SEGR) **/ Single Event Dielectric Rupture (**SEDR**):** Destructive rupture of the gate oxide layer or dielectric layer by a single ion strike. This leads to leakage currents under bias and can be observed as stuck bits in digitals devices

Single-Event Upset (SEU)**:** A soft error caused by the transient signal induced by a single energetic particle strike.

Single-Event Transient (SET): A transient signal induced by a single energetic particle strike.

Single-Event Latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.
SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.
An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

Single-Event Functional Interrupt (SEFI): A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single-event burnout (SEB).
A SEFI is often associated with an upset in a control bit or register.

Error cross-section: the number of errors per unit fluence. For device error cross-section, the dimensions are cm² per device. For bit error cross-section, the dimensions are cm² per bit.

Tilt angle: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis

Weibull fit: $F(x) = A (1- \exp\{-[(x-x_0)/W]^s\})$ with:

x = effective LET in MeV/(mg/cm^2);
$F(x)$ = SEE cross-section in cm^2;
A = limiting or plateau cross-section;
x_0 = onset parameter, such that $F(x) = 0$ for $x < x_0$;
W = width parameter;
s = a dimensionless exponent.

Error bars: error bars are computed using a confidence level of 95% and a beam flux uncertainty of +/- 10% as recommended by Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100.

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