Single Event Effects

Proton Test Report

Test type	Single-Event Upset, Single Event Latchup
Part Reference	MX30LF4G18AC
Tested function	NAND Flash Memory
Chip manufacturer	Macronix
Test Facility	PIF, Paul Scherrer Institute (PSI), Villigen, Switzerland
Test Date	November 2017
Customer	ESA ESTEC

BCE 5524

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1 Introduction

This report presents results of SEE test campaign for the Macronix NAND Flash Memory MX30LF4G18AC. 12 parts were made available for this. The test campaigns took place at PIF, Paul Scherrer Institute (PSI), Villigen, Switzerland in November 2017.

2 Applicable and Reference Documents

Applicable Documents

AD-1 Macronix MX30LFxG18AC Datasheet, Revision 1.3 (July, 10, 2015)
AD-2 MX30LF4G18AC physical analysis HRX/RCA/00110

Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100
RD-2. Proton Irradiation Facility at the PROSCAN project of the Paul Scherrer Institute PIF facility at PSI, Ulrike Grossner, Wojtek Hajdas, Ken Egli, Roger Brun, and Reno Harboe-Sorensen, RADECS 2009.

3 Device Information

Device description

MX30LF4G18AC, NAND Flash Memory

Manufacturer:	Macronix
Package:	TSOP48 12 x 20 mm
Marking:	MXIC S144411 MX30LF4G18AC-TI 84112708
Date code	1444
Technology :	CMOS
Die dimensions :	6.9 mm x 7.4 mm

This 4Gb memory is composed of 2 planes of 2048 blocks. Each block is organized in 64 pages of 2048 bytes with 64 additional bytes.

Device and die identification

Figure 1: Package, top.

Figure 2: Package, bottom.

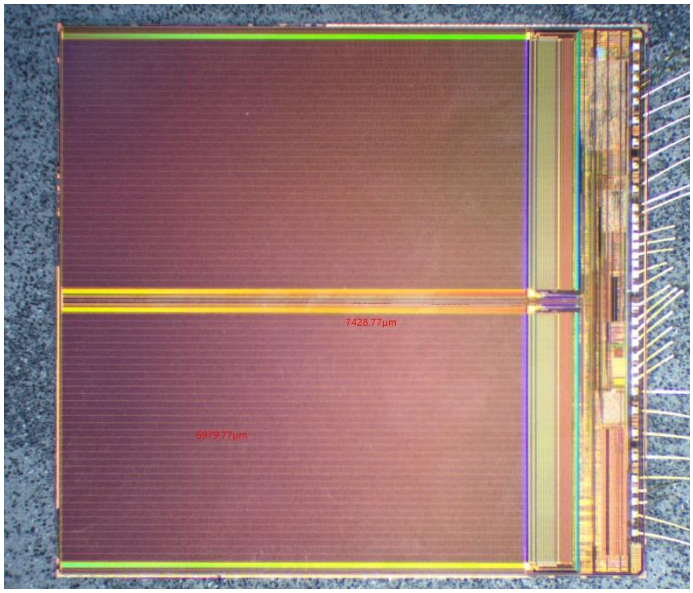


Figure 3: Die dimensions.

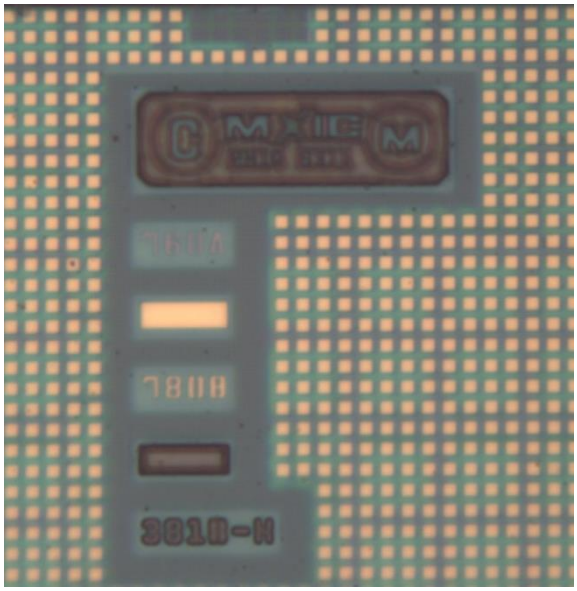


Figure 4: Die marking.

4 Test Setup

Figure 5 shows the principle of the single event test system.
The test system is based on a Virtex4 FPGA (Xilinx). It runs at 50 MHz. The test board has 271 I/Os which can be configured using several I/O standards.
The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 24 independent channels.
The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.
SEL event is detected when the supply current is over a configurable threshold (typically 5 to 10 times the nominal current) and processed:
Once detected, SEL state is maintained for typically 1 or 2ms and power supplies are cut off during a wait time of typically 1 s. These times are configurable.
Each power supply under supervision is monitored independently for SEL detection and processing but subsequent cut off is performed on all power supplies.

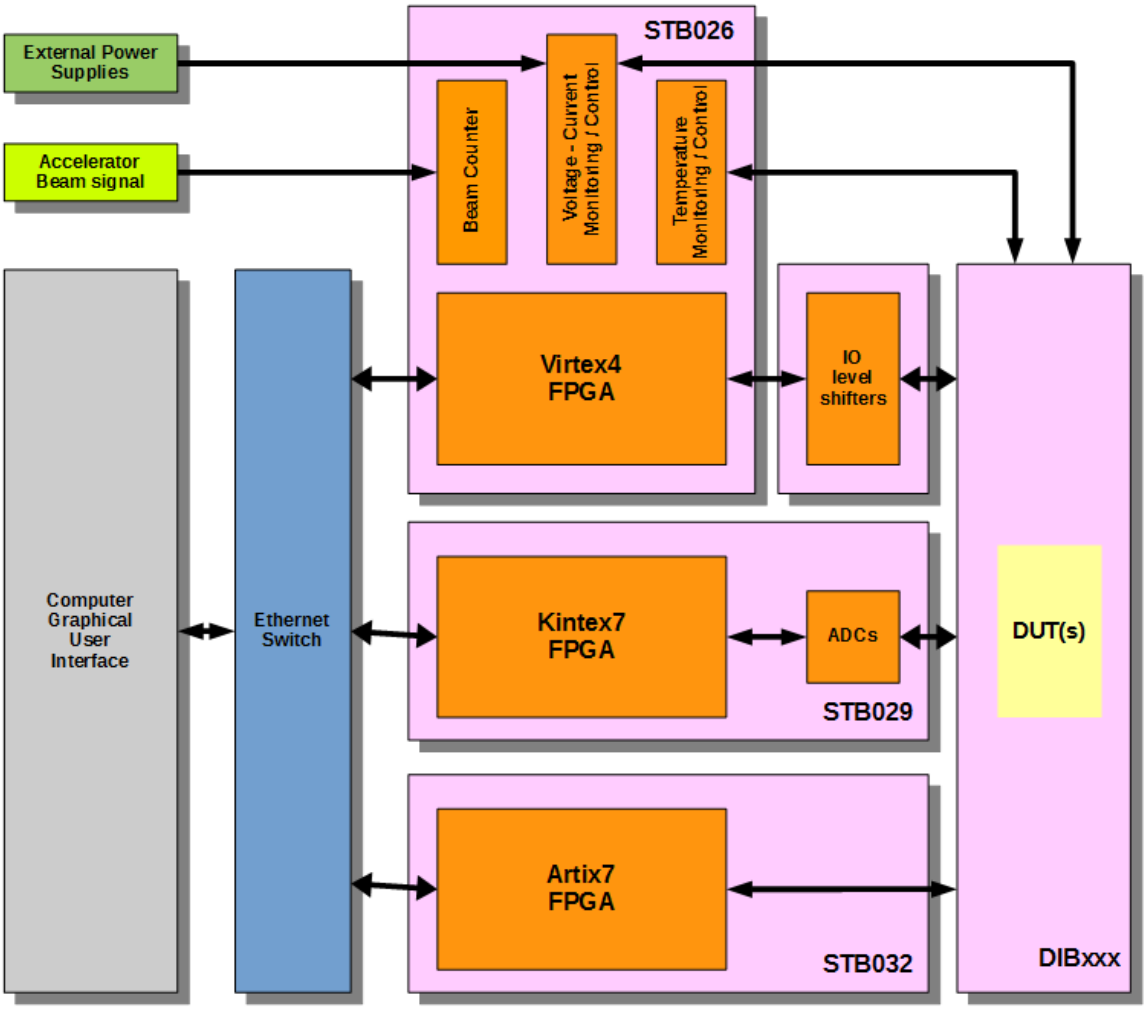


Figure 5: Hirex SEE test setup

A daughter board with 4 samples mounted on it has been used for this test (DIB299A) and Figure 6 show a picture this board drawing.

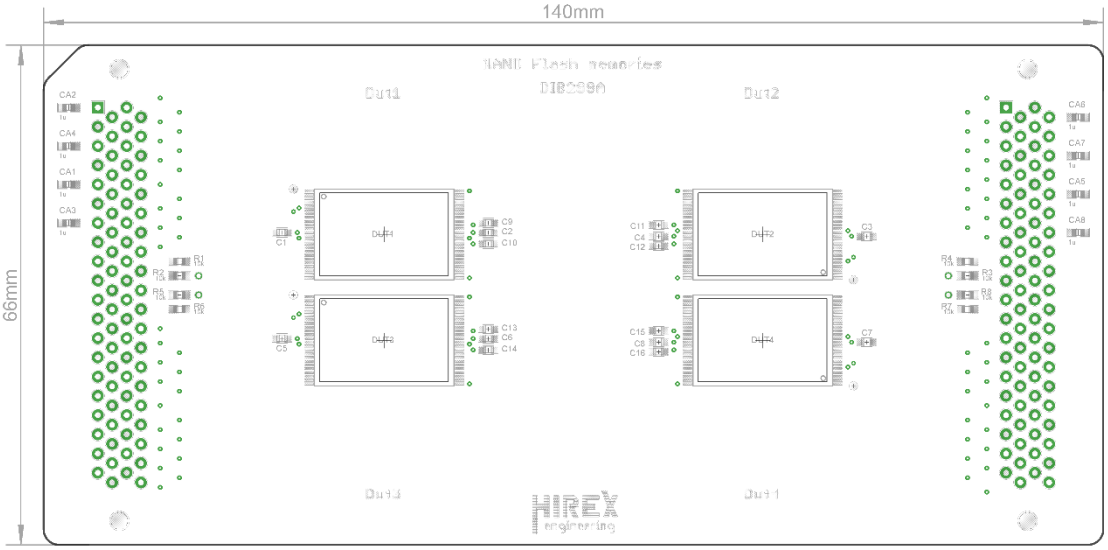


Figure 6 – DIB299A ONFI flash daughter board

5 Test sequence

Test modes and their sequence used during the test campaign are summarized inFigure 7. Operations in grey boxes are performed before the irradiation. Operation in blue boxes are performed under irradiation and operations in yellow boxes are performed once the beam is stopped at the end of the run.

Both static and dynamic results can be extrapolated based on a single run result. This is done by considering 100 blocks for dynamic behaviour and the rest of the chip for static behaviour.

Fill memory sequence

All DUT blocks are erased, then the first 100 blocks are written with complementary pattern 0x66/0x99, the remaining 3996 blocks are written with complementary pattern 0x55/0xAA

Off sequence

The DUT is turned off. It is then turned back on once the total fluence has been reached and the 3996 blocks are read.

Read sequence

The read sequence consists in a loop of a read operation followed by a power-cycle and a second read operation. This sequence focuses on the same 100 blocks of the memory. The pattern used is a complementary pattern (0x66 and 0x99) for this dynamic test. Upon completion of the beam exposure the 3996 remaining blocks are read.

Erase/Write sequence

During the erase/write (E/W) sequence, the same 100 blocks are erased and then written under the beam flux. The pattern used is a complementary pattern (0x66 and 0x99) for this dynamic test These operations are then looped for the duration of the run. Upon completion of the beam exposure the 3996 remaining blocks are read.

Both static and dynamic results can be extrapolated based on a single run result. This is done by considering 100 blocks for dynamic behaviour and the rest of the chip for static behaviour.

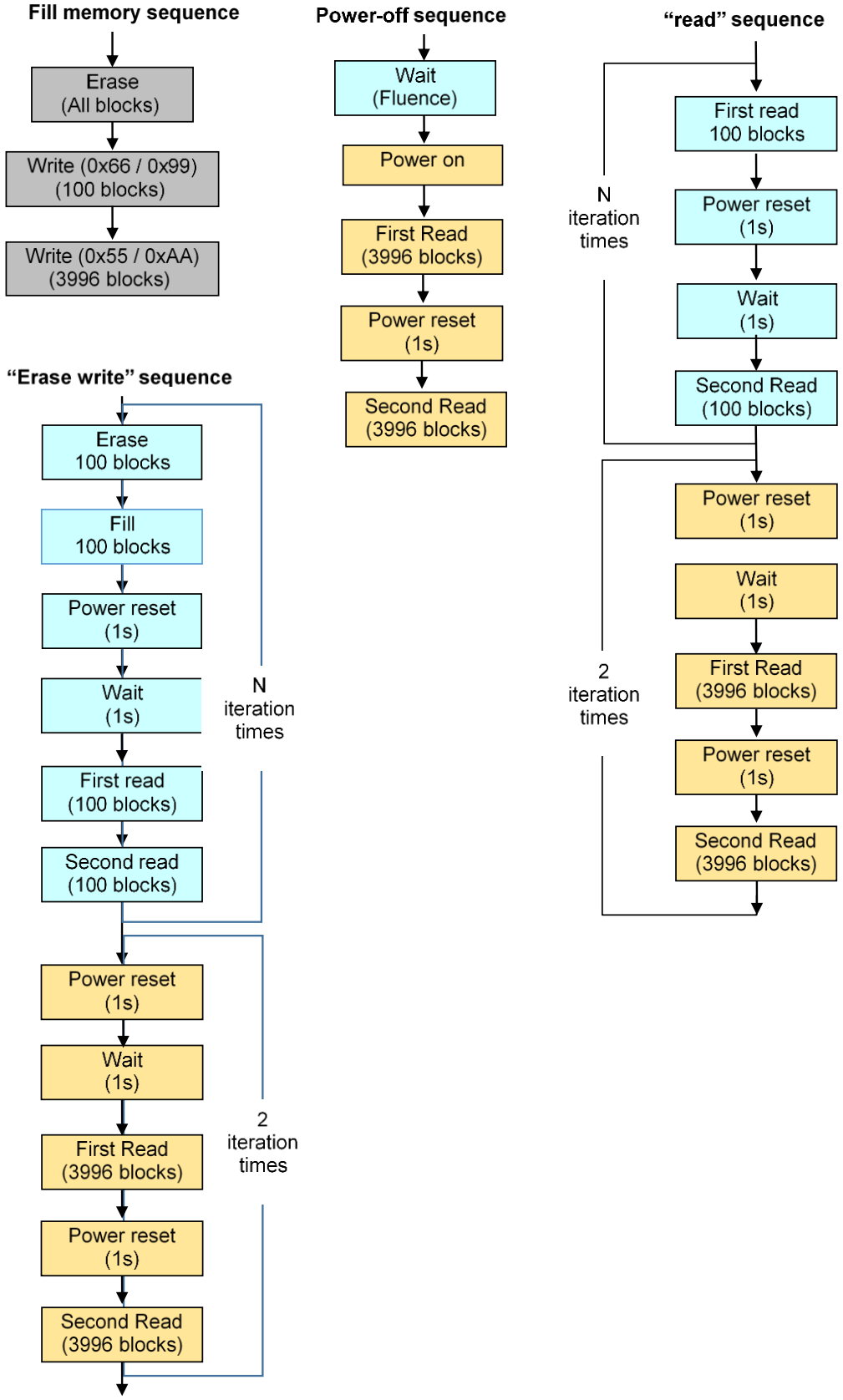


Figure 7 – Test run sequences

6 PIF Test Facility

A description of PIF test facility can be found in RD-2. As shown in Figure 8, proton beam from COMET cyclotron is delivered to the experimental PIF cave with an input energy that can be varied from few MeVs up to 250 MeV. Then in PIF room, local copper degraders can be inserted into the beam to obtain the different user energies.

200 MeV input beam's energy was selected and calibrated. The different proton beam have been obtained with the use of degraders.

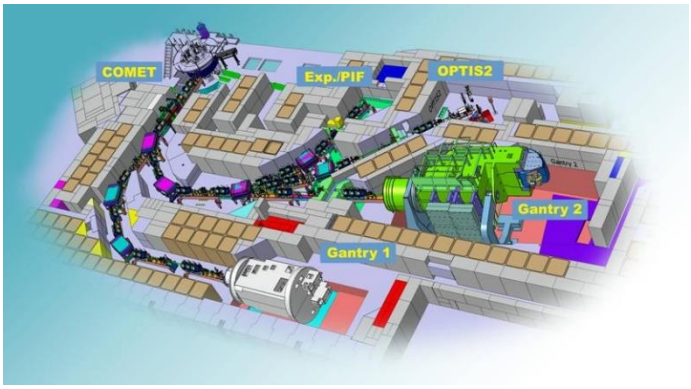


Figure 8 - Proscan facility

7 Test conditions.

SEU tests were carried out at Vddmin (2.7 V) and room temperature.
Samples for SEL were tested at Vddmax (3.6 V) and a junction temperature of 85°C while performing a static test.

8 Results

Detailed run results are presented in Table 3.

Dynamic test section of Table 3

Column headline	Description
first block	first block tested from the 100 blocks
last block	last block teste from the 100 blocks
nb_blocks	number of blocks tested
nb errors r1and r2	number of errors at 1st read **and** 2nd read
1st read	number of errors at first read
2nd read	number of errors at second read
Initial	number of errors read before exposure
Final	number of errors read after exposure
1st read – initial	number of errors at first read minus number of errors read before exposure
Capacity	Number of words monitored
"Dynamic cell SEU cross-section/word"	(first read minus initial)/entered fluence/capacity
logic error	Pages/blocks errors

Static test section of Table 3

Column headline	Description
first block	first block tested from the 3996 blocks
last block	last block teste from the 3996 blocks
nb_blocks off	number of bad blocks skipped
Nb blocks	Actual number of blocks monitored
capacity	Number of words monitored
1st read	number of errors at first read
2nd read	number of errors at second read
cumul fluence cells static	Fluence cumulated since power fill memory
Static cell SEU cross-section/word	First read/cumul fluence/capacity

For SEL, two samples have been tested with a proton energy of 200MeV and no SEL has been detected with a fluence of 1 10+11 protons / cm² at a case temperature of 85°C. Sample supply currents chronograms are shown in Figure 12 and Figure 13 together with temperature control monitoring and flux monitoring.

For SEU and for each sample at a given proton energy, the test runs sequence has consisted after an erase and write of the full memory by a power off test run, followed by a read test run and then an erase and write / read test run.
Very few logic errors have been detected. Logic error descriptions are given in Table 1.

Table 1 – Logic errors

Run number	Test mode	Logic error description
Run015	Read	**Block 62 in error**: At stepid112 (1st read) and stepid113 (2nd read), in block62, 16 first words in the 16 first pages read to 0x00 stepid number of words in error / block threshold reached (set to 256)
Run024	Read	**Block 86 in error**: At stepid417 (1st read) and stepid418 (2nd read), in block86, 16 first words in the 16 first pages read to 0x00 (stepid number of words in error / block threshold reached (set to 256) **Block 83 in error**: At stepid603 (2nd read) in block83, 16 first words in the 16 first pages read to 0x00 Stepid number of words in error / block threshold reached (set to 256)
Run025	Write/Read	**Block 0 in error**: At stepid2193 (1st read) and stepid2194 (2nd read), in block0, 16 first words in the 16 first pages read to 0x00 Stepid number of words in error / block threshold reached (set to 256)
Run028	Read	At stepid248 (2nd read) in the first 99 blocks in all pages, address 2031 (0x07EF) read to 0xFF

Figure 9 gives the SEU cross-section / word as a function of proton energy for the different test modes, (static, read and write / read). It can be observed that there is no significant variation with the proton energy.

With regards to SEU, most of the errors are SBUs (1 bit in the word in error) and bit flip are 0 to 1 (charge loss) for static tested blocks as shown in as an example.
It can also be observed that word errors increased in a non-linear way after each run of the test sequence, each run having the same test fluence. As an example, this can be observed with the test sequence (power off, read and read write) performed at run006, 007 and 008 on board1 / dut1 (see Table 3): the errors on the static tested cells increase by 3194, 12980 and 109870 respectively. This could mean that cells can lose some charge but not sufficiently to flip at the first hit but flip will occur with one other hit in the subsequent runs.

Lastly Figure 10 show the number of word errors versus the page number (all blocks cumulated). It can be observed that the last 2 pages, 62 and 63, are more sensitive that the other pages. Figure 11 shows also an increase of the SEU sensitivity of the blocks block versus the block number.

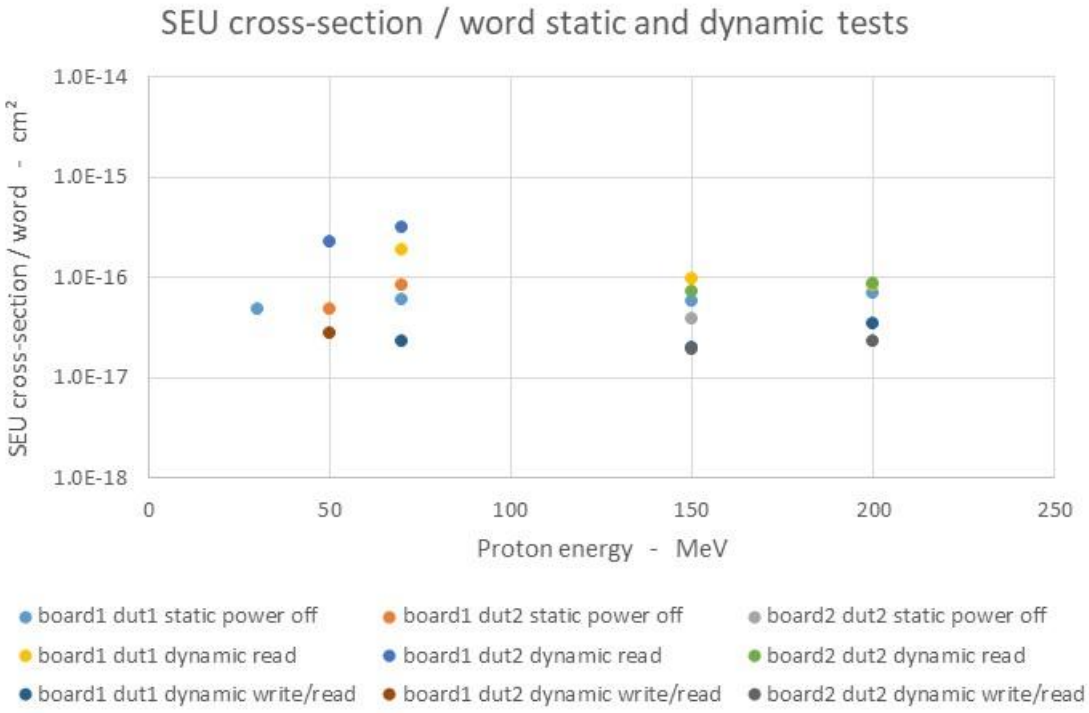


Figure 9 – SEU cross-section / word, static and dynamic tests

Table 2: Detailed data analysis, board1 DUT1, 70MeV proton energy, static cells .

		word errors	sbu	mbu2	bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7	trans 1->0	trans 0->1
run006	first read	3196	3195	1	403	415	404	380	388	367	400	440	1	3196
run006	second read	3193	3192	1	398	409	405	386	389	363	396	448	0	3194
run007	first read	12995	12991	4	1791	1587	1594	1550	1528	1515	1600	1834	0	12999
run007	second read	12980	12975	5	1815	1570	1606	1541	1516	1502	1600	1835	0	12985
run008	first read	110779	110579	199	19222	11973	12132	11709	11703	11914	11801	20527	0	110981
run008	second read	109870	109681	188	19095	11868	12011	11646	11634	11798	11770	20239	0	110061

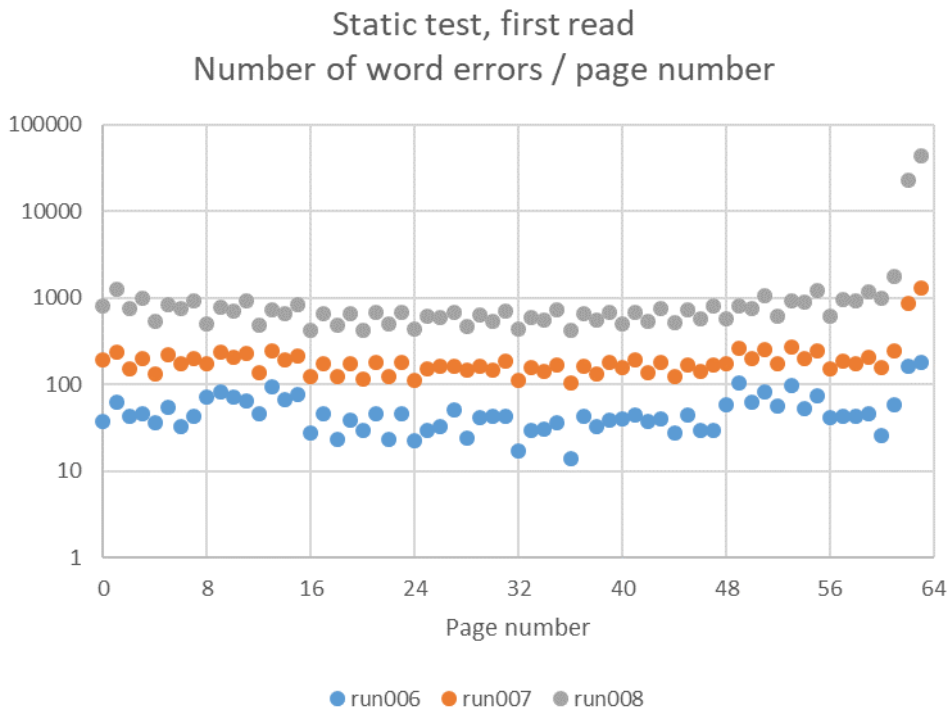


Figure 10 – Number of word errors versus page number, static test, first read, run006,7 & 8

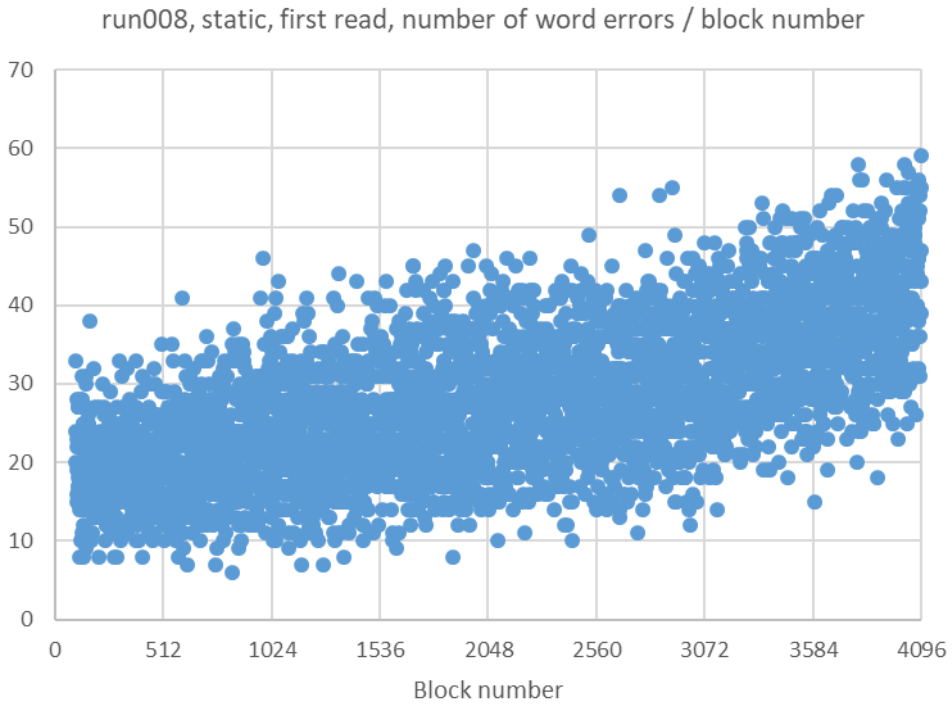
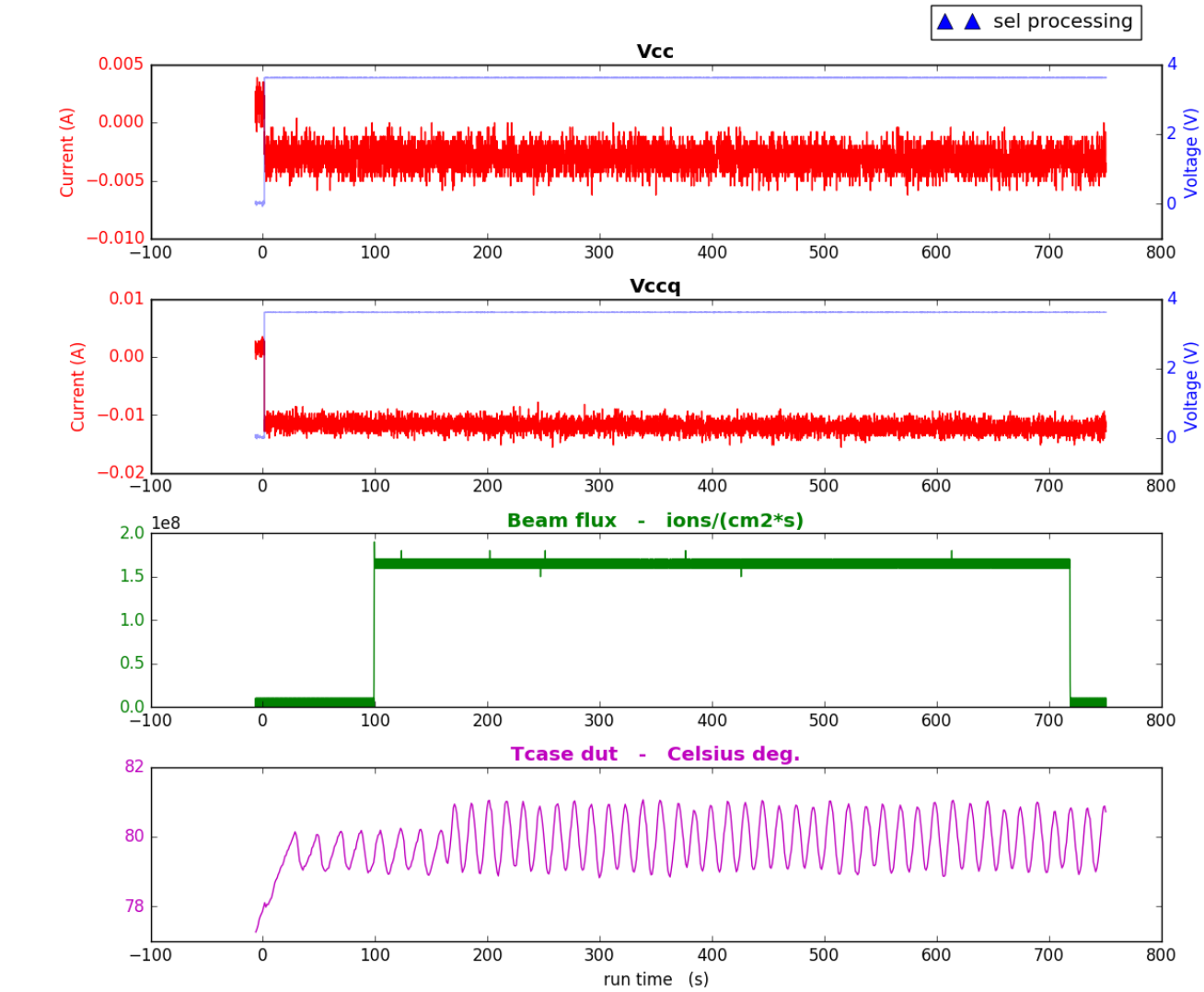


Figure 11 – Number of word errors versus block number, static test, first read, run008

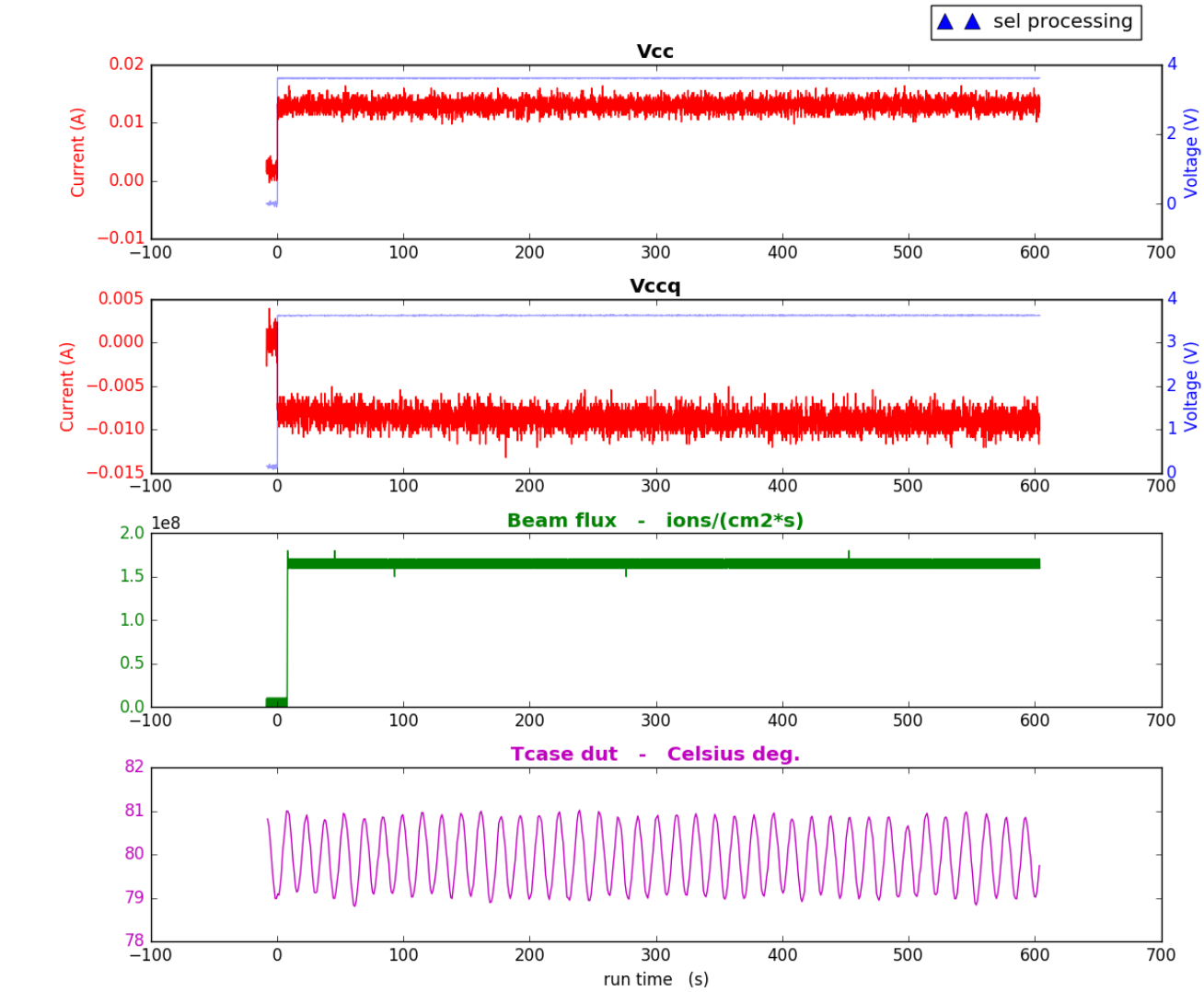
Table 3: Detailed SEE results.

												Dynamic												static								
Facility	dut_medium	run_number	Facility_run_number	board_id	DUT_partnumber	test_mode	temperature	proton energy	run_duration	entered_fluence	sel	first block	last block	nb_blocks	nb errors r1and r2	1st read	2nd read	initial	final	1st read - initial	capacity	Dynamic cell SEU cross-section/word	logic error	first block	last block	nb Block off	nb_blocks	capacity	1st read	2nd read	cumul fluence cells static	Static cell SEU cross-section/word
PIF	air			1	1	Fill memory																										
PIF	air	6	12	1	1	PowerOFF	70	1300	1.00E+11	0	-	-	-	-	-	-	-	-	-	-	-	-	100	4095	23	3973	537022464	3197	3194	1.0E+11	6.0E-17
PIF	air	7	13	1	1	Read	70	1359	1.00E+11	0	0	99	100	323	305	310	51	256	254	13516800	1.9E-16	0	100	4095	23	3973	537022464	12995	12980	2.0E+11	1.2E-16
PIF	air	8	14	1	1	ReadWrite	70	1348	1.00E+11	0	0	99	100	46	37	41	6	6	31	13516800	2.3E-17	0	100	4095	23	3973	537022464	110779	109870	3.0E+11	6.9E-16
PIF	air			1	1	Fill memory																										
PIF	air	10	15	1	1	PowerOFF	150	629	1.00E+11	0	-	-	-	-	-	-	-	-	-	-	-	-	100	4095	23	3973	537022464	3195	3189	1.0E+11	5.9E-17
PIF	air	11	16	1	1	Read	150	627	1.00E+11	0	0	99	100	190	176	173	46	150	130	13516800	9.6E-17	0	100	4095	23	3973	537022464	9115	9074	2.0E+11	8.5E-17
PIF	air	12	17	1	1	ReadWrite	150	628	1.00E+11	0	0	99	100	47	35	43	8	7	27	13516800	2.0E-17	0	100	4095	23	3973	537022464	21150	21098	3.0E+11	1.3E-16
PIF	air			1	1	Fill memory																										
PIF	air	14	18	1	1	PowerOFF	200	553	1.00E+11	0	-	-	-	-	-	-	-	-	-	-	-	-	100	4095	23	3973	537022464	3836	3824	1.0E+11	7.1E-17
PIF	air	15	19	1	1	Read	200	551	1.00E+11	0	0	99	100	192	173	186	57	157	116	13516800	8.6E-17	1	100	4095	23	3973	537022464	10204	10134	2.0E+11	9.5E-17
PIF	air	16	20	1	1	ReadWrite	200	552	1.00E+11	0	0	99	100	70	54	58	7	7	47	13516800	3.5E-17	0	100	4095	23	3973	537022464	22819	22734	3.0E+11	1.4E-16
PIF	air			1	1	Fill memory																										
PIF	air	18	21-23	1	1	PowerOFF	30		1.00E+11	0	-	-	-	-	-	-	-	-	-	-	-	-	100	4095	23	3973	537022464	2656	2665	1.0E+11	4.9E-17
PIF	air	20	24	1	1	PowerOFF	50	1697	1.00E+11	0	-	-	-	-	-	-	-	-	-	-	-	-	100	4095	23	device failed					
PIF	air			1	2	Fill memory																										
PIF	air	23	25	1	2	PowerOFF	50	1694	1.00E+11	0			-	-	-	-	-	-	-	-	-	-	100	4095	25	3971	536752128	2562	2596	1.0E+11	4.8E-17
PIF	air	24	26	1	2	Read	50	1690	1.00E+11	0	0	99	100	409	393	394	89	341	304	13516800	2.2E-16	2	100	4095	25		forgot to check blocks			2.0E+11	-
PIF	air	25	27	1	2	ReadWrite	50	1692	1.00E+11	0	0	99	100	53	39	44	1	1	38	13516800	2.8E-17	1	100	4095	25	3971	536752128	730675	714798	3.0E+11	4.5E-15
PIF	air			1	2	Fill memory																										
PIF	air	27	32	1	2	PowerOFF	70	1287	1.00E+11	0	-	-	-	-	-	-	-	-	-	-	-	-	100	4095	25	3971	536752128	4474	4426	1.0E+11	8.3E-17
PIF	air	28	33	1	2	Read	70	1248	1.00E+11	0	0	99	100	526	506	502	78	416	428	13516800	3.2E-16	1	100	4095	25	3971	536752128	23900	23627	2.0E+11	2.2E-16
PIF	air	29	34	1	2	ReadWrite	70	1249	1.00E+11	0	0	99	100	device failed										100	4095	25	device failed					
PIF	air			2	2	Fill memory																										
PIF	air	33	35	2	2	PowerOFF	200	620	1.00E+11	0	-	-	-	-	-	-	-	-	-	-	-	-	100	4095	33		forgot to check blocks			1.0E+11	-
PIF	air	35	36	2	2	Read	200	621	1.00E+11	0	0	99	100	177	167	170	50	148	117	13516800	8.7E-17	0	100	4095	33	3963	535670784	5636	5636	2.0E+11	5.3E-17
PIF	air	36	37	2	2	ReadWrite	200	621	1.00E+11	0	0	99	100	53	33	44	1	2	32	13516800	2.4E-17	0	100	4095	33	3963	535670784	13124	13057	3.0E+11	8.2E-17
PIF	air			2	2	Fill memory																										
PIF	air	38	38	2	2	PowerOFF	150	708	1.00E+11	0	-	-	-	-	-	-	-	-	-	-	-	-	100	4095	33	3963	535670784	2050	2030	1.0E+11	3.8E-17
PIF	air	39	39	2	2	Read	150	707	1.00E+11	0	0	99	100	155	143	144	45	122	98	13516800	7.3E-17	0	100	4095	33	3963	535670784	6321	6308	2.0E+11	5.9E-17
PIF	air	40	40	2	2	ReadWrite	150	712	1.00E+11	0	0	99	100	43	27	40	1	2	26	13516800	1.9E-17	0	100	4095	33	3963	535670784	14805	14782	3.0E+11	9.2E-17
PIF	air			4	2	Fill memory																										
PIF	air	49	41	4	2	Reset	85	200	619	1.00E+11	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PIF	air			4	1	Fill memory																										
PIF	air	50	42	4	1	Reset	85	200	620	1.00E+11	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-



RUN049

Figure 12: Run049, chronograms for Vcc and Vccq lines along with temperature and flux.



RUN050

Figure 13: Run050, chronograms for Vcc and Vccq lines along with temperature and flux.

9 Glossary

DUT: Device under test.

Fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.
In this document, Fluence is expressed in ions per cm².

Flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.
In this document, Flux is expressed in ions per cm².s.

Single-Event Effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.
Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL).

Single Event Gate Rupture (SEGR) **/ Single Event Dielectric Rupture (**SEDR**):** Destructive rupture of the gate oxide layer or dielectric layer by a single ion strike. This leads to leakage currents under bias and can be observed as stuck bits in digitals devices

Single-Event Upset (SEU)**:** A soft error caused by the transient signal induced by a single energetic particle strike.

Single-Event Transient (SET): A transient signal induced by a single energetic particle strike.

Single-Event Latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.
SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.
An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

Single-Event Functional Interrupt (SEFI): A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single-event burnout (SEB).
A SEFI is often associated with an upset in a control bit or register.

Error cross-section: the number of errors per unit fluence. For device error cross-section, the dimensions are cm² per device. For bit error cross-section, the dimensions are cm² per bit.

Tilt angle: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis

Weibull fit: $F(x) = A\,(1- \exp\{-[(x-x_0)/W]^s\})$ with:

x = effective LET in MeV/(mg/cm²);
F(x) = SEE cross-section in cm²;
A = limiting or plateau cross-section;
x_0 = onset parameter, such that $F(x) = 0$ for $x < x_0$;
W = width parameter;
s = a dimensionless exponent.

Error bars: error bars are computed using a confidence level of 95% and a beam flux uncertainty of +/- 10% as recommended by Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100.