Single Event Effects

Proton Test Report

Test type	Single-Event Upset, Single Event Latchup
Part Reference	TC58NVG2S0HTAI0
Tested function	NAND Flash Memory
Chip manufacturer	Toshiba
Test Facility	PIF, Paul Scherrer Institute (PSI), Villigen, Switzerland
Test Date	November 2017
Customer	ESA ESTEC

BCE 5524

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1 Introduction

This report presents results of SEE test campaign for the Toshiba NAND Flash Memory TC58NVG2S0HTAI0. 8 parts were made available for this. The test campaigns took place at PIF, Paul Scherrer Institute (PSI), Villigen, Switzerland in November 2017.

2 Applicable and Reference Documents

Applicable Documents

AD-1 TOSHIBA TC58NVG2S0HTAI0 Datasheet, Revision 1.0 (July, 05, 2013)
AD-2 TC58NVG2S0HTAI0 physical analysis HRX/RCA/00109

Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100
RD-2. Proton Irradiation Facility at the PROSCAN project of the Paul Scherrer Institute PIF facility at PSI, Ulrike Grossner, Wojtek Hajdas, Ken Egli, Roger Brun, and Reno Harboe-Sorensen, RADECS 2009.

3 Device Information

3.1 Device description

TC58NVG2S0HTAI0, NAND Flash Memory

Manufacturer:	Toshiba
Package:	TSOP48
Marking:	TOSHIBA NH2156 TAIWAN 1509 9AE
Date code	1509
Technology:	CMOS
Die dimensions:	4.9 mm x 6.2 mm

This 4Gb memory is composed of 2048 blocks. Each block is organized in 64 pages of (4096 + 256) bytes.

3.2 Device and die identification

Figure 1: Package, top.

Figure 2: Package, bottom.

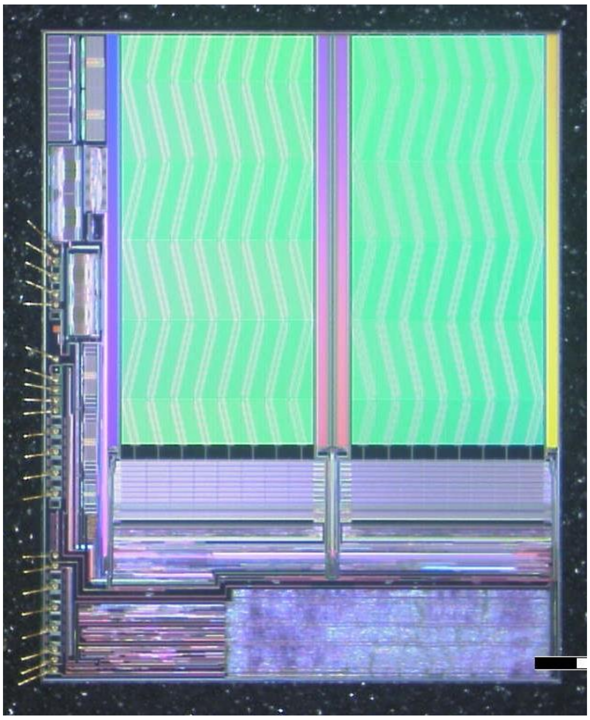

Figure 3: Die dimension.

Figure 4: Die marking.

4

5 Test Setup

Figure 5 shows the principle of the single event test system.

The test system is based on a Virtex4 FPGA (Xilinx). It runs at 50 MHz. The test board has 271 I/Os which can be configured using several I/O standards.

The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 24 independent channels.

The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.

SEL event is detected when the supply current is over a configurable threshold (typically 5 to 10 times the nominal current) and processed:

Once detected, SEL state is maintained for typically 1 or 2ms and power supplies are cut off during a wait time of typically 1 s. These times are configurable.

Each power supply under supervision is monitored independently for SEL detection and processing but subsequent cut off is performed on all power supplies.

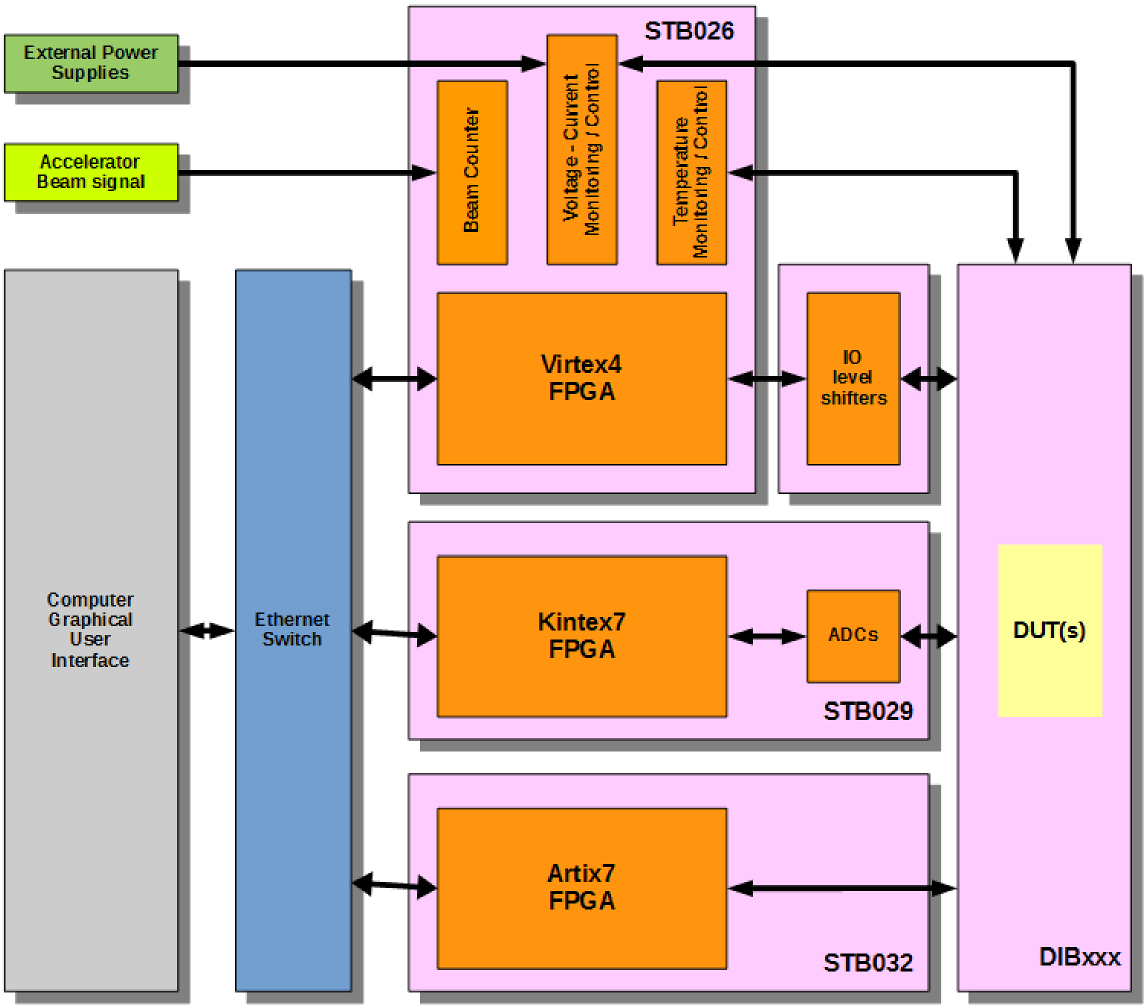

Figure 5: Hirex SEE test setup

A daughter board with 4 samples mounted on it has been used for this test (DIB299A) and Figure 6 show a picture this board drawing.

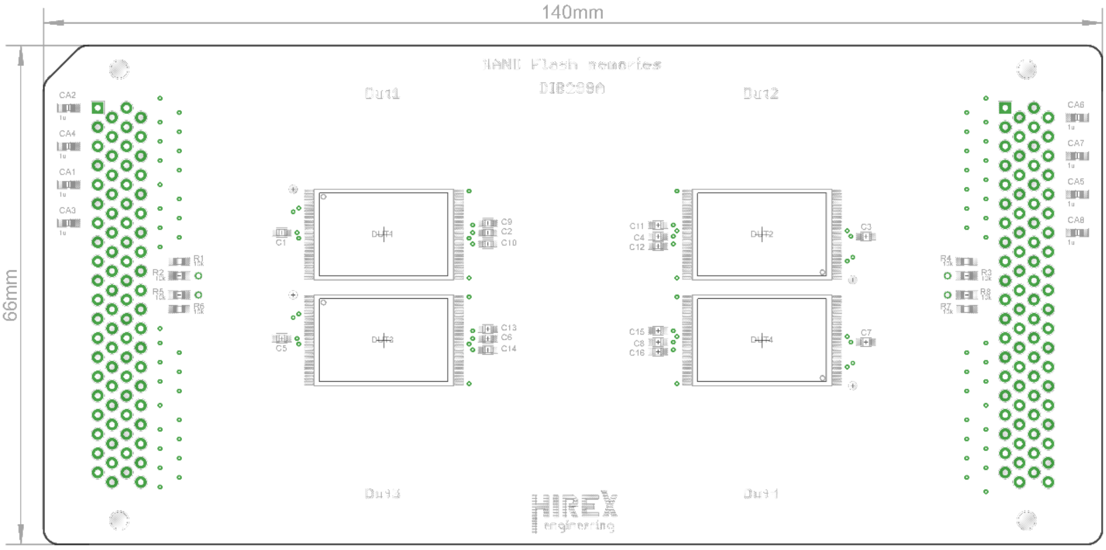

Figure 6 – DIB299A ONFI flash daughter board

6 Test sequence

Test modes and their sequence used during the test campaign are summarized inFigure 7. Operations in grey boxes are performed before the irradiation. Operation in blue boxes are performed under irradiation and operations in yellow boxes are performed once the beam is stopped at the end of the run.

Both static and dynamic results can be extrapolated based on a single run result. This is done by considering 100 blocks for dynamic behaviour and the rest of the chip for static behaviour.

Fill memory sequence

All DUT blocks are erased, then the first 100 blocks are written with complementary pattern 0x66/0x99, the remaining 3996 blocks are written with complementary pattern 0x55/0xAA

Off sequence

The DUT is turned off. It is then turned back on once the total fluence has been reached and the 3996 blocks are read.

Read sequence

The read sequence consists in a loop of a read operation followed by a power-cycle and a second read operation. This sequence focuses on the same 100 blocks of the memory. The pattern used is a complementary pattern (0x66 and 0x99) for this dynamic test. Upon completion of the beam exposure the 3996 remaining blocks are read.

Erase/Write sequence

During the erase/write (E/W) sequence, the same 100 blocks are erased and then written under the beam flux. The pattern used is a complementary pattern (0x66 and 0x99) for this dynamic test These operations are then looped for the duration of the run. Upon completion of the beam exposure the 3996 remaining blocks are read.

Both static and dynamic results can be extrapolated based on a single run result. This is done by considering 100 blocks for dynamic behaviour and the rest of the chip for static behaviour.

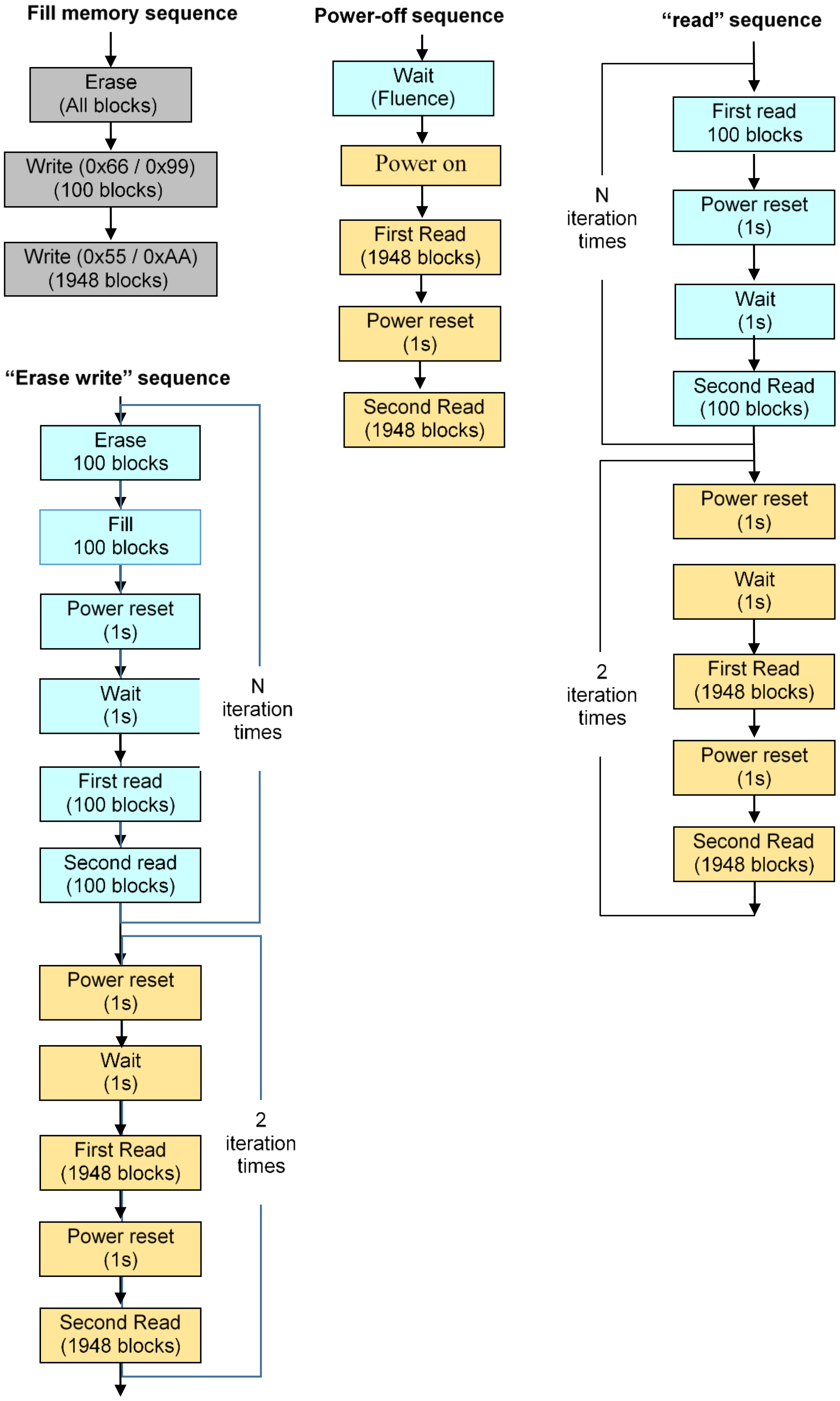

Figure 7 – Test run sequences

7 PIF Test Facility

A description of PIF test facility can be found in RD-2. As shown in Figure 8, proton beam from COMET cyclotron is delivered to the experimental PIF cave with an input energy that can be varied from few MeVs up to 250 MeV. Then in PIF room, local copper degraders can be inserted into the beam to obtain the different user energies.

200 MeV input beam's energy was selected and calibrated. The different proton beam have been obtained with the use of degraders.

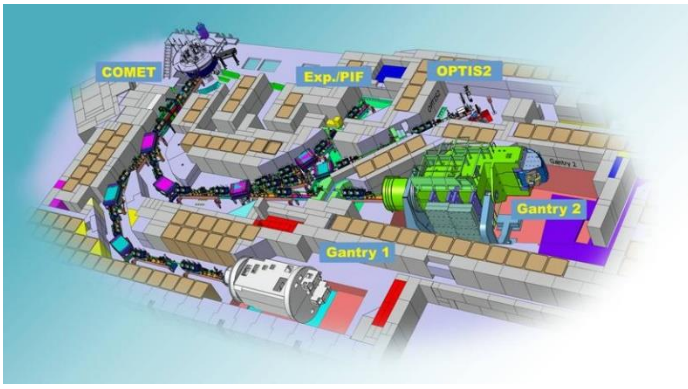

Figure 8 - Proscan facility

8 Test conditions.

SEU tests were carried out at Vddmin (2.7 V) and room temperature.
Samples for SEL were tested at Vddmax (3.6 V) and a junction temperature of 85°C while performing a static test.

9 Results

Detailed run results are presented in Table 3.

Dynamic test section of Table 3

Column headline	Description
first block	first block tested from the 100 blocks
last block	last block teste from the 100 blocks
nb_blocks	number of blocks tested
nb errors r1and r2	number of errors at 1st read **and** 2nd read
1st read	number of errors at first read
2nd read	number of errors at second read
Initial	number of errors read before exposure
Final	number of errors read after exposure
1st read – initial	number of errors at first read minus number of errors read before exposure
Capacity	Number of words monitored
"Dynamic cell SEU cross-section/word"	(first read minus initial)/entered fluence/capacity
logic error	Pages/blocks errors

Static test section of Table 3

Column headline	Description
first block	first block tested from the 1948 blocks
last block	last block tested from the 1948 blocks
nb_blocks off	number of bad blocks skipped
Nb blocks	Actual number of blocks monitored
capacity	Number of words monitored
1st read	number of errors at first read
2nd read	number of errors at second read
cumul fluence cells static	Fluence cumulated since power fill memory
Static cell SEU cross-section/word	First read/cumul fluence/capacity

For SEL, two samples have been tested with a proton energy of 200MeV and no SEL has been detected with a fluence of 1 10+11 protons / cm² at a case temperature of 85°C. Sample supply currents chronograms are shown in Figure 12 and Figure 13 together with temperature control monitoring and flux monitoring.

Erase/write/read test mode: 2 samples failed during this test condition and then usable dynamic test data could not be obtained

Very few logic errors have been detected. These errors consist in pages / blocks read mostly with data at 0x00 or 0xFF as shown in Table 1.

Table 1 – Logic errors

Run number	Test mode	Logic error description
Run010	Read	Dynamic: - at stepid247 to stepid288, block 0 in error, limit reach (512) data 0xFF
Run030	Erase /Write /Read	dynamic: - at stepid 323 &324, first read & second read, block 131 read to 0x00 limit block reached (256) - at stepid522, second read, 50 blocks read to 0x 00, limit block reached (256) for each block - at stepid 532 & 533, first read & second read, 70 blocks read to 0xFF limit block reached (256) for each block static: - 946 blocks in error, data=0xFF up to block error limit (512)

Figure 9 gives the SEU cross-section / word as a function of proton energy for the test modes static and dynamic (read) on board1 Dut1. It can be observed that there is there an increase in the cross-section / word with a proton energy decrease.

With regards to SEU, most of the errors are SBUs (1 bit in the word in error) and bit flip are 0 to 1 (charge loss) for static tested blocks as shown in Table 2 as an example.

Lastly Figure 10 show the number of word errors versus the page number (all blocks cumulated). It can be observed that the sensitivity increases with the page number. On the other hand, one can observe in Figure 11 that there is no significant variation of the number of errors as a function the block number.

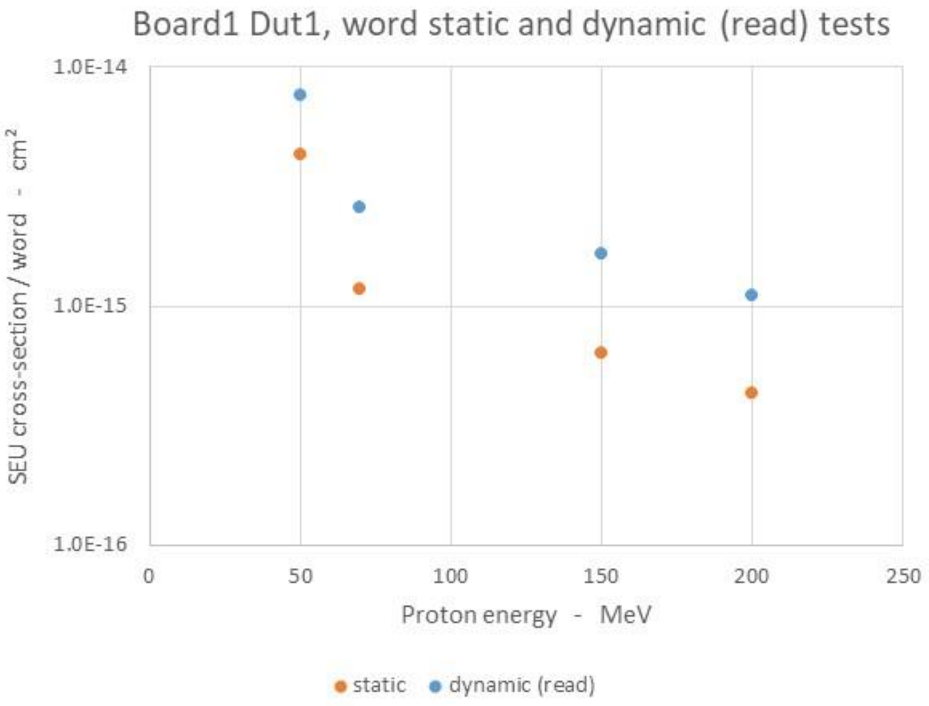

Figure 9 – SEU cross-section / word, static and dynamic tests

Table 2: Detailed data analysis, board1 DUT1, 50MeV proton energy, static cells .

	word errors	sbu	mbu2	mbu3	bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7	trans 1 -> 0	trans 0 -> 1
run014	98918	98768	144	6	10961	13306	12439	12876	12622	12640	13265	10965	181	98893

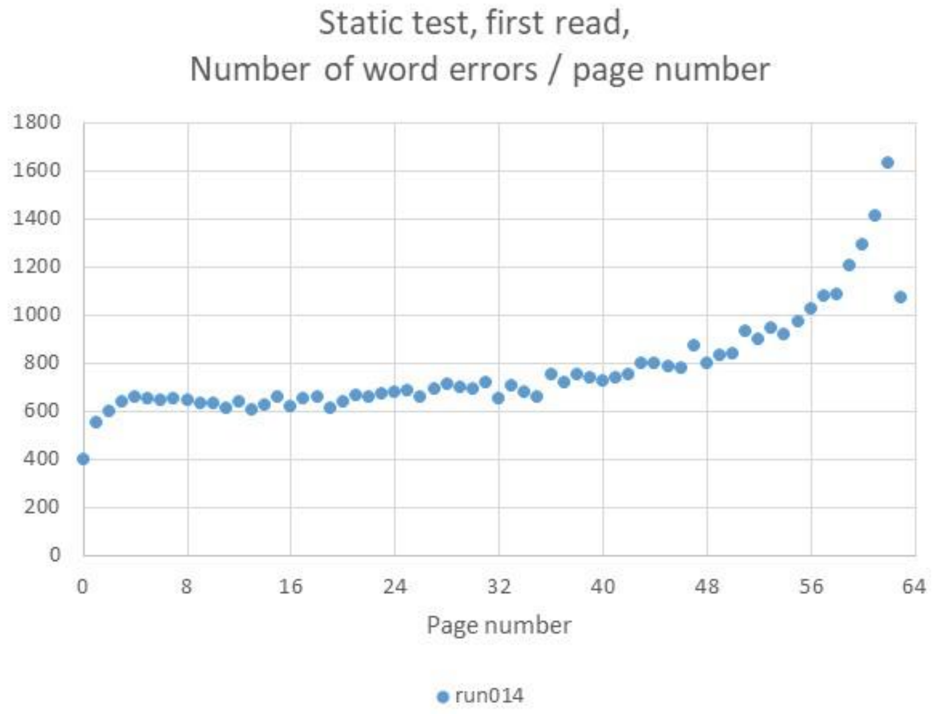

Figure 10 – Number of word errors versus page number, static test, first read, run014

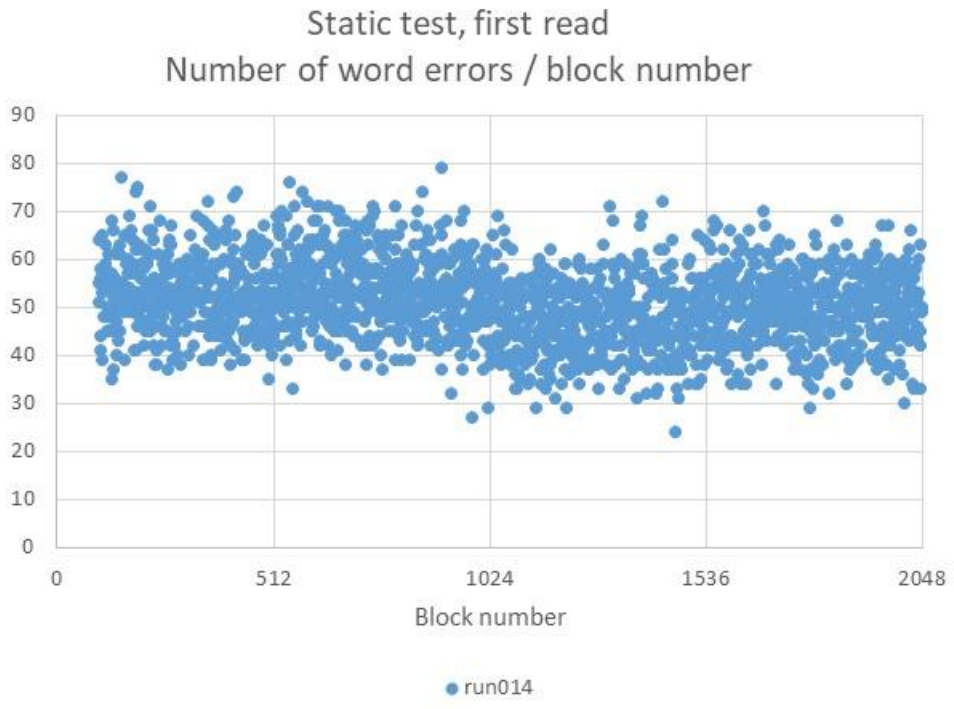

Figure 11 – Number of word errors versus block number, static test, first read, run014

Table 3: Detailed SEE results.

												Dynamic												static									
Facility	dut_medium	run_number	Facility_run_number	board_id	DUT_partnumber	test_mode	temperature	run_duration	entered_fluence	facility_comment	sel	first block	last block	nb_blocks	nb errors r1and r2	1st read	2nd read	initial	final	1st read - initial	capacity	Dynamic cell SEU cross-section/word	logic error	first block	last block	nb Block off	nb_blocks	capacity	1st read	2nd read	cumul fluence cells static	Static cell SEU cross-section/word	Comment
PIF	vacuum	2		1	1	FillMem																											
PIF	vacuum	3	44	1	1	PowerOFF		618	1.00E+11	200MeV		-	-	-	-	-	-	-	-	-	-	-	-	100	2047	24	1923	535609344	16575	16260	1.00E+11	3.1E-16	
PIF	vacuum	4	45	1	1	Read		617	1.00E+11	200MeV	0	0	99	100	3408	3937	3927	875	2350	3062	27852800	1.10E-15	0	100	2047	24	1923	535609344	46190	45368	2.00E+11	4.3E-16	
PIF	vacuum	5		1	1	FillMem																											
PIF	vacuum	6	46	1	1	PowerOFF		702	1.00E+11	150MeV		-	-	-	-	-	-	-	-	-	-	-	-	100	2047	24	1923	535609344	21578	21015	1.00E+11	4.0E-16	
PIF	vacuum	7	47	1	1	Read		698	1.00E+11	150MeV	0	0	99	100	5082	5684	5600	1076	3543	4608	27852800	1.65E-15		100	2047	24	1923	535609344	68305	67166	2.00E+11	6.4E-16	
PIF	vacuum	8		1	1	FillMem																											
PIF	vacuum	9	48	1	1	PowerOFF		1246	1.00E+11	70MeV		-	-	-	-	-	-	-	-	-	-	-	-	100	2047	24	1923	535609344	55907	54449	1.00E+11	1.0E-15	
PIF	vacuum	10	49	1	1	Read		393	3.16E+10	70MeV	0	0	99	100	8343	9168	9197	2875	5942	6293	27852800	7.15E-15	**1**	100	2047	24	1923	535609344	117100	114573	1.32E+11	1.7E-15	
PIF	vacuum	11		1	1	FillMem																											
PIF	vacuum	12	50	1	1	Read		872	6.06E+10	70MeV	0	0	99	100	4131	4483	4451	103	2013	4380	27852800	2.59E-15	0	100	2047	24	1923	535609344	38263	-	6.06E+10	1.2E-15	run010 continuation
PIF	vacuum	13		1	1	FillMem																											
PIF	vacuum	14	51	1	1	PowerOFF		1219	7.00E+10	50MeV		-	-	-	-	-	-	-	-	-	-	-	-	100	2047	24	1923	535609344	98918	-	7.00E+10	2.6E-15	
PIF	vacuum	16		1	1	FillMem																											
PIF	vacuum	17	52	1	1	Read		1212	7.00E+10	50MeV	0	0	99	100	14001	15190	15233	288	8930	14902	27852800	7.64E-15	0	100	2047	24	1923	535609344	160668	-	7.00E+10	4.3E-15	
PIF	vacuum	21		1	1	FillMem																											
PIF	vacuum	22	54	1	1	Reset	85	626	1.00E+11	200MeV	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
PIF	vacuum	23		1	2	FillMem																											
PIF	vacuum	24	55	1	2	Read	85	604	1.00E+11	200MeV	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
PIF	vacuum	25		1	2	FillMem																											
PIF	vacuum	26	56	1	2	PowerOFF		613	1.00E+11	200MeV																							
PIF	vacuum	27		1	2	PowerOFF				200MeV	0	-	-	-	-	-	-	-	-	-	-	-	-	100	2047	24	1923	535609344	18539	-	1.00E+11	3.5E-16	run026 continuation
PIF	vacuum	28		1	2	FillMem																											
PIF	vacuum	29	57	1	2	Read		639	1.00E+11	200MeV	0	0	99	100	1442	1538	1545	12	1090	1526	27852800	5.48E-16	0	-	-	-	-	-	-	-	-	-	
PIF	vacuum	30	58	1	2	ReadWrite		602	1.00E+11	200MeV	0	100	199	100	473	545	700	6	15	539	27852800	1.94E-16	**3**	200	2047	24	877	244269056	113375	-	2.00E+11	2.3E-15	static failure :946 blocks to 0xFF
PIF	vacuum	31		1	2	FillMem																											
PIF	vacuum	32	59	1	2	PowerOFF		702	1.00E+11	150MeV	0	-	-	-	-	-	-	-	-	-	-	-	-	100	2047	24	1923	535609344	28271	-	7.00E+10	7.5E-16	
PIF	vacuum	33		1	2	FillMem																											
PIF	vacuum	34	60	1	2	Read		682	1.00E+11	150MeV	0	0	99	100							27852800			100	2047	24	1923	535609344	31522	-	1.00E+11	5.9E-16	
PIF	vacuum	35	61	1	2	ReadWrite		493	7.24E+10	150MeV	0	100	199	100							27852800			200	2047	24	1823	507756544	66606	-	1.72E+11	7.6E-16	dynamic: memory failure
PIF	vacuum	36		1	2	FillMem																											Dut2 dead
PIF	vacuum	37		2	1	FillMem																											
PIF	vacuum	38	62	2	1	PowerOFF		824	6.22E+10	70MeV	0	-	-	-	-	-	-	-	-	-	-	-	-	100	2047	24	1923	535609344	9801	-	6.22E+10	2.9E-16	
PIF	vacuum	39		2	1	FillMem																											
PIF	vacuum	40	63	2	1	Read		1020	6.94E+10	70MeV	0	0	99	100	987	1057	1037	7	732	1050	27852800	5.43E-16	0	100	2047	24	1923	535609344	14015	-	6.94E+10	3.8E-16	
PIF	vacuum	41		2	1	FillMem																											
PIF	vacuum	42	64	2	1	ReadWrite		929	7.00E+10	70MeV	0	100	199	100	315	354	471	2	2	352	27852800	1.81E-16	0	200	2047	24	1823	507756544	15977	-	7.00E+10	4.5E-16	
PIF	vacuum	43		2	1	FillMem																											
PIF	vacuum	44	65	2	1	PowerOFF		1119	7.00E+10	50MeV	0	-	-	-	-	-	-	-	-	-	-	-	-	100	2047	24	1923	535609344	27551	-	7.00E+10	7.3E-16	
PIF	vacuum	45		2	1	FillMem																											
PIF	vacuum	46	66	2	1	Read		1065	7.00E+10	50MeV	0	0	99	100	2907	3087	3107	16	2052	3071	27852800	1.57E-15	0	100	2047	24	1923	535609344	38365	-	7.00E+10	1.0E-15	
PIF	vacuum	47	67	2	1	ReadWrite		249	1.64E+10	50MeV	0	100	199	100							27852800			200	2047	24	1823	507756544	54755	-	7.00E+10	1.5E-15	dynamic: memory failure

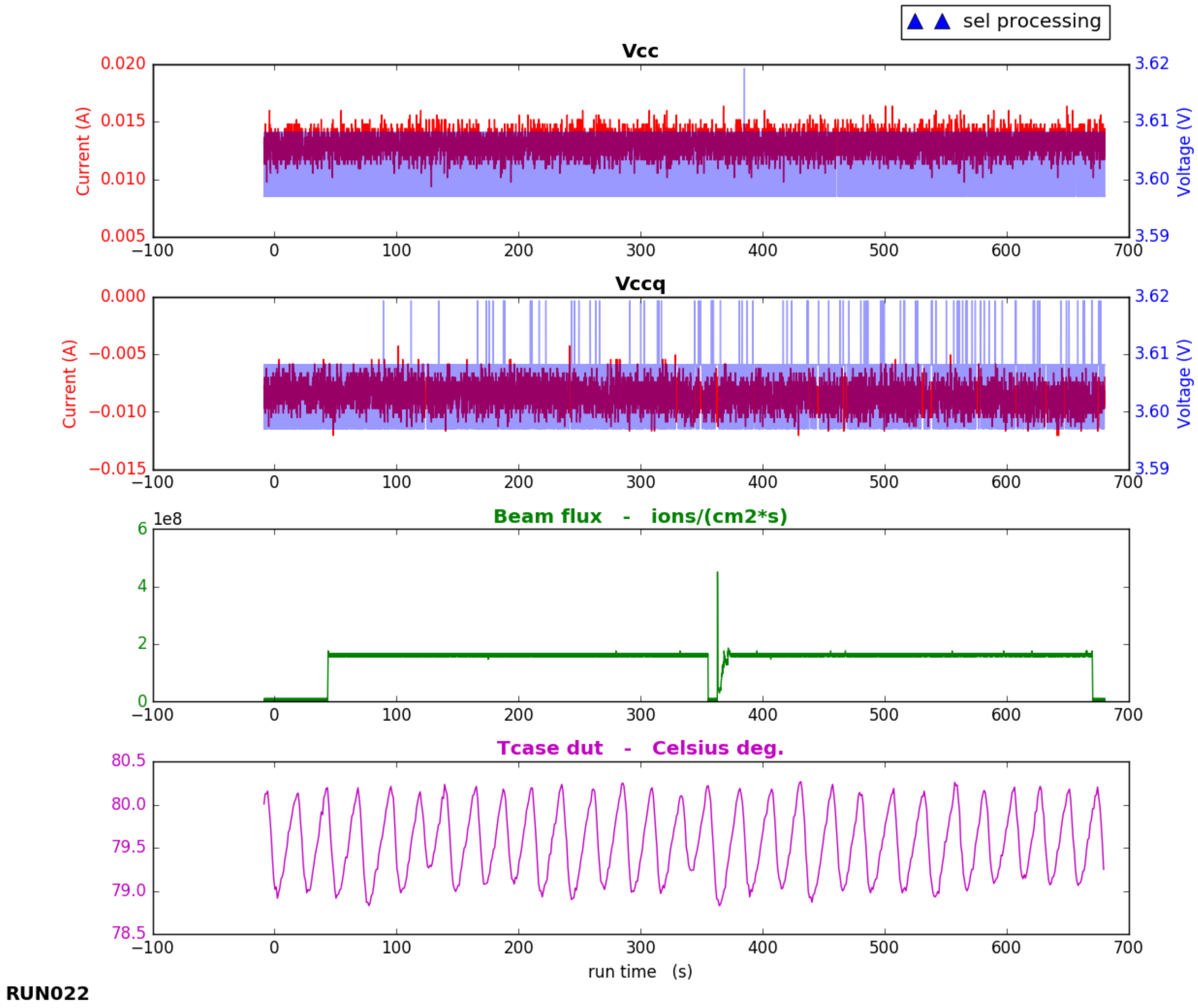

Figure 12: Run022, chronograms for Vcc and Vccq lines along with temperature and flux.

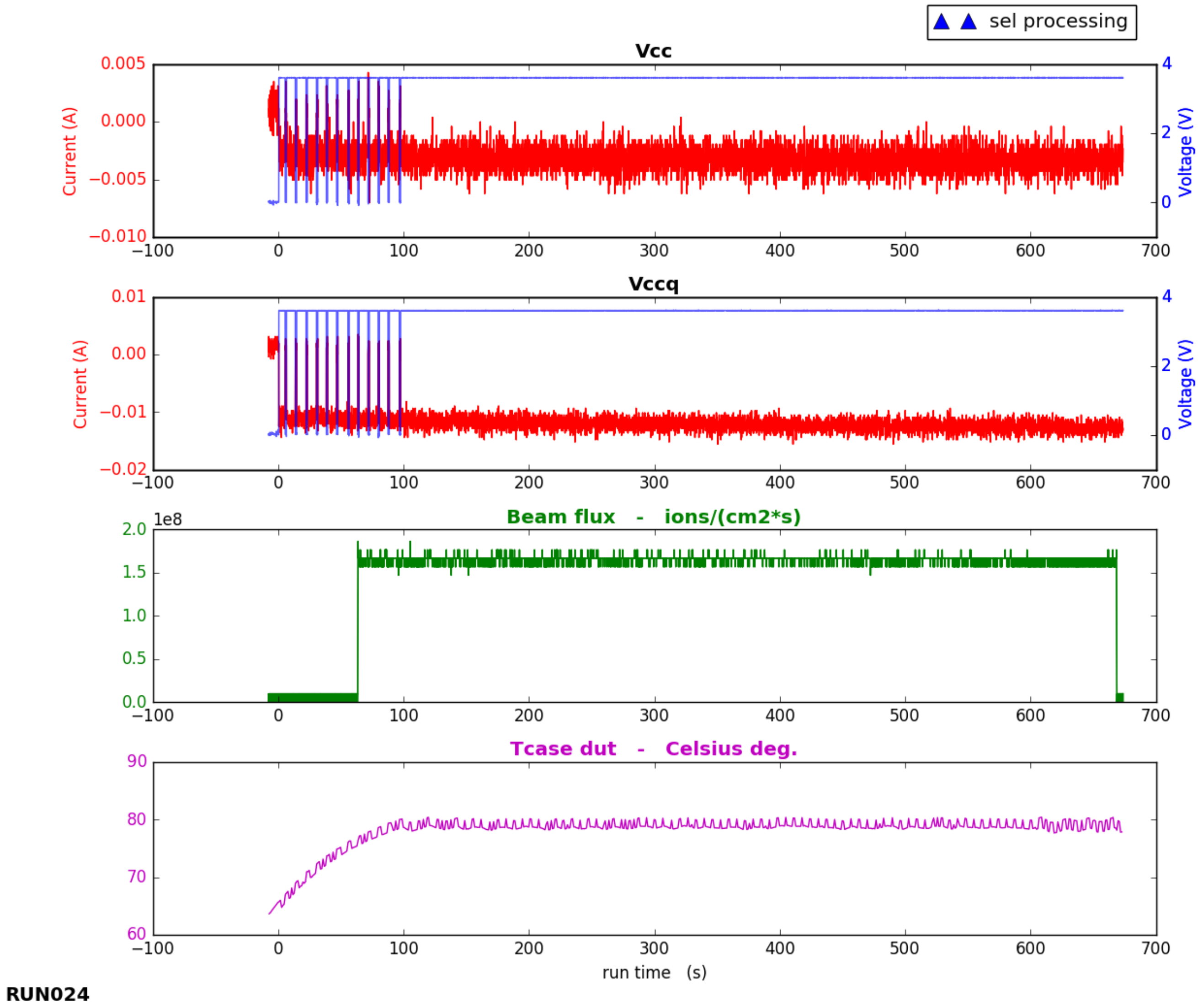

Figure 13: Run024, chronograms for Vcc and Vccq lines along with temperature and flux.

10 Glossary

DUT: Device under test.

Fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.
In this document, Fluence is expressed in ions per cm^2.

Flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.
In this document, Flux is expressed in ions per $cm^2.s$.

Single-Event Effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.
Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL).

Single Event Gate Rupture (SEGR) **/ Single Event Dielectric Rupture (**SEDR**):** Destructive rupture of the gate oxide layer or dielectric layer by a single ion strike. This leads to leakage currents under bias and can be observed as stuck bits in digitals devices

Single-Event Upset (SEU)**:** A soft error caused by the transient signal induced by a single energetic particle strike.

Single-Event Transient (SET): A transient signal induced by a single energetic particle strike.

Single-Event Latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.
SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.
An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

Single-Event Functional Interrupt (SEFI): A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single-event burnout (SEB).
A SEFI is often associated with an upset in a control bit or register.

Error cross-section: the number of errors per unit fluence. For device error cross-section, the dimensions are cm^2 per device. For bit error cross-section, the dimensions are cm^2 per bit.

Tilt angle: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis

Weibull fit: $F(x) = A (1- \exp\{-[(x-x_0)/W]^s\})$ with:

x = effective LET in $MeV/(mg/cm^2)$;
$F(x)$ = SEE cross-section in cm^2;
A = limiting or plateau cross-section;
x_0 = onset parameter, such that $F(x) = 0$ for $x < x_0$;
W = width parameter;
s = a dimensionless exponent.

Error bars: error bars are computed using a confidence level of 95% and a beam flux uncertainty of +/- 10% as recommended by Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100.