Single Event Effects

Heavy Ions Test Report

Test type	Single Event Latchup – Single Event Upset Single Event Functional Interrupt
Part Reference	TC58NVG2S0HTAI0
Tested function	NAND Flash Memory
Chip manufacturer	Toshiba
Test Facility	RADEF, Jyvaskyla, Finland
Test Date	March 2017 and June 2017
Customer	ESA ESTEC

BCE5524

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1 Introduction

This report presents results of SEE test campaign for the Toshiba NAND Flash Memory TC58NVG2S0HTAI0. 16 parts were prepared with 2 parts per test sequence. The test campaign took place at RADEF, Jyvaskyla, Finland in March 2017 and June 2017.

2 Applicable and Reference Documents

Applicable Documents

AD-1 TOSHIBA TC58NVG2S0HTAI0 Datasheet, Revision 1.0 (July, 05, 2013)
AD-2 TC58NVG2S0HTAI0 physical analysis HRX/RCA/00109
AD-3 Single Event Effects test specification HRX/SEP/00095 issue1

Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

3 Device Information

3.1 Device description

TC58NVG2S0HTAI0, NAND Flash Memory

Manufacturer:	Toshiba
Package:	TSOP48
Marking:	TOSHIBA NH2156 TAIWAN 1509 9AE
Date code	1509
Technology:	CMOS
Die dimensions:	4.9 mm x 6.2 mm

This 4Gb memory is composed of 2048 blocks. Each block is organized in 64 pages of (4096 + 256) bytes.

3.2 Device and die identification

Figure 1: Package, top.

Figure 2: Package, bottom.

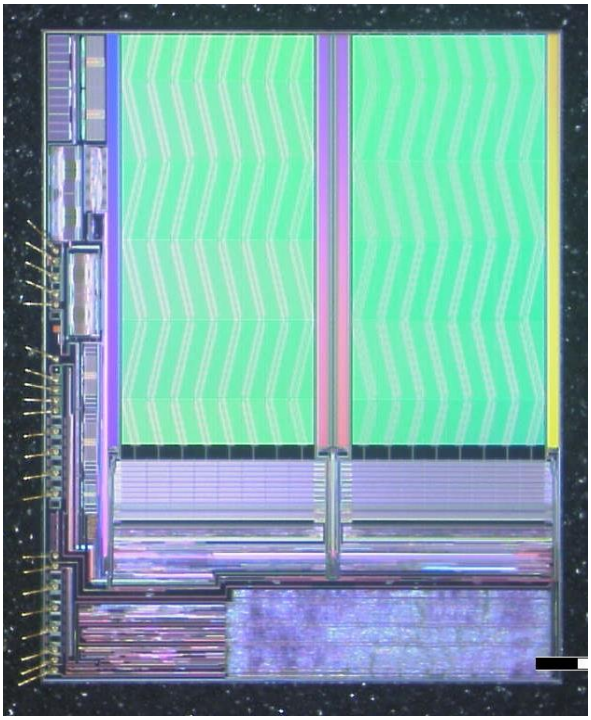


Figure 3: Die dimension.

Figure 4: Die marking.

3.3 Sample preparation

Components were opened from the front side and tested for their functionality. Static tests were performed on DUT 4 of board TC2 and DUT 4 of board TC1. SEL test were performed on DUT 4 of board TC1. Dynamic tests were performed on DUT 1, 2, 3 and 4 of board TC12.

4 Test Setup

Figure 5 shows the principle of the single event test system.
The test system is based on a Virtex4 FPGA (Xilinx). It runs at 50 MHz. The test board has 271 I/Os which can be configured using several I/O standards.
The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 24 independent channels.
The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.
SEL event is detected when the supply current is over a configurable threshold (typically 5 to 10 times the nominal current) and processed:
Once detected, SEL state is maintained for typically 1 or 2ms and power supplies are cut off during a wait time of typically 1 s. These times are configurable.
Each power supply under supervision is monitored independently for SEL detection and processing but subsequent cut off is performed on all power supplies.

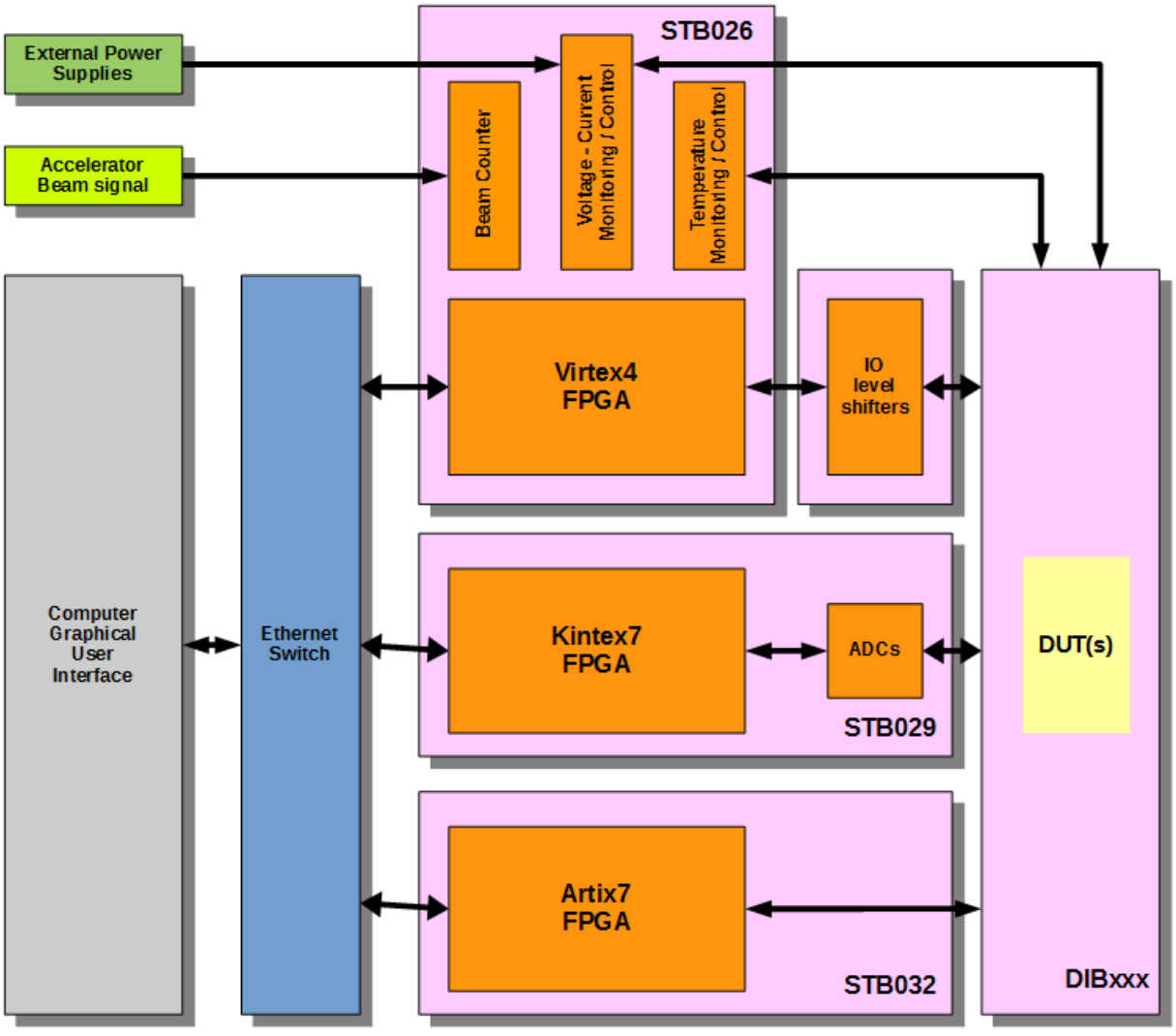


Figure 5: Hirex SEL test setup

5 Test sequence

Test modes and their sequence used during the test campaign are summarized in Figure 6. Operations in grey boxes are performed before the irradiation. Operations in white are performed outside the beam when the shutter is closed. Operation in blue boxes are performed under irradiation and operations in yellow boxes are performed once the beam is stopped at the end of the run.
Each test mode starts with a pre-run sequence during which the full chip is erased and then written with a complementary pattern (0x66 and 0x99).

5.1 Off sequence

The DUT is turned off after the pre-run. It is then turned back on once the total fluence has been reached and the full chip is read twice.

5.2 Read sequence

The read sequence consists in a loop of a read operation followed by a power-cycle and a second read operation. This sequence focuses on 100 blocks of the memory. The pattern used is alternatively a checkerboard and complementary checkerboard pattern (0xAA and 0x55).

5.3 Erase/Write sequence

During the erase/write (E/W) sequence, 100 blocks are erased and then written under the beam flux. The shutter is then closed to power-cycle the DUT and read the blocks previously written. These operations are then looped for the duration of the run before performing a power-cycle and reading the full chip.

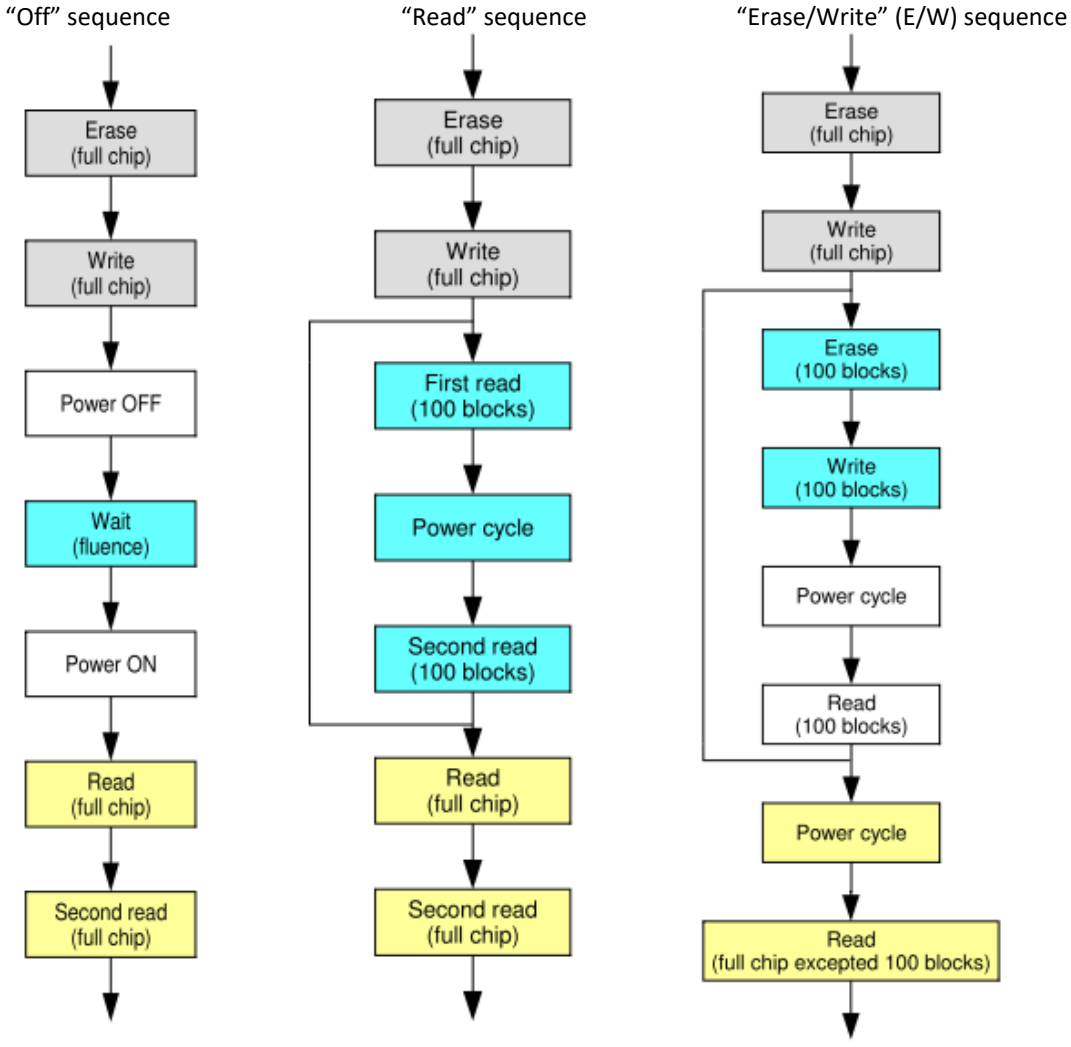


Figure 6: Test mode used during the test campaign.

6 RADEF facility

The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.
The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula,

$$130\ Q^2/M,$$

where Q is the ion charge state and M is the mass in Atomic Mass Units.

6.1 Test chamber

Irradiation of components is performed in a vacuum chamber with an inside diameter of 75 cm and a height of 81 cm.
The vacuum in the chamber is achieved after 15 minutes of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the X, Y and Z directions. The possibility of rotation around the Y-axis is provided by a round table. The free movement area reserved for the components is 25 cm x 25 cm, which allows one to perform several consecutive irradiations for several different components without breaking the vacuum.
The assembly is equipped with a standard mounting fixture. The adapters required to accommodate the special board configurations and the vacuum feed-throughs can also be made in the laboratory's workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components.
A CCD camera with a magnifying telescope is located at the other end of the beam line to determine accurate positioning of the components. The coordinates are stored in the computer's memory allowing fast positioning of various targets during the test.

6.2 Beam quality control

For measuring beam uniformity at low intensity, a CsI(Tl) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis.
A set of four collimated PIN-CsI(Tl) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.
Two beam wobblers and/or a 0.5 microns diffusion Gold foil can be used to achieve good beam homogeneity. The foil is placed 3 m in front of the chamber. The wobbler-coils vibrate the beam horizontally and vertically, the proper sweeping area being attained with the adjustable coil-currents.

6.3 Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI(Tl) detectors. Three collimators of different size and shape are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.
At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(Tl) detectors.

6.4 Used ions

Ion	LET^{SRIM} at surface [MeV.cm^2.mg^{-1}]	Range [µm]	Beam energy [MeV]
$^{15}N^{4+}$	1.83	202	139
$^{20}Ne^{6+}$	3.63	146	186
$^{40}Ar^{12+}$	10.2	118	372
$^{56}Fe^{15+}$	18.5	97	523
$^{82}Kr^{22+}$	32.1	94	768
$^{131}Xe^{35+}$	60.0	89	1217

SRIM-2003.26

Table 1: Ion beam setting

6.5 Test conditions

SEU tests were carried out at Vdd min and room temperature.
Samples for SEL were tested at Vdd max and at a junction temperature of 85°C.

7 Results

Only the static SEU and SEL were investigated for this reference during the test campaign.
Retention mode tested during “Off” sequence exhibits a saturated cross-section of 2.0E-10 cm²/bit and a LET threshold around 1.8 MeV/mg/cm².
Detailed results are presented in section 8. Data are plotted for the two DUT and extrapolated with a Weibull curve given by the following equation:

$$F(x) = Sat\left(1 - \exp\left\{-\left[\frac{x - x_0}{W}\right]^S\right\}\right)$$

During SEL tests, several events were recorded on the Vcc line with high current steps around 0.4 A and peaks over 0.6 A.
SEL have been observed only at high temperature and Vdd max for the Vcc source. No typical cross-section curve can be extrapolated with only one LET value. The SEL cross section at a LET of 60 MeV/mg/cm² is below 8.0E-6 cm²/device

8 Detailed results

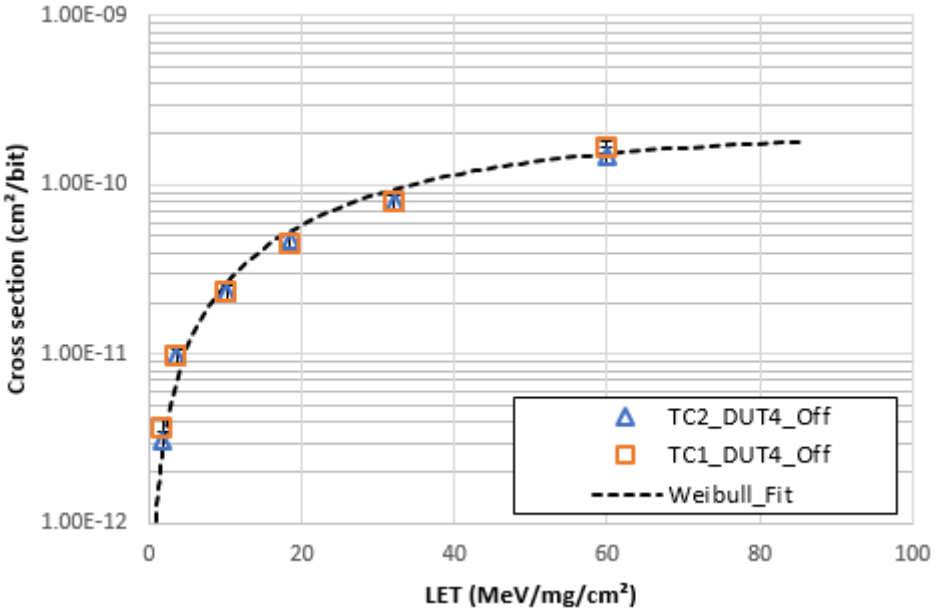
8.1 SEE tests

8.1.1 Off sequence

Results for the Off sequence are summarized in Table 2. Each bit flip is counted as an SEU. When only one bit flipped in a single word, the error is categorized as Single Bit Upset (SBU) and when multiple bits of a single word are flipped, this is counted as Multiple Bit Upsets (MBU).

Table 2: SEU results for "Off" sequence.

Facility	Campaign	Run number	Board id	DUT	Test mode	Ion	LET (MeV.cm²/mg)	Fluence (ions/cm²)	SEU	SBU	MBU	SEU cross-section (cm²/bit)
RADEF	1	49	tc 1	4	Off	N	1.83	1.00E+06	15593	15527	17	3.63E-12
RADEF	1	27	tc 1	4	Off	Ne	3.63	1.00E+06	41186	41118	18	9.59E-12
RADEF	1	45	tc 1	4	Off	Ar	10.2	1.01E+06	100242	99589	310	2.31E-11
RADEF	1	64	tc 1	4	Off	Fe	18.5	1.00E+06	193487	178314	7586	4.50E-11
RADEF	1	76	tc 1	4	Off	Kr	32.1	1.00E+06	337970	239176	49333	7.87E-11
RADEF	1	82	tc 1	4	Off	Xe	60	1.01E+06	712093	337737	181609	1.64E-10
RADEF	1	48	tc 2	4	Off	N	1.83	1.01E+06	13242	13172	19	3.05E-12
RADEF	1	25	tc 2	4	Off	Ne	3.63	1.00E+06	41824	41756	18	9.74E-12
RADEF	1	46	tc 2	4	Off	Ar	10.2	1.01E+06	101201	100922	123	2.33E-11
RADEF	1	65	tc 2	4	Off	Fe	18.5	1.00E+06	200706	185441	7629	4.67E-11
RADEF	1	77	tc 2	4	Off	Kr	32.1	1.00E+06	338538	237626	50405	7.88E-11
RADEF	1	79	tc 2	4	Off	Xe	60	1.00E+06	643802	285642	173935	1.50E-10



Weibull
W = 45
S = 1.3
x_0 = 0.1
Sat = 2.00e-10

Figure 7: SEU static cross-section for "OFF" sequence.

8.1.2 Read sequence

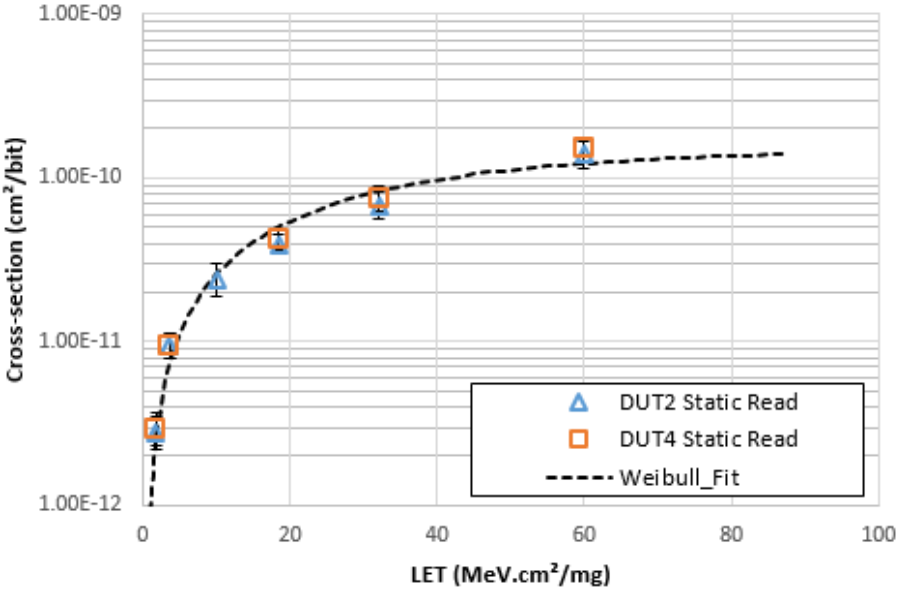
Results for “read” sequence runs are given in Table 3. The SEU static value is computed from the blocks that are not used during read operation. The SEU dynamic value takes into account new errors after each read cycle but reject major functional errors called step failed (read steps with most of the blocks having more than 10 pages with multiple errors).

Large errors recorded are several pages, a full block or most of the tested blocks with errors. Large errors with size 4 MBU are specific addresses stuck to one for several pages of different blocks for one read iteration.

For one run (number 7) no data in static mode has been acquired.

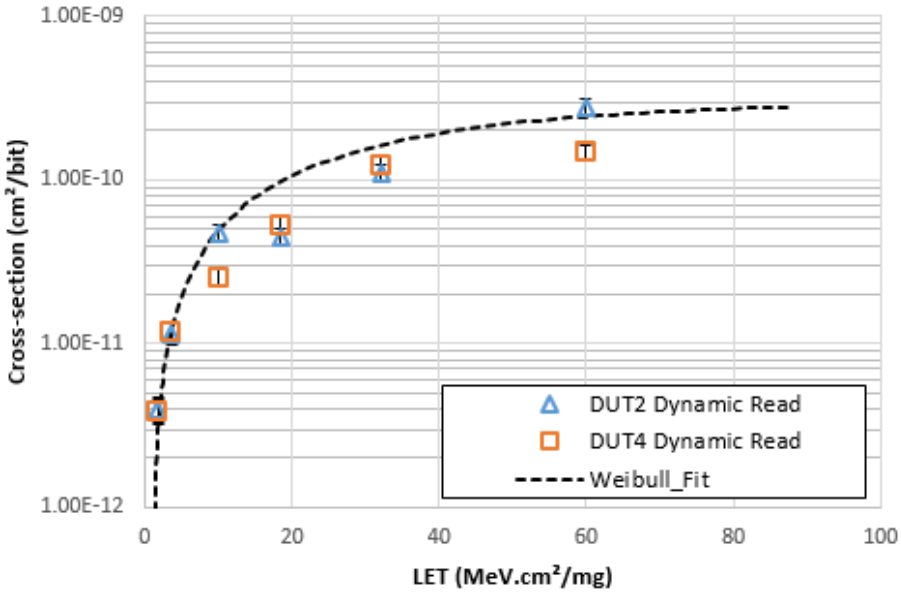
Table 3: Results for read sequence.

Facility	Run number	Board id	DUT	Test mode	Ion	LET (MeV.cm²/mg)	Fluence (ions/cm²)	SEL	SEU static	SEU dynamic	Large errors	SBU	MBU	SEU static cross-section (cm²/bit)	SEU dynamic cross-section (cm²/bit)	Large errors cross-section (cm²/device)
RADEF	17	TC12	2	Read	N	1.8	1.00E+06	0	11366	821	0	12187	0	2.78E-12	3.91E-12	/
RADEF	13	TC12	2	Read	Ne	3.63	1.00E+06	0	38281	2385	0	40662	2	9.37E-12	1.14E-11	/
RADEF	8	TC12	2	Read	Ar	10.1	1.00E+06	0	97135	9800	5	102299	1315	2.38E-11	4.67E-11	5.00E-06
RADEF	22	TC12	2	Read	Fe	18.5	1.00E+06	0	160237	9388	10	156673	6457	3.92E-11	4.48E-11	1.00E-05
RADEF	26	TC12	2	Read	Kr	32.1	1.00E+06	0	276974	22932	18	206603	45120	6.78E-11	1.09E-10	1.80E-05
RADEF	34	TC12	2	Read	Xe	60	1.00E+06	0	579353	57966	15	354504	177132	1.42E-10	2.76E-10	1.50E-05
RADEF	15	TC12	4	Read	N	1.8	1.00E+06	0	11951	800	0	12751	0	2.93E-12	3.81E-12	/
RADEF	14	TC12	4	Read	Ne	3.63	1.00E+06	0	38085	2435	0	40518	1	9.32E-12	1.16E-11	/
RADEF	7	TC12	4	Read	Ar	10.1	1.00E+06	0	No data	5286	5	5185	38	No data	2.52E-11	5.00E-06
RADEF	23	TC12	4	Read	Fe	18.5	1.00E+06	0	173750	11133	14	170909	6963	4.25E-11	5.31E-11	1.40E-05
RADEF	25	TC12	4	Read	Kr	32.1	1.00E+06	0	307226	25629	12	237267	45803	7.52E-11	1.22E-10	1.20E-05
RADEF	36	TC12	4	Read	Xe	60	1.00E+06	0	614216	30755	15	316590	174149	1.5E-10	1.47E-10	1.50E-05



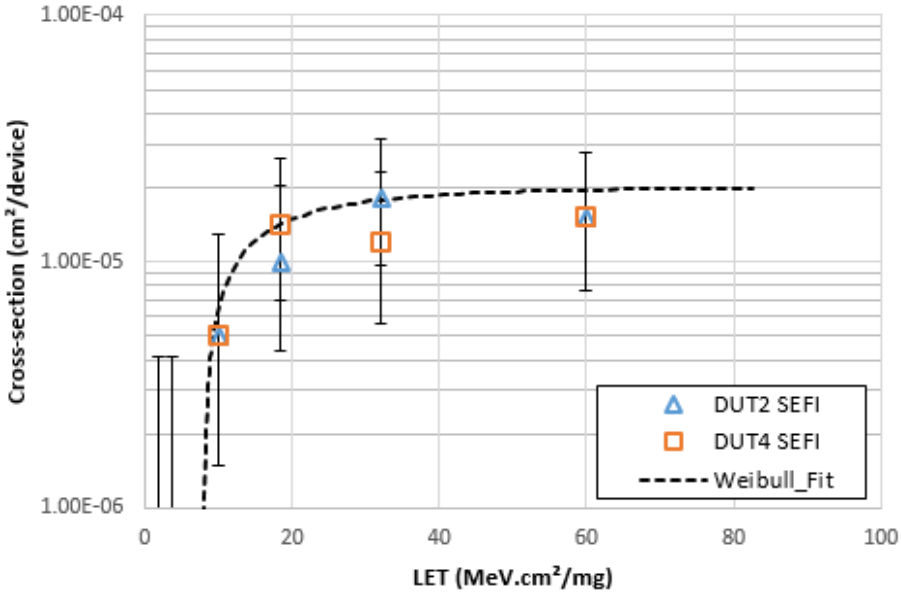
Weibull
W = 38
S = 1.2
x_0 = 0.5
Sat = 1.50Ee-10

Figure 8: SEU static cross-section for "Read" sequence.



Weibull
W = 38
S = 1.2
x_0 = 1
Sat = 3.00E-10

Figure 9: SEU dynamic cross-section for "Read" sequence.



Weibull
W = 7.7
S = 0.7
x_0 = 8
Sat = 2.00E-5

Figure 10: Large error cross-section for "Read" sequence.

8.1.3 Erase/Write sequence

Results for “Erase/Write” sequence runs are given in Table 4. The SEU static value is computed from the blocks that are not used during read operation. The SEU dynamic value takes into account new errors after each E/W cycle but reject step failed and blocks continuously in error.

Large errors occurred above an LET of 3.63 MeV.cm²/mg with errors recorded on several addresses of a single page or several pages of a single block. A typical error called a step failed is characterized by most of the blocks with errors (typically the 16 firsts addresses of the 16 firsts pages of each block in error are set to all 1 or all 0).

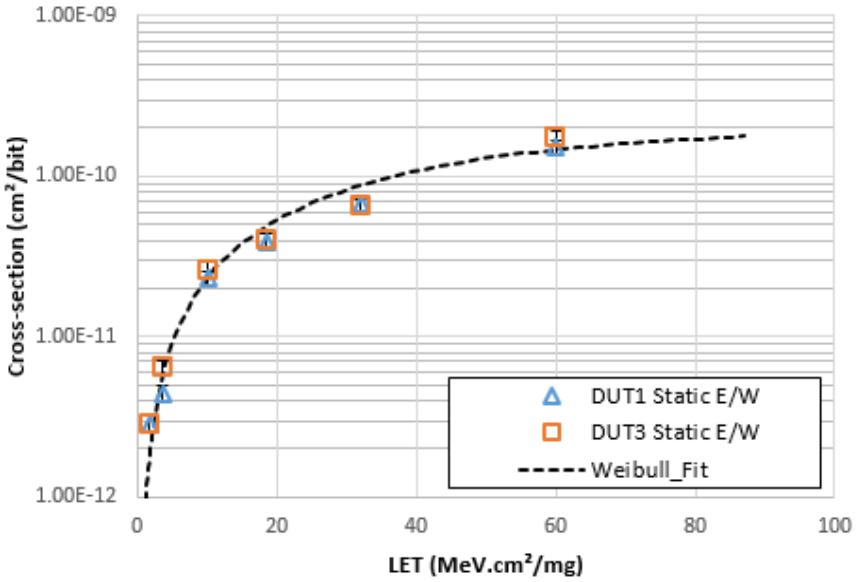
One DUT exhibited blocks continuously in error under Krypton. Both DUT lost most of the dynamically used blocks under Xenon. These blocks remain in error when the beam is off.

Some bits remained stuck for several steps (between 2 and 30 iterations) during dynamic tests causing the same address to remain in error.

Large errors with size 4 MBU are due to specific addresses for all pages of several blocks returning all ones for one read iteration. The discrepancy between the two DUT dynamic cross-section is mainly due to errors similar to large errors but with fewer addresses or pages impacted.

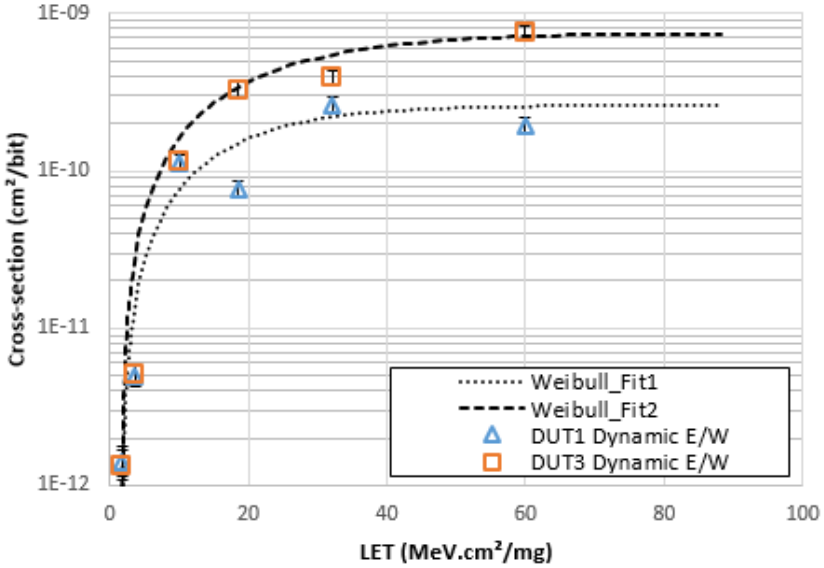
Table 4: Results for erase/write sequence.

Facility	Run number	Board id	DUT	Test mode	Ion	LET (MeV.cm²/mg)	Fluence (ions/cm²)	SEL	SEU static	SEU dynamic		Large errors	SBU	MBU	SEU static cross-section (cm²/bit)	SEU dynamic cross-section (cm²/bit)	Large Errors cross-section (cm²/device)
										Total	Stuck bits						
RADEF	18	TC12	1	E/W	N	1.8	1.00E+06	0	11644	297	1	0	11933	4	2.8503E-12	1.42E-12	/
RADEF	12	TC12	1	E/W	Ne	3.63	1.00E+06	0	18052	1043	23	0	18837	129	4.4188E-12	4.97E-12	/
RADEF	9	TC12	1	E/W	Ar	10.1	1.00E+06	0	94271	23220	471	11	96467	5525	2.3076E-11	1.11E-10	1.10E-05
RADEF	21	TC12	1	E/W	Fe	18.5	1.00E+06	0	159600	16168	2046	21	154291	8495	3.9067E-11	7.71E-11	2.10E-05
RADEF	27	TC12	1	E/W	Kr	32.1	1.00E+06	0	271649	55063	3448	36	203896	51250	6.6495E-11	2.63E-10	3.60E-05
RADEF	32	TC12	1	E/W	Xe	60	6.86E+05	0	425336	7636	2335	18	228838	105765	1.5177E-10	1.92E-10	2.62E-05
RADEF	19	TC12	3	E/W	N	1.8	1.00E+06	0	11504	281	3	0	11775	5	2.816E-12	1.34E-12	/
RADEF	11	TC12	3	E/W	Ne	3.63	1.00E+06	0	26035	1062	18	0	26680	207	6.3729E-12	5.06E-12	/
RADEF	10	TC12	3	E/W	Ar	10.1	1.00E+06	0	106692	24312	730	11	110433	5473	2.6116E-11	1.16E-10	1.10E-05
RADEF	20	TC12	3	E/W	Fe	18.5	1.00E+06	0	162089	68819	2002	39	155672	21924	3.9677E-11	3.28E-10	3.90E-05
RADEF	28	TC12	3	E/W	Kr	32.1	1.00E+06	0	264647	82017	5903	53	204727	54892	6.4781E-11	3.91E-10	5.30E-05
RADEF	29	TC12	3	E/W	Xe	60	1.00E+06	0	705572	157015	14055	45	421439	187692	1.7271E-10	7.49E-10	4.50E-05



Weibull
W = 48
S = 1.3
x_0 = 0.5
Sat = 2.00E-10

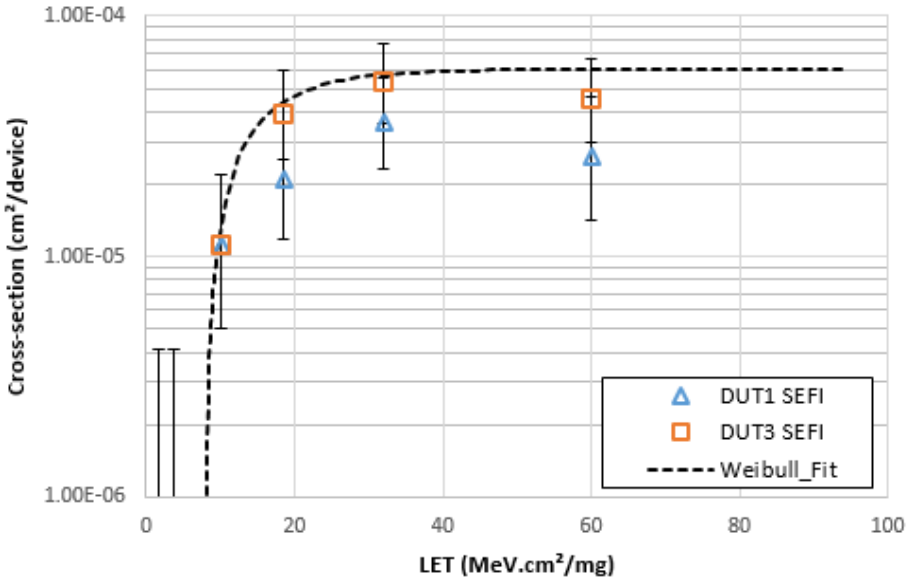
Figure 11: SEU static cross-section for "E/W" sequence.



Weibull 1
W = 19
S = 1.3
x_0 = 1.6
Sat = 2.60E-10

Weibull 2
W = 25
S = 1.3
x_0 = 1.6
Sat = 7.50E-10

Figure 12: SEU dynamic cross-section for "E/W" sequence.



Weibull
W = 8
S = 1
x_0 = 8
Sat = 6.00E-5

Figure 13: Large error cross-section for "E/W" sequence.

8.2 MBU contribution

SBU and MBU contributions are summarized in Table 5. For each test sequence, SBU are counted in the first line ("SBU"), MBU of size 2 or 3 are counted in the second line ("MBU < 4") and blocks with at least one MBU of size 4 are counted in the last line ("MBU ≥ 4").
Static results present the same ratio with a majority of SBU (about 80%).
Dynamic read mode slightly increases the number of MBU compared to static read mode with mostly size 4 MBU due to full pages in error. This increase is higher for E/W mode and leads to as much SBU errors as MBU of size 4 and more.
Once again, the E/W mode is more sensitive and presents the highest ratio of MBU.

Table 5: MBU contribution to overall block errors

Size	Read		Erase/Write		Off
	Static	Dynamic	Static	Dynamic	Static
SBU	78.72%	72.97%	81.83%	46.88%	79.04%
MBU < 4	21.28%	19.74%	18.07%	7.07%	20.95%
MBU ≥ 4	0.00%	7.30%	0.11%	46.04%	0.01%

8.3 SEL tests

Results for SEL runs under Xenon are summarized in Table 6 and illustrated in Figure 14 and Figure 15. Voltage and current for Vcc and Vccq lines are plotted along with the device temperature and the beam flux. The detection threshold set for SEL detection is given by the black curve called "Limit" on current monitoring graphs.
During the first SEL run (number 84) the detection was first set to 100 mA and then adjusted up to 600 mA to be able to record current steps. The second run was lead with a 600 mA upper current limit.
Most of the detected events are preceded by a current step between 150 mA and 500 mA. During run number 84, the last current step lasted when the device was out of the beam and this overcurrent was suppressed by a manual reset.

Table 6: SEL results for TC58NVG2S0HTAI0.

Facility	Run number	Board	DUT	Vcc	Test mode	Temperature (°C)	Ion	Fluence (ions/cm²)	LET (MeV.cm²/mg)	SEL	SEL cross-section (cm²/device)
RADEF	84	tc 1	4	3.6	SEL	85	Xe	2.46E+06	60	8	3.76E-06
RADEF	85	tc 1	4	3.6	SEL	85	Xe	1.00E+07	60	11	1.11E-06

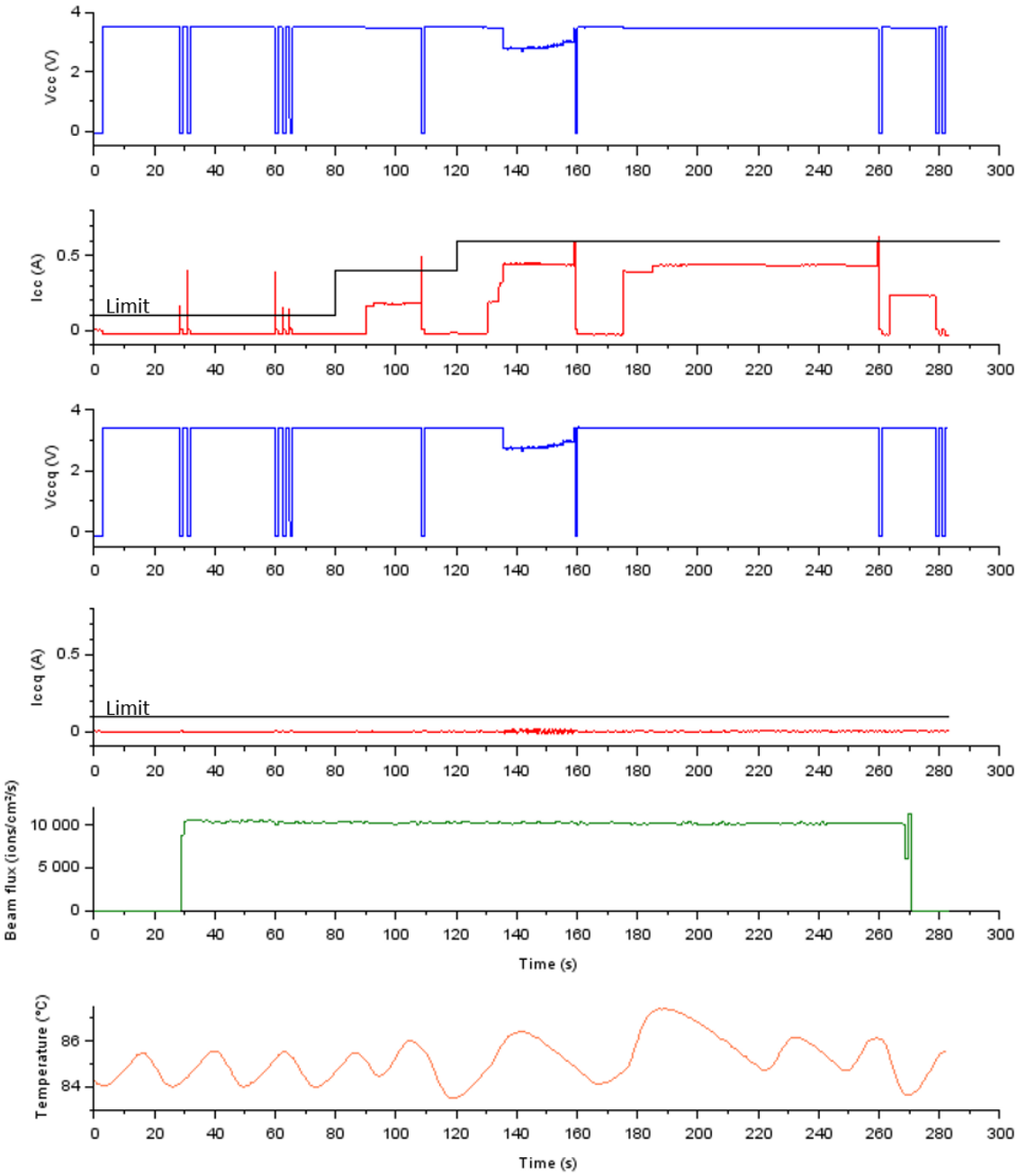


Figure 14: RUN84 chronograms for Vcc and Vccq lines along with temperature and beam flux.

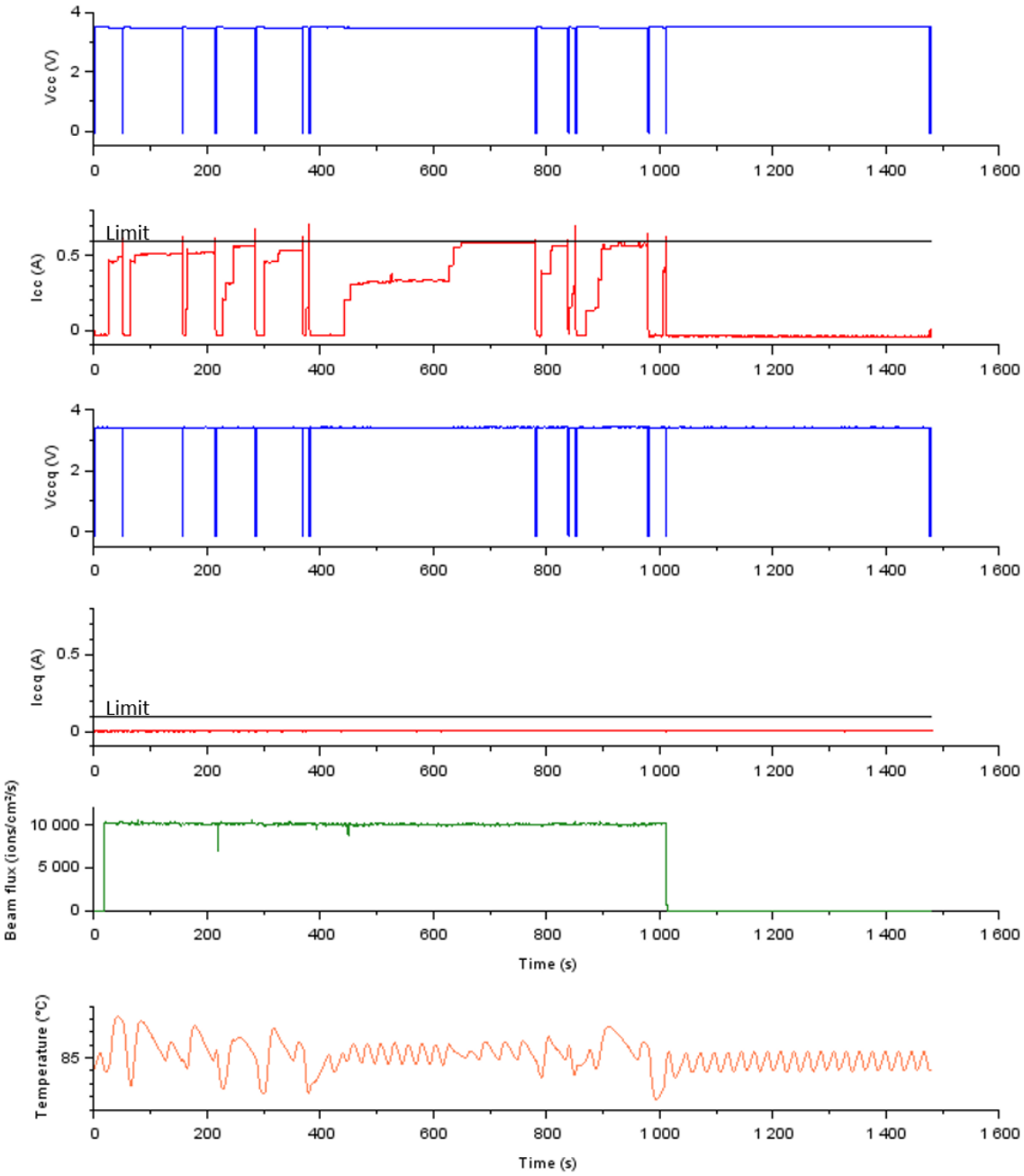


Figure 15: RUN85 chronograms for Vcc and Vccq lines along with temperature and beam flux.

9 Glossary

DUT: Device under test.

Fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.
In this document, Fluence is expressed in ions per cm².

Flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.
In this document, Flux is expressed in ions per cm².s.

Single-Event Effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.
Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL).

Single Event Gate Rupture (SEGR) **/ Single Event Dielectric Rupture (**SEDR**):** Destructive rupture of the gate oxide layer or dielectric layer by a single ion strike. This leads to leakage currents under bias and can be observed as stuck bits in digitals devices

Single-Event Upset (SEU)**:** A soft error caused by the transient signal induced by a single energetic particle strike.

Single-Event Transient (SET): A transient signal induced by a single energetic particle strike.

Single-Event Latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.
SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.
An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

Single-Event Functional Interrupt (SEFI): A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single-event burnout (SEB).
A SEFI is often associated with an upset in a control bit or register.

Error cross-section: the number of errors per unit fluence. For device error cross-section, the dimensions are cm² per device. For bit error cross-section, the dimensions are cm² per bit.

Tilt angle: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis

Weibull fit: $F(x) = A\,(1- \exp\{-[(x-x_0)/W]^s\})$ with:

x = effective LET in MeV/(mg/cm²);
$F(x)$ = SEE cross-section in cm²;
A = limiting or plateau cross-section;
x_0 = onset parameter, such that $F(x) = 0$ for $x < x_0$;
W = width parameter;
s = a dimensionless exponent.

Error bars: error bars are computed using a confidence level of 95% and a beam flux uncertainty of +/- 10% as recommended by Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100.