Single Event Effects

Heavy Ions Test Report

Test type	Single-Event Upset, Single Event Latchup
Part Reference	MX30LF4G18AC
Tested function	NAND Flash Memory
Chip manufacturer	Macronix
Test Facility	RADEF, Jyvaskyla, Finland
Test Date	March 2017 and June 2017
Customer	ESA ESTEC

BCE 5524

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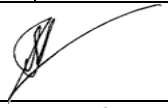
Written by :	M. Rousselet	Engineer		
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1 Introduction

This report presents results of SEE test campaign for the Macronix NAND Flash Memory MX30LF4G18AC. 16 parts were prepared with 2 parts per test sequence. The test campaigns took place at RADEF, Jyvaskyla, Finland in March 2017 and in June 2017.

2 Applicable and Reference Documents

Applicable Documents

AD-1 Macronix MX30LFxG18AC Datasheet, Revision 1.3 (July, 10, 2015)
AD-2 MX30LF4G18AC physical analysis HRX/RCA/00110
AD-3 Single Event Effects test specification, HRX/SEP/00096 issue1

Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

3 Device Information

Device description

MX30LF4G18AC, NAND Flash Memory

Manufacturer:	Macronix
Package:	TSOP48 12 x 20 mm
Marking:	MXIC S144411 MX30LF4G18AC-TI 84112708
Date code	1444
Technology :	CMOS
Die dimensions :	6.9 mm x 7.4 mm

This 4Gb memory is composed of 2 planes of 2048 blocks. Each block is organized in 64 pages of 2048 bytes with 64 additional bytes.

Device and die identification

Figure 1: Package, top.

Figure 2: Package, bottom.

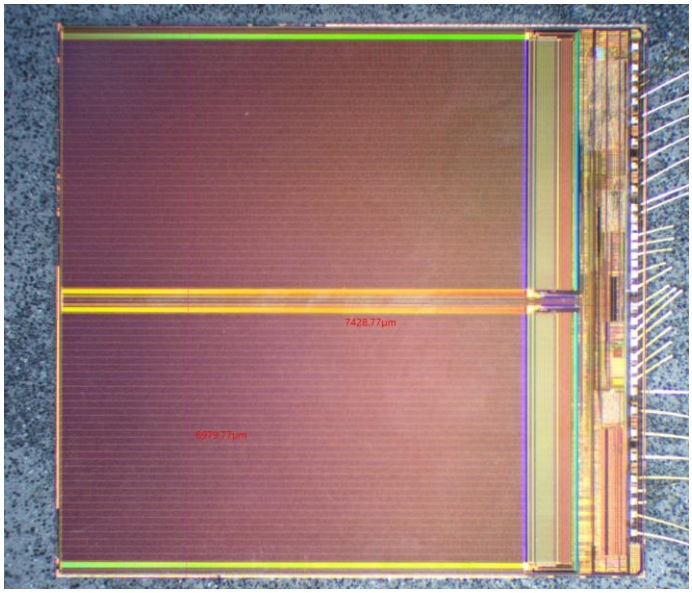


Figure 3: Die dimensions.

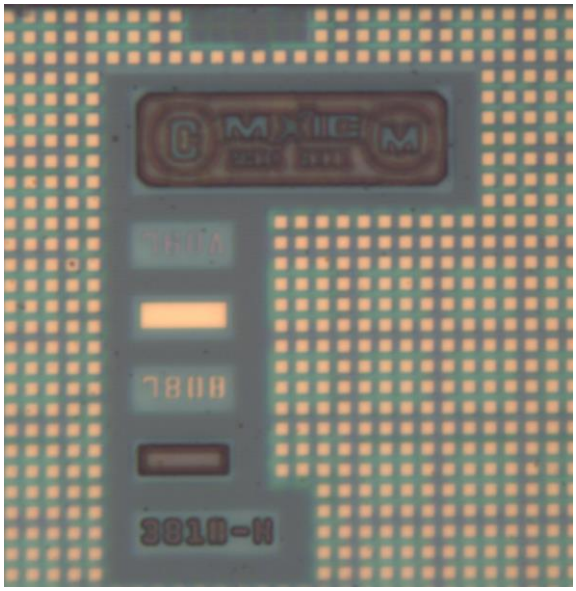


Figure 4: Die marking.

Samples preparation

Samples have been opened chemically and tested for their functionality before the test campaign. Two DUT (number 2 and 4) of board MX1 were used for static tests and two DUT (number 1 and 3) of board MX3 plus three DUT (number 1, 3 and 4] of board MX11 were used for dynamic tests. DUT 1 on board MX4 and 4 on board MX11 were used for SEL test at high temperature.

4 Test Setup

Figure 5 shows the principle of the single event test system.
The test system is based on a Virtex4 FPGA (Xilinx). It runs at 50 MHz. The test board has 271 I/Os which can be configured using several I/O standards.
The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 24 independent channels.
The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.
SEL event is detected when the supply current is over a configurable threshold (typically 5 to 10 times the nominal current) and processed:
Once detected, SEL state is maintained for typically 1 or 2ms and power supplies are cut off during a wait time of typically 1 s. These times are configurable.
Each power supply under supervision is monitored independently for SEL detection and processing but subsequent cut off is performed on all power supplies.

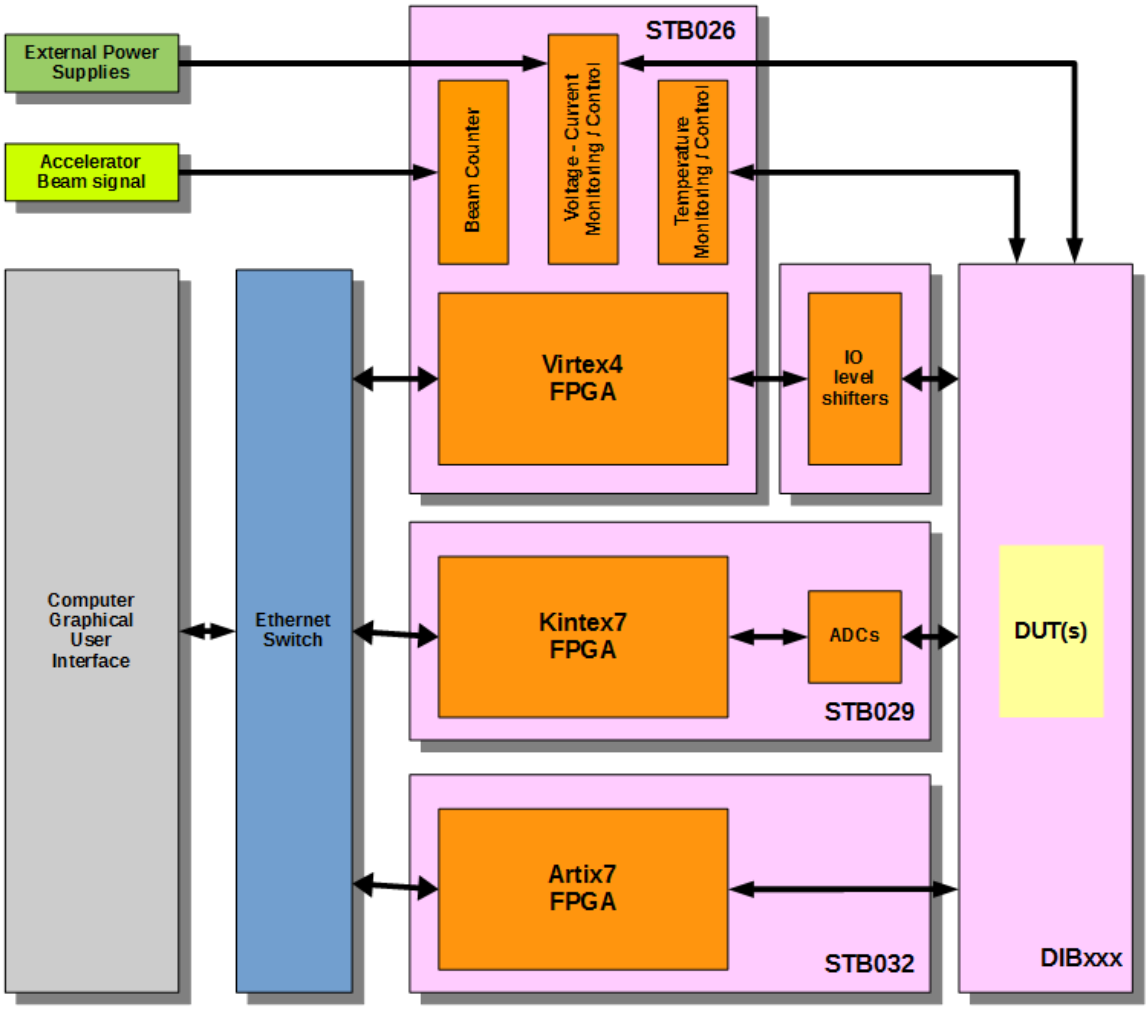


Figure 5: Hirex SEL test setup

5 Test sequence

Test modes and their sequence used during the test campaign are summarized in Figure 6. Operations in grey boxes are performed before the irradiation. Operations in white boxes are performed outside the beam when the shutter is closed. Operation in blue boxes are performed under irradiation and operations in yellow boxes are performed once the beam is stopped at the end of the run.
Each test mode starts with a pre-run sequence during which the full chip is erased and then written with a complementary pattern (alternatively 0x66 and 0x99).

Off sequence

The DUT is turned off after the pre-run. It is then turned back on once the total fluence has been reached and the full chip is read.

Read sequence

The read sequence consists in a loop of a read operation followed by a power-cycle and a second read operation. This sequence focuses on 100 blocks of the memory. The pattern used is alternatively a checkerboard and complementary checkerboard pattern (0xAA and 0x55).

Erase/Write sequence

During the erase/write (E/W) sequence, 100 blocks are erased and then written under the beam flux. The shutter is then closed to power-cycle the DUT and read the blocks previously written. These operations are then looped for the duration of the run before performing a power-cycle and reading the full chip.

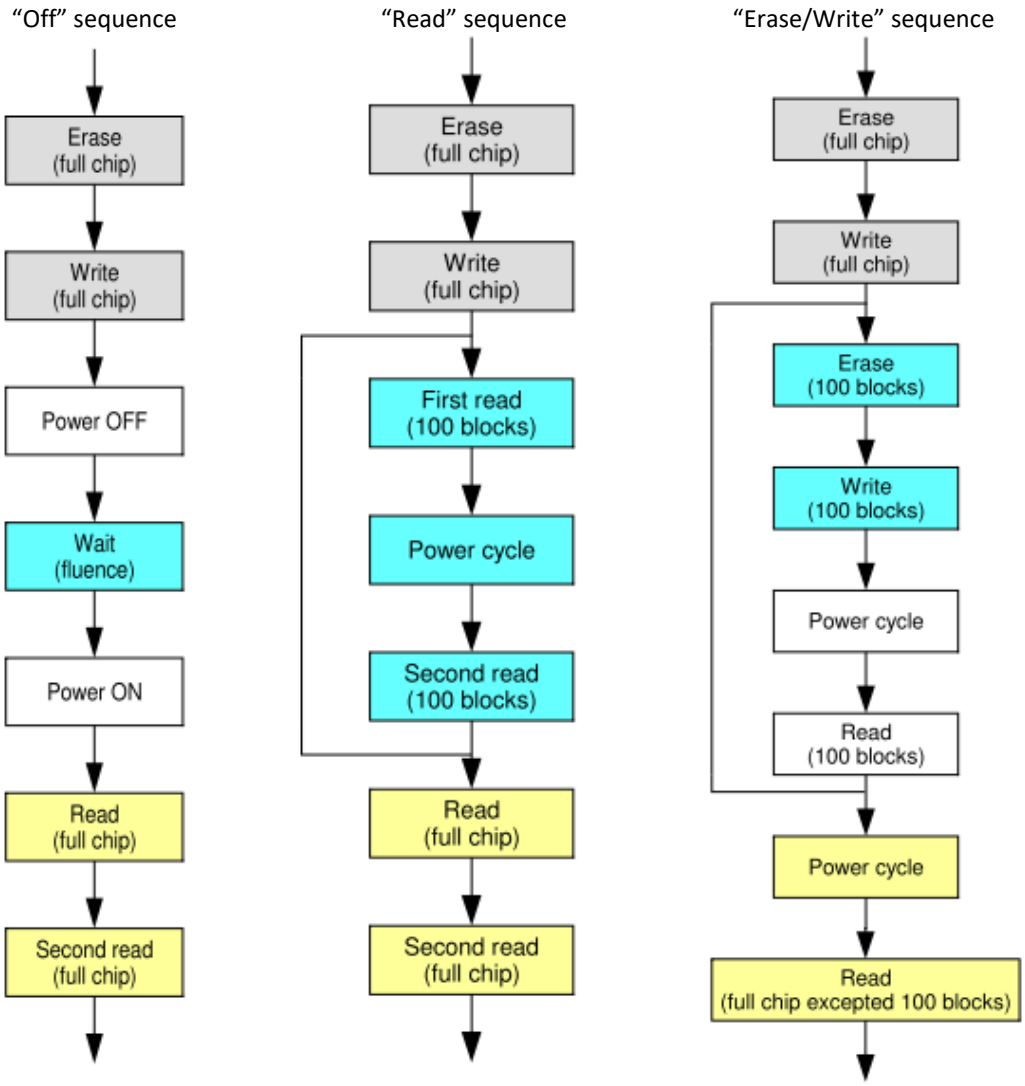


Figure 6: Test modes used during the test campaign.

Both static and dynamic results can be extrapolated based on a single run result. This is done by considering 100 blocks for dynamic behaviour and the rest of the chip for static behaviour.

6 RADEF facility

The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.
The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula,

$$130\ Q^2/M,$$

where Q is the ion charge state and M is the mass in Atomic Mass Units.

Test chamber

Irradiation of components is performed in a vacuum chamber with an inside diameter of 75 cm and a height of 81 cm.
The vacuum in the chamber is achieved after 15 minutes of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the X, Y and Z directions. The possibility of rotation around the Y-axis is provided by a round table. The free movement area reserved for the components is 25 cm x 25 cm, which allows one to perform several consecutive irradiations for several different components without breaking the vacuum.
The assembly is equipped with a standard mounting fixture. The adapters required to accommodate the special board configurations and the vacuum feed-throughs can also be made in the laboratory's workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components.
A CCD camera with a magnifying telescope is located at the other end of the beam line to determine accurate positioning of the components. The coordinates are stored in the computer's memory allowing fast positioning of various targets during the test.

Beam quality control

For measuring beam uniformity at low intensity, a CsI(Tl) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis.
A set of four collimated PIN-CsI(Tl) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.
Two beam wobblers and/or a 0.5 microns diffusion Gold foil can be used to achieve good beam homogeneity. The foil is placed 3 m in front of the chamber. The wobbler-coils vibrate the beam horizontally and vertically, the proper sweeping area being attained with the adjustable coil-currents.

Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI(Tl) detectors. Three collimators of different size and shape are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.
At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(Tl) detectors.

Used ions

Table 1: Ion beam setting.

Ion	LET^{SRIM} at surface [MeV.cm^2.mg^{-1}]	Range [µm]	Beam energy [MeV]
$^{15}N^{4+}$	1.83	202	139
$^{20}Ne^{6+}$	3.63	146	186
$^{40}Ar^{12+}$	10.2	118	372
$^{56}Fe^{15+}$	18.5	97	523
$^{82}Kr^{22+}$	32.1	94	768
$^{131}Xe^{35+}$	60.0	89	1217

SRIM-2003.26

7 Test conditions.

SEU tests were carried out at Vddmin (2.7 V) and room temperature.
Samples for SEL were tested at Vddmax (3.6 V) and a junction temperature of 85°C.

8 Results

Dynamic mode exhibits events characterized as SEFI which are anomalously large number of events. These events can be caused by full pages, several pages of a single block or full blocks in error for a single step as well as specific addresses or pages in error for several steps.
Under Krypton and Xenon, devices tested dynamically in E/W mode loss some functionality and returned bad data (0xFF) for dynamically tested blocks even when the device was out of beam.
Detailed results are provided in section 9 with error bars taking into account a 95% confidence level and 10% beam uniformity. For each data set, a Weibull curve has been proposed based on the following equation:

$$F(x) = Sat\left(1 - \exp\left\{-\left[\frac{x - x_0}{W}\right]^S\right\}\right)$$

SEL runs exhibits events on the Vcc line with high current steps around 0.5 A and peaks over the detection limit of 0.8 A. Some SEL were recorded at high LET for dynamic test runs (read and erase/write) at ambient temperature with amplitude below 0.3 A.
Data and chronograms of SEL recorded are presented at the end of section 9. The SEL cross-section at a LET of 60 MeV/mg/cm² is below 8.0E-5 cm²/device.

9 Detailed results

9.1 SEE

Off sequence

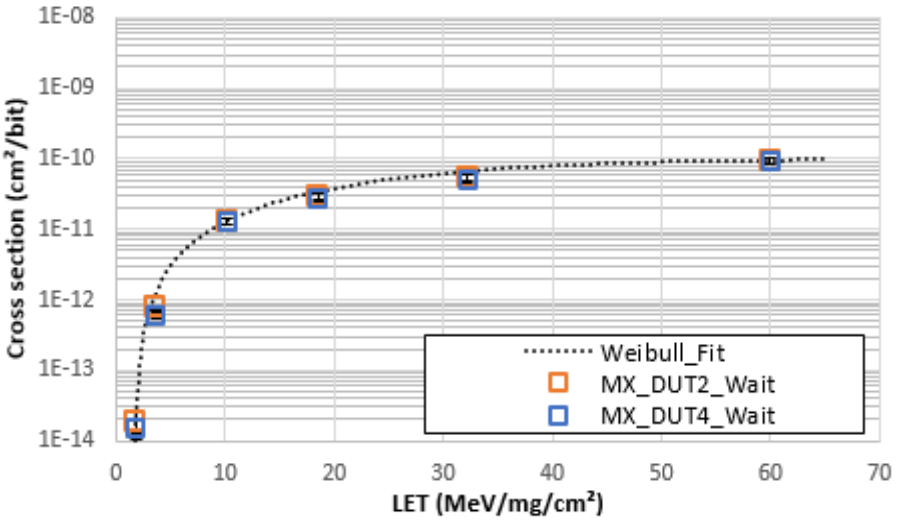
Results for “off” sequence runs are summarized in Table 2. Each bit flip is counted as an SEU. When only one bit flipped in a single word, the error is categorized as Single Bit Upset (SBU) and when multiple bits of a single word are flipped, this is counted as Multiple Bit Upsets (MBU). This later event is subdivided into different sizes of MBU depending on data recorded.

Only SBU and size 2 MBU occurred during the off sequence. MBU were recorded for LET above 10 MeV.cm²/mg.

Table 2: SEE results for "Off" sequence.

Facility	Campaign	Run number	DUT	Test mode	Ion	Fluence (ions/cm²)	LET (MeV.cm²/mg)	SEU	SBU	MBU (2)	SEU cross-section (cm²/bit)
RADEF	1	51	2	Off	N	1.02E+06	1.83	80	80	0	1.83E-14
RADEF	1	8	2	Off	Ne	1.01E+06	3.63	3312	3312	0	7.64E-13
RADEF	1	43	2	Off	Ar	1.01E+06	10.2	54842	54836	3	1.26E-11
RADEF	1	62	2	Off	Fe	1.00E+06	18.5	124559	124547	6	2.90E-11
RADEF	1	74	2	Off	Kr	1.01E+06	32.2	227416	227344	36	5.24E-11
RADEF	1	87	2	Off	Xe	1.00E+06	60	405336	405028	154	9.44E-11
RADEF	1	50	4	Off	N	1.01E+06	1.83	64	64	0	1.48E-14
RADEF	1	11	4	Off	Ne	1.01E+06	3.63	2641	2641	0	6.09E-13
RADEF	1	44	4	Off	Ar	1.01E+06	10.2	54355	54351	2	1.25E-11
RADEF	1	63	4	Off	Fe	1.00E+06	18.5	120327	120309	9	2.80E-11
RADEF	1	75	4	Off	Kr	1.01E+06	32.2	224984	224904	40	5.19E-11
RADEF	1	86	4	Off	Xe	1.00E+06	60	403899	403651	124	9.40E-11

Cross-section results are plotted in Figure 7 along with a Weibull fit curve.



Weibull parameters
W = 29
S = 1.6
x_0 = 1.7
Sat = 1.0E-10

Figure 7: SEU static cross-section for "OFF" sequence.

Read sequence

Results for “read” sequence runs are given in Table 3. The SEU static value is computed from the blocks that are not used during read operation. The SEU dynamic value takes into account new errors after each read cycle but reject major SEFI (step failed and addresses or blocks continuously in error).

Table 3: SEE results for "Read" sequence.

Facility	Campaign	Run number	DUT	Test mode	Ion	Fluence (ions/cm²)	LET (MeV.cm²/mg)	SEU - static	SEU - dynamic	SEFI	SBU	MBU (2)	MBU (3)	MBU (4)	Static cross section (cm²/bit)	Dynamic cross section (cm²/bit)	SEFI cross-section (cm²/DUT)
RADEF	1	66	1	Read	N	1.56E+06	1.83	120	2	0	122	0	0	0	1.43E-14	9.54E-15	/
RADEF	1	18	1	Read	Ne	1.55E+06	3.63	6121	212	0	6333	0	0	0	7.30E-13	1.01E-12	/
RADEF	1	41	1	Read	Ar	7.92E+05	10.2	54813	1701	2	56222	2	0	272	1.31E-11	1.62E-11	2.00E-06
RADEF	1	59	1	Read	Fe	8.17E+05	18.5	123699	4363	4	126930	18	0	541	2.95E-11	4.16E-11	4.00E-06
RADEF	1	72	1	Read	Kr	1.23E+06	32.2	333930	9665	18	342303	88	0	279	5.31E-11	6.14E-11	1.20E-05
RADEF	1	69	3	Read	N	7.82E+05	1.83	134	0	0	134	0	0	0	3.17E-14	/	/
RADEF	1	17	3	Read	Ne	1.56E+06	3.63	4295	141	1	4432	0	0	1	5.13E-13	6.72E-13	5.00E-07
RADEF	1	42	3	Read	Ar	7.84E+05	10.2	51616	1242	2	52858	0	0	0	1.23E-11	1.18E-11	2.00E-06
RADEF	1	61	3	Read	Fe	7.91E+05	18.5	113442	2767	6	116117	14	0	16	2.71E-11	2.64E-11	6.00E-06
RADEF	1	70	3	Read	Kr	1.22E+06	32.2	313843	7448	14	321143	64	0	5	4.99E-11	4.74E-11	9.33E-06
RADEF	2	41	1	Read	Xe	1.00E+06	60	411011	10796	13	421517	130	10	0	9.81E-11	1.03E-10	1.30E-05
RADEF	2	42	4	Read	Xe	1.00E+06	60	380459	10989	13	390166	129	0	256	9.08E-11	1.05E-10	1.30E-05

Some SEFI are observed during read operation:

Address error: One address in error for several blocks during a single read operation

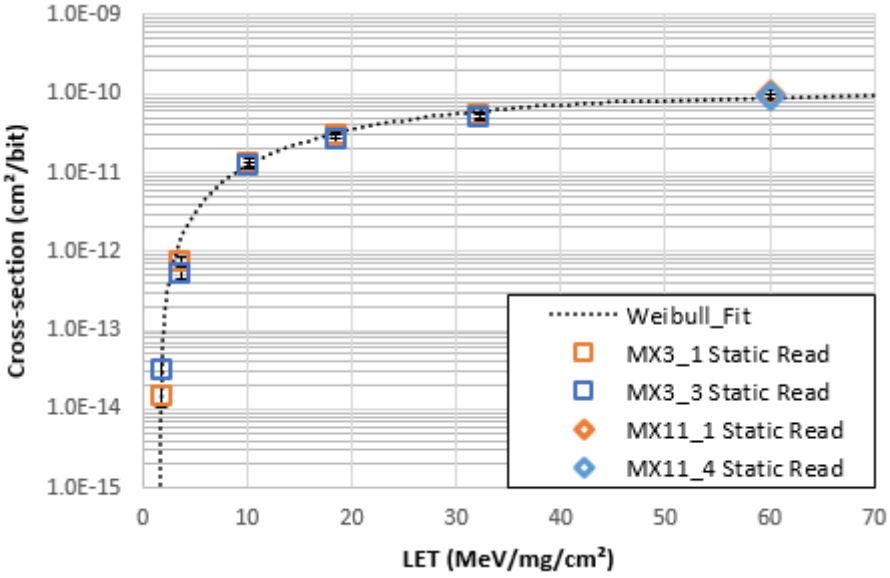
Page error: Several pages of a single block in error

Block error: One block in error

Step fail: Most of the blocks (>80%) read in error

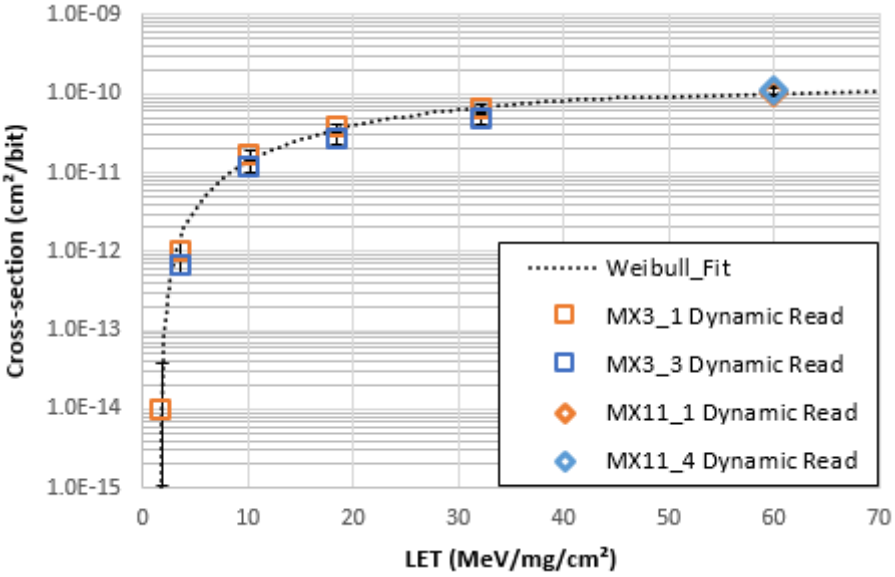
Block and page errors are observed in the same proportion. Size 3 MBU recorded for run 41 correspond to several addresses read in static mode (not read during irradiation).

During the second campaign, 2 SEL occurred under Xenon for each run (number 41 and 42) during read operation with peaks below 0.3 A.



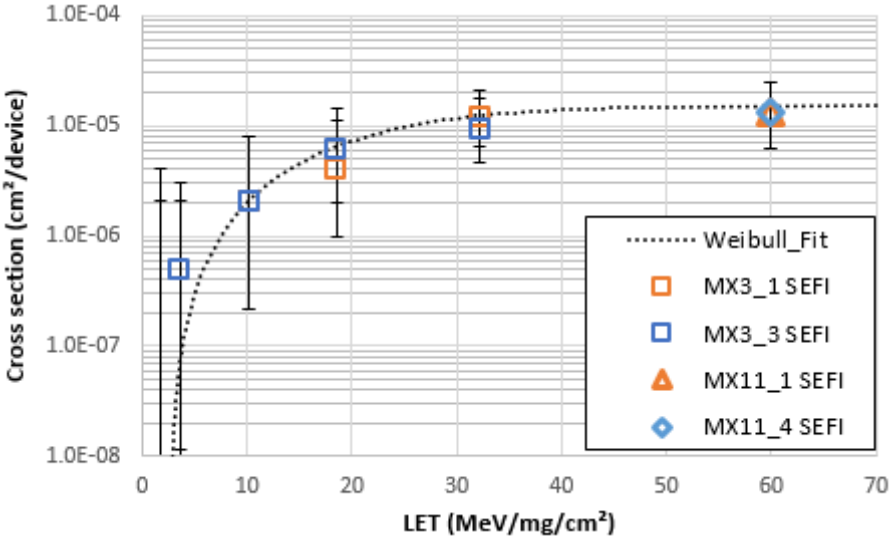
Weibull
W = 31.6
S = 1.5
x_0 = 1.7
Sat = 9.8E-11

Figure 8: SEU static cross-section for "Read" sequence.



Weibull
W = 31.5
S = 1.5
x_0 = 1.8
Sat = 1.1E-10

Figure 9: SEU dynamic cross-section for "Read" sequence.



Weibull
W = 22
S = 1.8
x_0 = 2.5
Sat = 1.5E-5

Figure 10: SEFI cross-section for "Read" sequence.

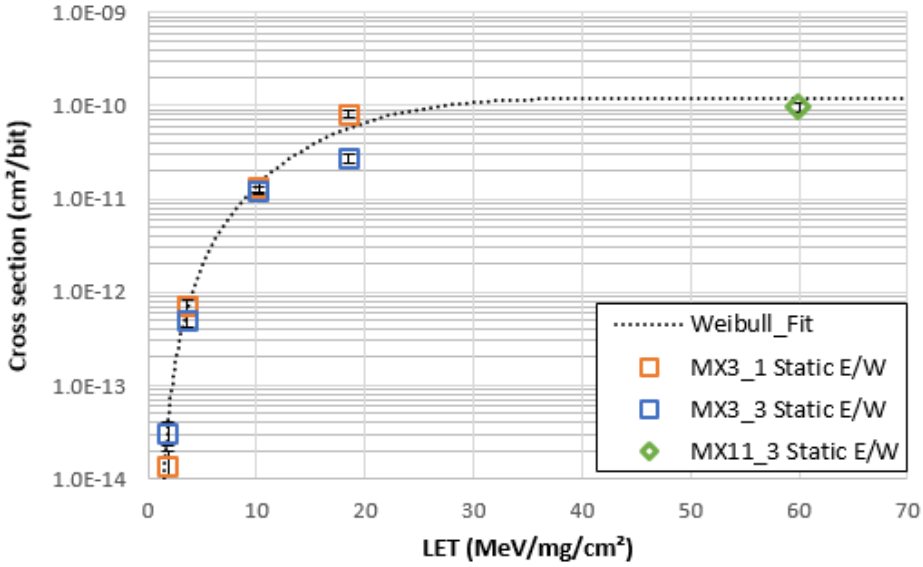
Erase/Write sequence

Results for “Erase/Write” sequence runs are given in Table 4. The SEU static value is computed from the blocks that are not used during read operation. The SEU dynamic value takes into account new errors after each E/W cycle but reject major SEFI (step failed and addresses or blocks continuously in error). The E/W mode suffered from several pages errors for LET above 10 MeV.cm²/mg.

Table 4: SEE results for "Erase/Write" sequence.

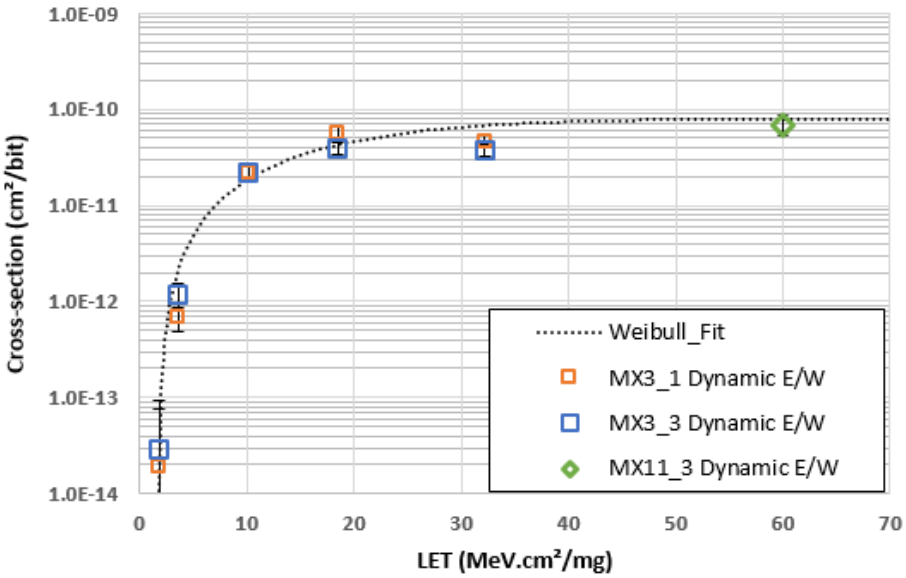
Facility	Campaign	Run number	DUT	Test mode	Ion	Fluence (ions/cm²)	LET (MeV.cm²/mg)	SEU - static	SEU - dynamic	SEFI	SBU	MBU (2)	MBU (3)	MBU (4)	Static SEU cross-section (cm²/bit)	Dynamic SEU cross-section (cm²/bit)	SEFI cross-section (cm²/DUT)
RADEF	1	67	1	E/W	N	1.00E+06	1.83	56	2	0	58	0	0	0	1.34E-14	1.91E-14	/
RADEF	1	36	1	E/W	Ne	1.00E+06	3.63	2964	72	0	3034	1	0	0	7.07E-13	6.87E-13	/
RADEF	1	40	1	E/W	Ar	1.00E+06	10.2	55706	2341	15	55022	461	161	405	1.33E-11	2.23E-11	1.50E-05
RADEF	1	58	1	E/W	Fe	1.00E+06	18.5	340154	5897	38	118780	4357	19791	39796	8.12E-11	5.62E-11	3.80E-05
RADEF	1	73	1	E/W	Kr	3.40E+05	32.2	/	1619	17	1296	10	9	290	/	4.54E-11	5.00E-5
RADEF	1	68	3	E/W	N	1.01E+06	1.83	128	3	0	131	0	0	0	3.02E-14	2.83E-14	/
RADEF	1	37	3	E/W	Ne	1.00E+06	3.63	2049	121	0	2170	0	0	0	4.89E-13	1.15E-12	/
RADEF	1	39	3	E/W	Ar	1.00E+06	10.2	51120	2322	17	51647	235	23	314	1.22E-11	2.21E-11	1.70E-05
RADEF	1	57	3	E/W	Fe	1.00E+06	18.5	111589	4085	49	112814	479	82	414	2.66E-11	3.90E-11	4.90E-05
RADEF	1	71	3	E/W	Kr	6.68E+05	32.2	/	1436	19	828	52	29	8141	/	3.71E-11	2.84E-05
RADEF	2	43	3	E/W	Xe	9.30E+04	60	37649	172	8	37685	36	0	16	9.66E-11	6.70E-11	8.60E-05

Devices lost their functionality during Krypton and Xenon test runs. This loss lead to most or all of the blocks erased and written being stuck to 0xFF even xhen the beam is off. In that case, the dynamic SEU value corresponds only to the first operations before the loss of functionality. SEFI registered in dynamic E/W mode are mostly page errors. Few block error and step failed occurred in the same proportion.
During the run number 43 (campaign 2), 2 SEL occurred under Xenon in E/W mode.



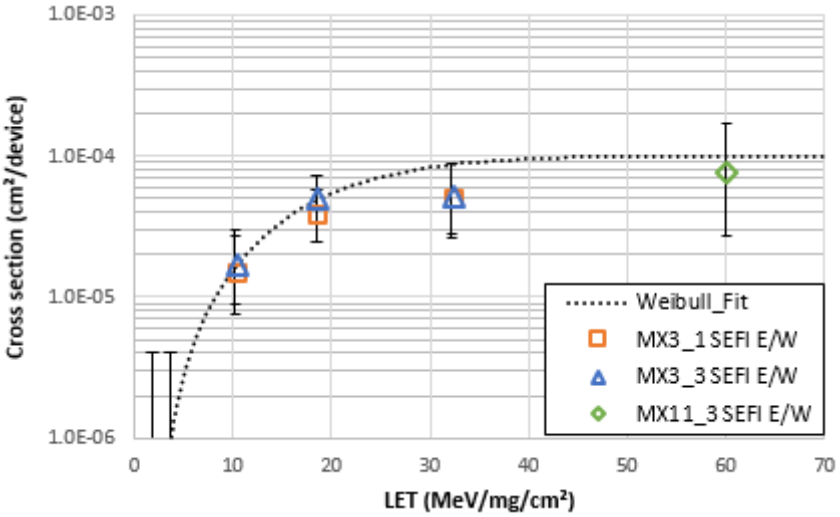
Weibull
W = 20.7
S = 2.5
x_0 = 1
Sat = 1.2E-10

Figure 11: SEU static cross-section for "Erase/Write" sequence.



Weibull
W = 20
S = 1.5
x_0 = 1.8
Sat = 8.0E-11

Figure 12: SEU dynamic cross-section for "Erase/Write" sequence.



Weibull
W = 20.7
S = 1.87
x_0 = 2
Sat = 1.0E-4

Figure 13: SEFI cross-section for "Erase/Write" sequence.

9.2 MBU contribution

SBU and MBU contributions are summarized in Table 5. For each test sequence, SBU are counted in the first line ("SBU"), MBU of size 2 or 3 are counted in the second line ("MBU < 4") and blocks with at least one MBU of size 4 are counted in the last line ("MBU ≥ 4"). Static errors for both Off and Read mode present the same ratio with almost all errors recorded being SBU.
MBU of size 4 are due to errors with all bits of a single word set to 1 or 0 hence inducing 4 bits in error for the data pattern used.
Once again, the E/W mode is more sensitive and presents the highest ratio of MBU.

Table 5: MBU contribution to overall block errors

Size	Read		Erase/Write		Off
	Static	Dynamic	Static	Dynamic	Static
SBU	99.98%	96.29%	84.06%	42.10%	99.98%
MBU < 4	0.02%	0.01%	6.26%	2.80%	0.02%
MBU ≥ 4	0%	3.70%	9.68%	55.10%	0%

9.3 SEL tests

Specific runs where carried out at high temperature. During these runs devices are in idle mode.
Some SEL occurred during dynamic tests at Vddmin and ambient temperature under Xenon. Current spikes are smaller than the ones recorded for specific SEL runs with amplitude below 0.3 A.

Table 6: SEL results for MX30LF4G18AC.

Facility	Campaign	Run	Board ID	DUT	Power	Test mode	Temperature	Ion	Fluence (ions/cm²)	LET	SEL	SEL cross section (cm²/device)
RADEF	1	92	mx 4	1	3.6 V	SEL	85°C	Xe	2.76E+06	60	119	1.94E-05
RADEF	2	44	mx 11	4	3.6 V	SEL	85°C	Xe	1.50E+06	60	115	7.67E-05
RADEF	2	41	mx 11	1	2.7 V	Read	Ambiant	Xe	1.00E+06	60	2	2.00E-06
RADEF	2	42	mx 11	4	2.7 V	Read	Ambiant	Xe	1.00E+06	60	2	2.00E-06
RADEF	2	43	mx 11	3	2.7 V	E/W	Ambiant	Xe	9.30E+4	60	2	2.15E-05

The chronogram for SEL run number 92 is given in Figure 14. SEL occurred on Vcc line (Icc current) with no abnormal behaviour on Vccq line.

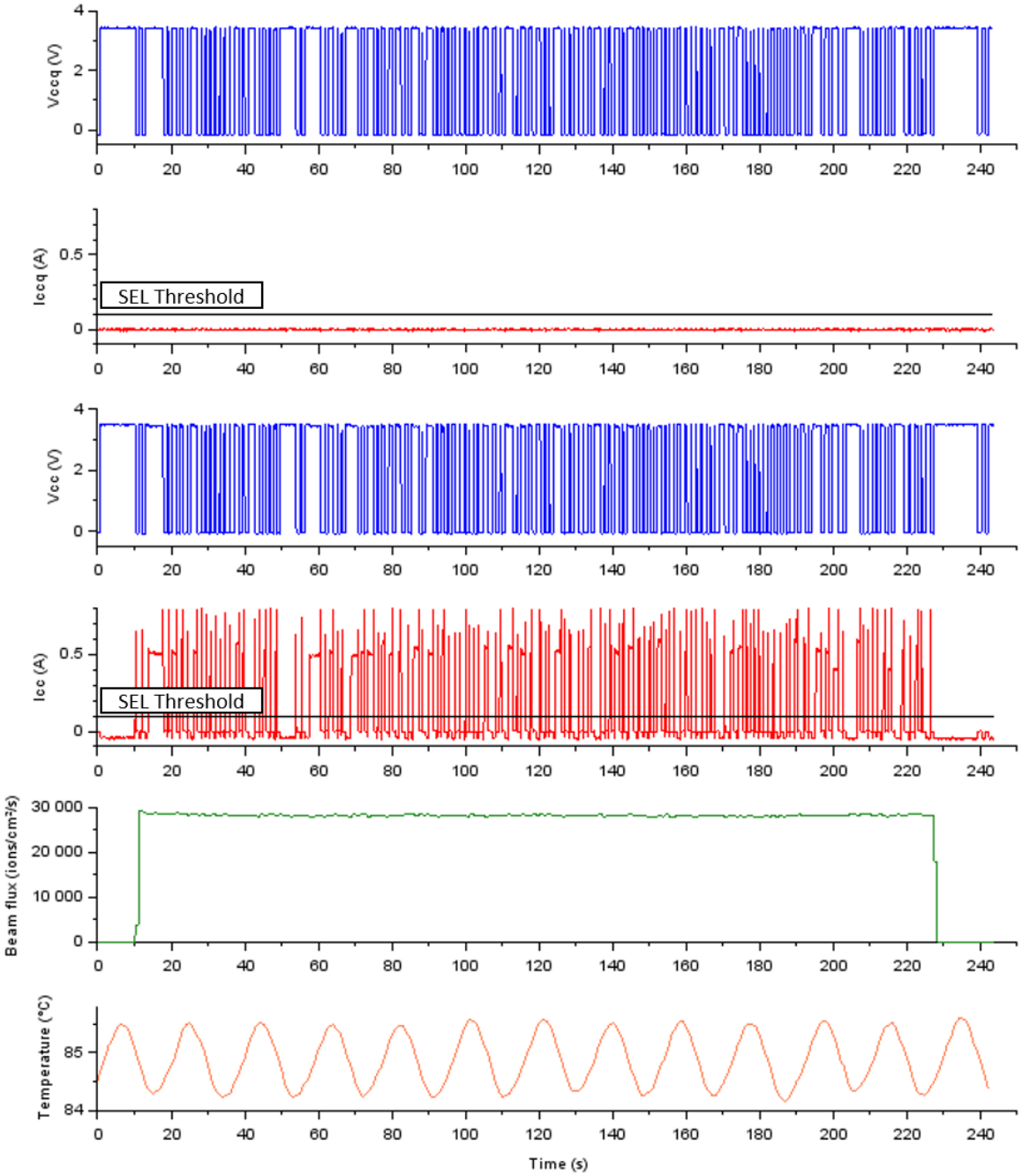


Figure 14: Campaign 1 run 92 chronograms for Vccq and Vcc lines along with temperature and flux.

The chronogram for SEL run number 44 is given in Figure 15. SEL detected were trigged by Icc. A small peak occurred on Iccq following an SEL trigged on Icc line when the power was turned off.

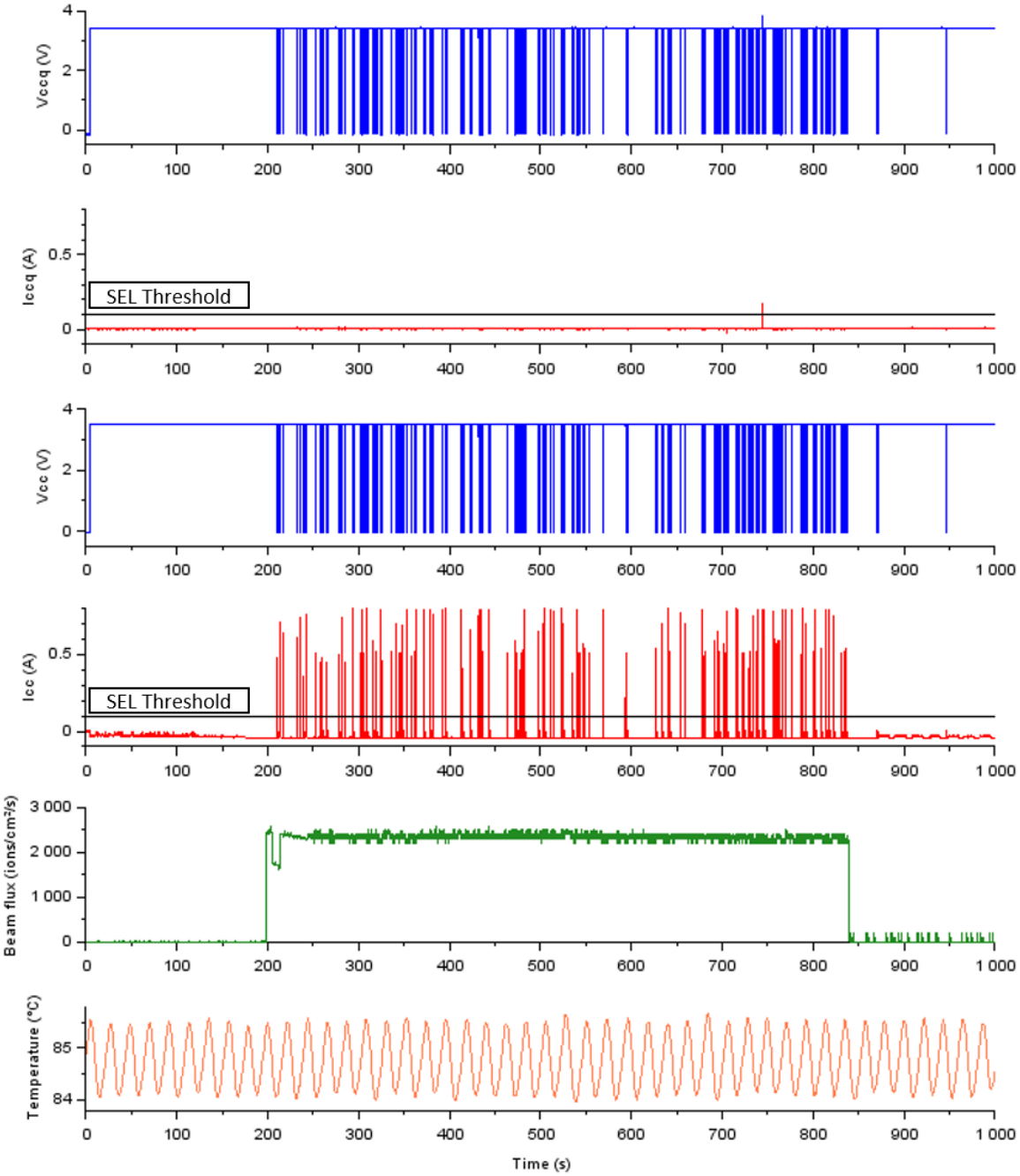


Figure 15: Campaign 2 run 44 chronograms for Vccq and Vcc lines along with temperature and flux.

The chronogram for “read” run number 41 is given in Figure 16. Two SEL were detected and trigged by Icc line.

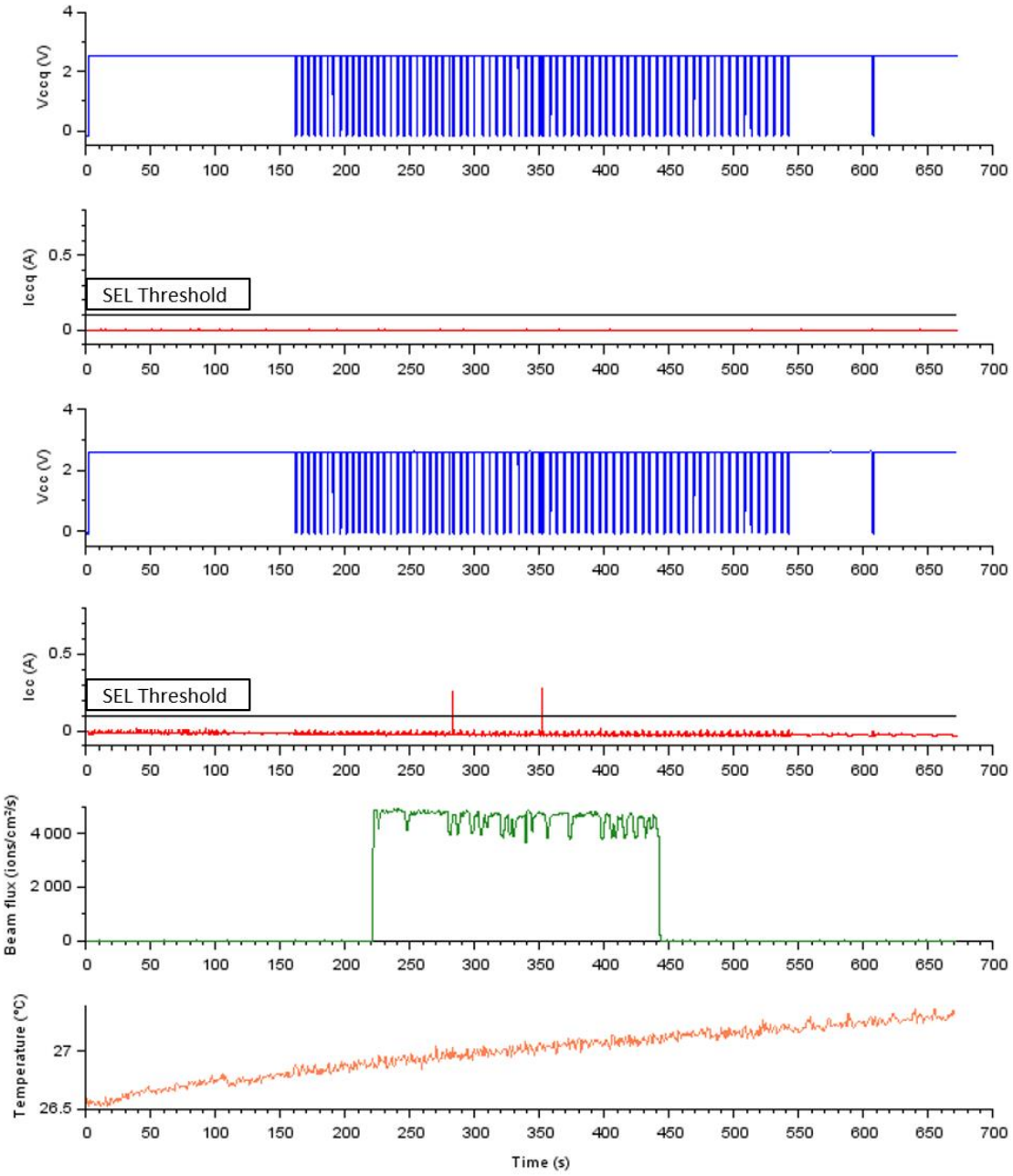


Figure 16: Campaign 2 run 41 chronograms for Vccq and Vcc lines along with temperature and flux.

The chronogram for “read” run number 42 is given in Figure 17. Two SEL were detected and trigged by Icc line.

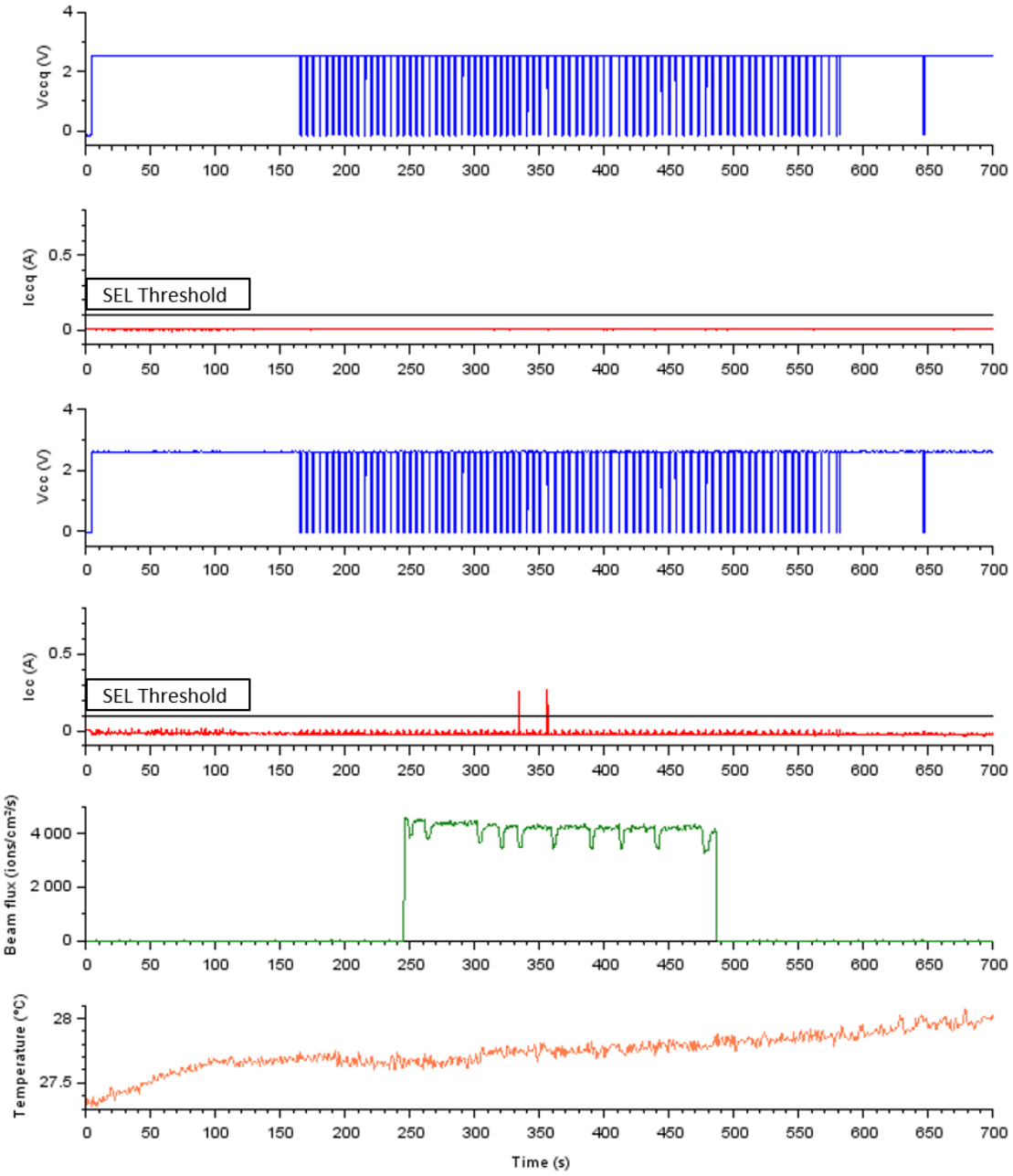


Figure 17: Campaign 2 run 42 chronograms for Vccq and Vcc lines along with temperature and flux.

The chronogram for “read” run number 43 is given in Figure 18. Two SEL were detected and triggered by Icc line.

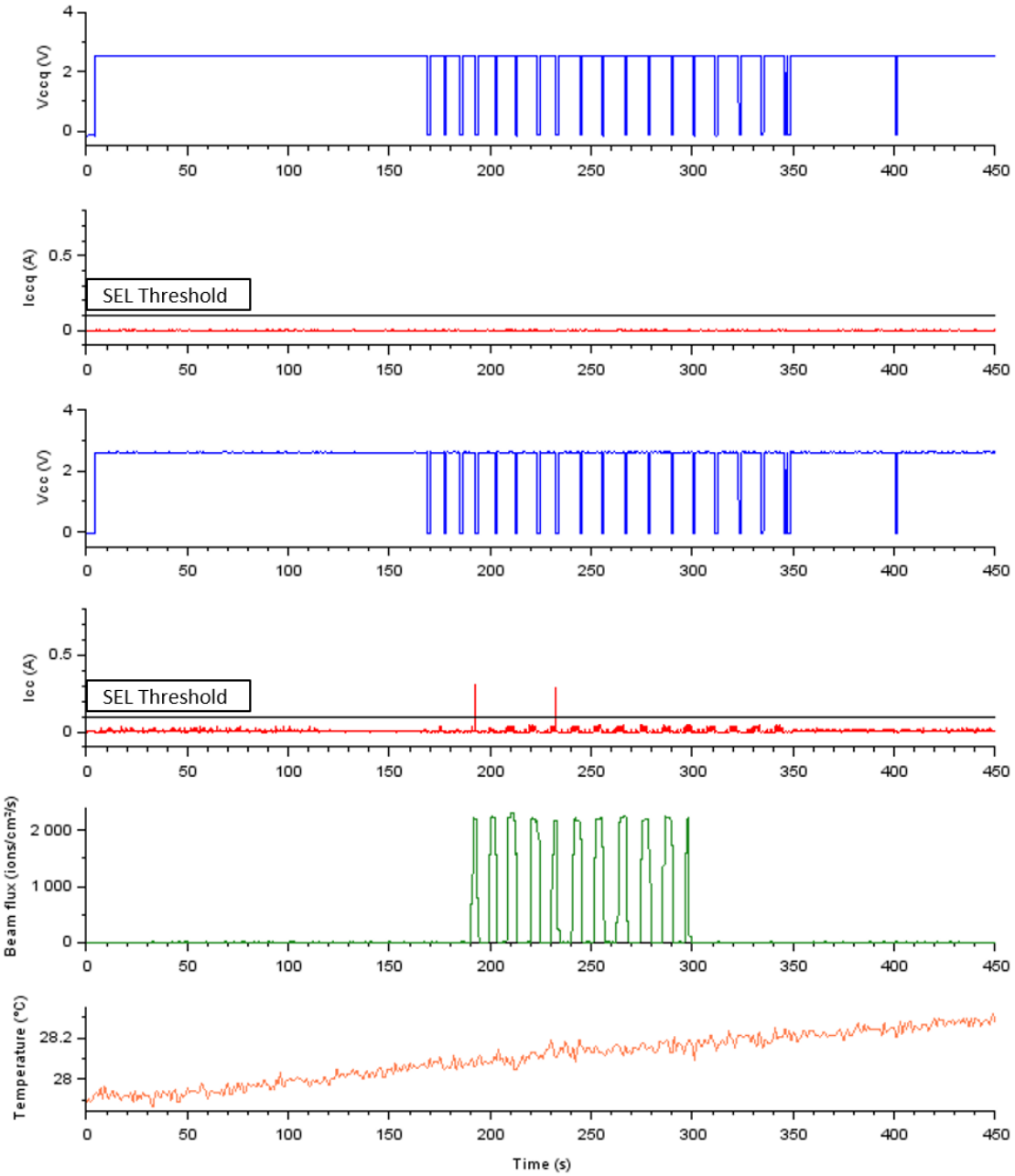


Figure 18: Campaign 2 run 43 chronograms for Vccq and Vcc lines along with temperature and flux.

10 Glossary

DUT: Device under test.

Fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.
In this document, Fluence is expressed in ions per cm^2.

Flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.
In this document, Flux is expressed in ions per $cm^2.s$.

Single-Event Effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.
Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL).

Single Event Gate Rupture (SEGR) **/ Single Event Dielectric Rupture (**SEDR**):** Destructive rupture of the gate oxide layer or dielectric layer by a single ion strike. This leads to leakage currents under bias and can be observed as stuck bits in digitals devices

Single-Event Upset (SEU)**:** A soft error caused by the transient signal induced by a single energetic particle strike.

Single-Event Transient (SET): A transient signal induced by a single energetic particle strike.

Single-Event Latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.
SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.
An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

Single-Event Functional Interrupt (SEFI): A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single-event burnout (SEB).
A SEFI is often associated with an upset in a control bit or register.

Error cross-section: the number of errors per unit fluence. For device error cross-section, the dimensions are cm^2 per device. For bit error cross-section, the dimensions are cm^2 per bit.

Tilt angle: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis

Weibull fit: $F(x) = A\,(1- \exp\{-[(x-x_0)/W]^s\})$ with:

x = effective LET in $MeV/(mg/cm^2)$;
F(x) = SEE cross-section in cm^2;
A = limiting or plateau cross-section;
x_0 = onset parameter, such that $F(x) = 0$ for $x < x_0$;
W = width parameter;
s = a dimensionless exponent.

Error bars: error bars are computed using a confidence level of 95% and a beam flux uncertainty of +/- 10% as recommended by Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100.