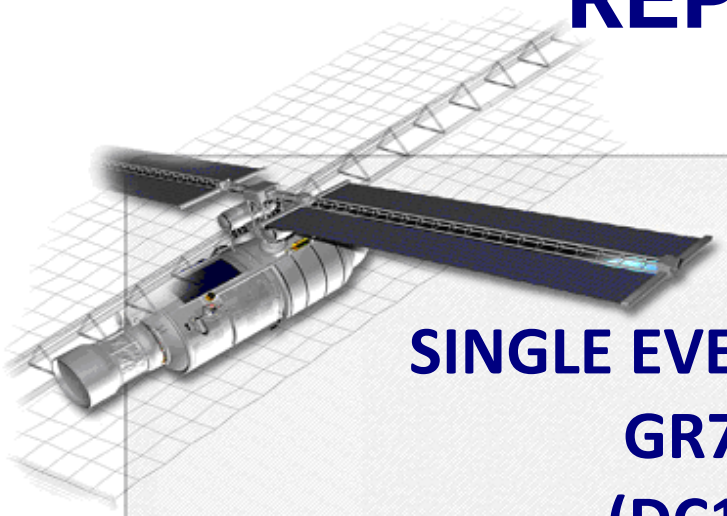
HEAVY IONS TEST REPORT



SINGLE EVENT EFFECTS
GR718A
(DC1411)
SpaceWire Router
from
Cobham Gaisler

TRAD/TI/GR718/XXX1/ESA/ELG/1501		Labège, January 19th, 2016
Tests & radiations afaq ISO 9001 Qualité AFNOR CERTIFICATION		TRAD, Bât Gallium 907, Voie l'Occitane - 31670 LABEGE France ☏: 05 61 00 95 60 Fax: 05 61 00 95 61 Email: trad@trad.fr Web Site: www.trad.fr SIRET 397 862 038 00056 - TVA FR59397862038
Written by	Verified by / Quality control	Approved by
E. LE GOULVEN **19/01/2016**	**P. GARCIA** **19/01/2016**	**A. VAROTSOU** **19/01/2016**

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To:	**ESA** **POIVEY Christian**	Project/Program: COO6 of Frame Contract Ref: ESTEC Contract No 4000105666/12/NL/Sfe

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1. Introduction

The aim of this study was to investigate on the Single Event Effect sensitivity of the GR718A, a SpaceWire Router developed by Cobham Gaisler, with respect to heavy ions.
The facility chosen to perform the irradiation was the U.C.L in Louvain-La-Neuve. The irradiation was performed under the direction of the Cobham Technical Officer Fredrik Sturesson.
This test was performed as part of an activity initiated by the European Space Agency (ESA). The test bench developed in collaboration with Cobham Gaisler allowed detecting Single Event Latchups (SELs), Single Event Upsets (SEUs) and Single Event Transients (SETs) on this device type.
After completion of this study, Cobham Gaisler has made a new revision of the SpaceWire Router, GR718B. The new revision is back compatible with the GR718A tested in this study. GR718B is implemented in the same technology. Thus, the results in this study on GR718A related to the technology, e.g. SEL, shall be relevant to the GR718B. However, the GR718B has been designed with new SEU mitigation concepts. Thus it may be expected that the GR718B will be less SEU sensitive compared to the results presented in this study for the GR718A.

This test was performed for ESA at U.C.L. in Louvain-La-Neuve from the 21st until the 25th of April 2015.
During the test two samples were irradiated.

2. Documents

2.1. Applicable documents

ESA Statement of Work: TEC-QEC/CP/SOW/2014-4 issue 1 dated 17/03/2015
Irradiation test plan: TRAD/ITP/ESA/COO6/ELG/120315 Rev. 1 dated 20/04/2015
Mail from Mr Sturesson Fredrik, dated 20/05/2015, subject “Re: Input for Testplan: GR718 SEE testing”.
Mail from Mr Sturesson Fredrik, dated 24/05/2015, subject “Final test plan GR718”.

2.2. Reference documents

Data Sheet: GR718 Advanced Data Sheet and User’s Manual, February 2014, Version 1.7
User’s Manual: GR718 Dynamic SEE Test Software, ERRATA_20150617, September 2013, Rev. 0.3
User’s Manual: GR718-BOARD Development Board User Manual, June 2014, Rev. 1.0
Schematic: GR718 Development Board Schematic, March 2014, Rev. 1.0
Mail from Mr Francisco Hernandez, dated 06/07/2015, subject “RE: Outcome of Test: GR718 SEE testing”.

3. Organization of Activities

The devices for the test were provided by Cobham Gaisler (2 parts). One part was provided delidded by Cobham Gaisler and the other part was delidded by TRAD. The testing board and the testing software were developed together by Cobham Gaisler and TRAD. Before the campaign the samples were checked and the test bench was validated at TRAD. The heavy ions campaign was performed by TRAD under the supervision of Mr Sturesson from Cobham Gaisler. The next table summarises the responsible entity for each activity of this project.

1	Procurement of Test Samples	Cobham Gaisler
2	Preparation of Test Samples (delidding)	Cobham Gaisler and TRAD
3	Preparation of Test Hardware and Test Program	Cobham Gaisler and TRAD
4	Samples Check out	TRAD
5	Accelerator Test	Cobham Gaisler and TRAD
6	Heavy Ion Test Report	TRAD

Table 1: Organization of activities

4. Parts information

4.1. Device description

The GR718A is a fault tolerant 18x SpaceWire Router compliant with ECSS-E-ST-50-12C (ESA's SpaceWire Standard). It supports SpaceWire Plug-and-Play. The architecture of the GR718A is centred on a non-blocking switch-matrix, which can connect any input port to any output port. Group adaptive routing is fully supported. The GR718A has two priority levels for output port arbitration. 16x of the SpaceWire ports come with on-chip LVDS. The additional 2x SpaceWire ports come with LVTTL for use with off-chip LVDS transceivers. The GR718A has an on-chip, high speed, bus which hosts UART and JTAG interfaces. The router also implements an internal configuration port and an internal port in SpaceWire In System Test (SIST).The GR718A has an internal PLL that allows the multiplication of the input clk or input SPWCLK by 0 (bypass), x2, x4 and x8. This allows an ample range of application conditions. The GR718A has an SPI interface and a GPIO interface accessible through the configuration port.

The GR718A SpaceWire router ASIC has been implemented with IMEC's Dare ASIC Technology v5.4, which is based on UMC's 180 nm CMOS process. Except for 108 non-hardened FF placed at the ports (parity corrected). The rest of FF used on this ASIC are SEU hardened by design.

4.2. Identification

Type:	GR718A
Manufacturer:	Cobham Gaisler
Function:	SpaceWire Router

4.3. Procurement information

Packaging:	CQFP256
Date code:	1411
Serial numbers:	001, 003
Others No.:	W#02SW75032
Sample size:	2 parts provided by Cobham Gaisler

4.4. Sample Preparation

One part was delidded by TRAD and one part was delidded by Gaisler. A functional test sequence was performed on delidded samples to check that the devices were not degraded by the delidding operation.
Before performing the heavy ion test, the whole system (delidded samples, test boards and software) were assembled and tested by TRAD at V.A.S.C.O (Vacuum System for Californium Operation).

4.5. Sample pictures

4.5.1. External view

Figure 1: Package marking (SN001)

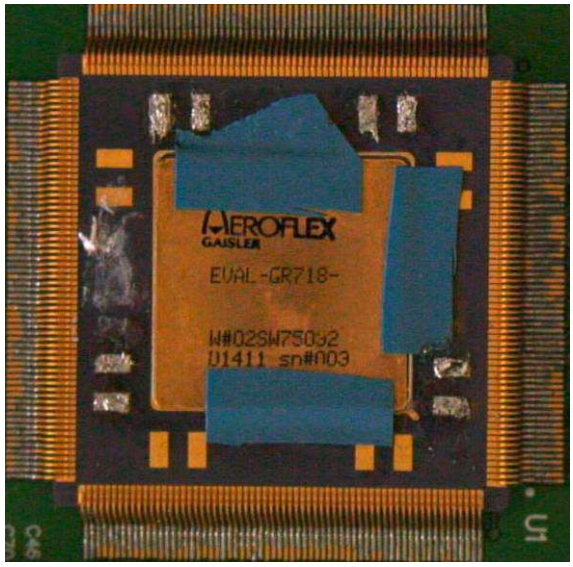


Figure 2: Package marking (SN003)

4.5.2. Internal view

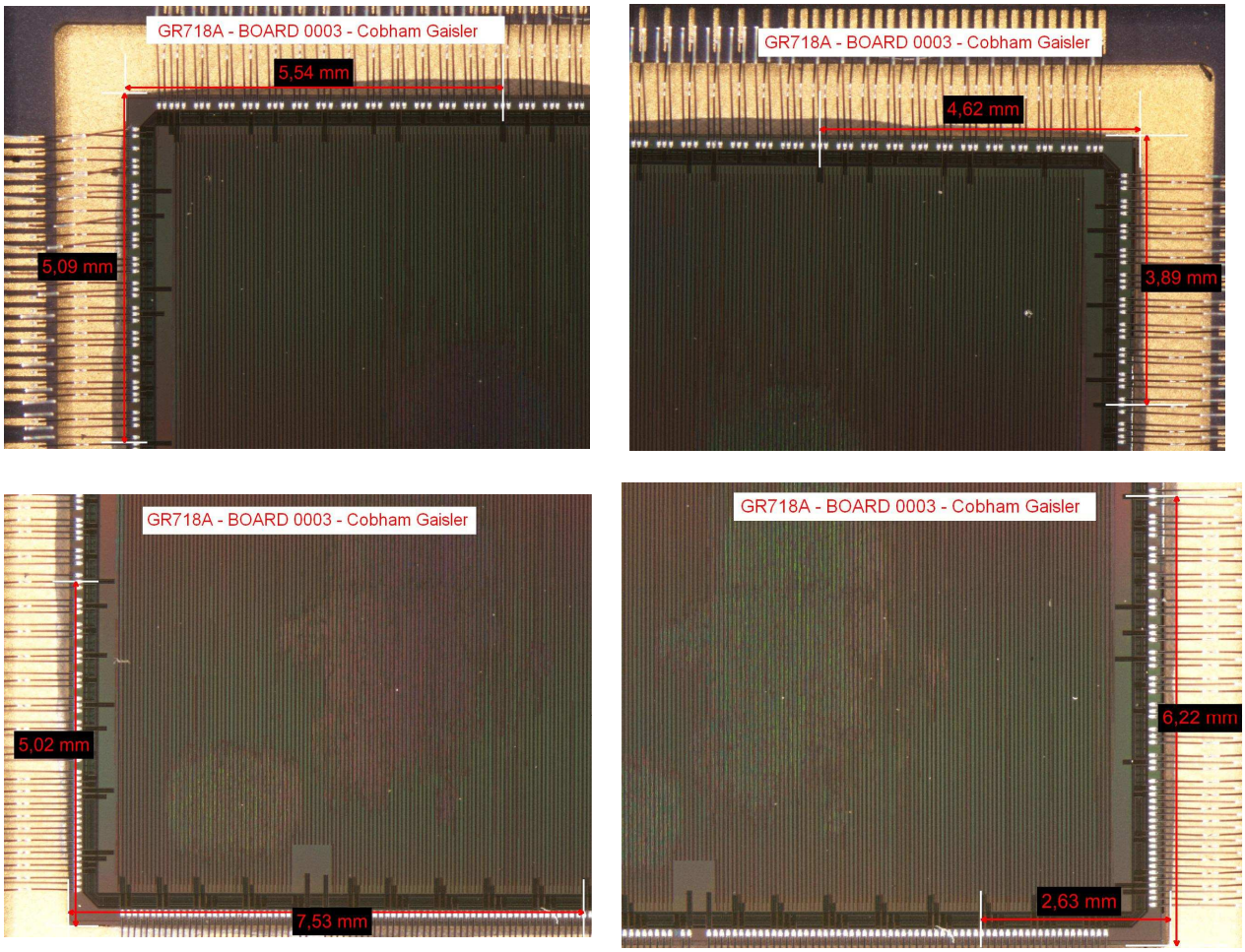


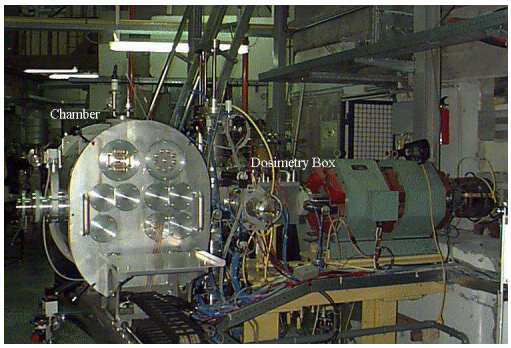
Figure 3: Internal overall view of SN003

5. Dosimetry and Irradiation Facilities

The test was performed at U.C.L (Université Catholique de Louvain) on April 21 to 25, 2015. Two delidded samples were irradiated.

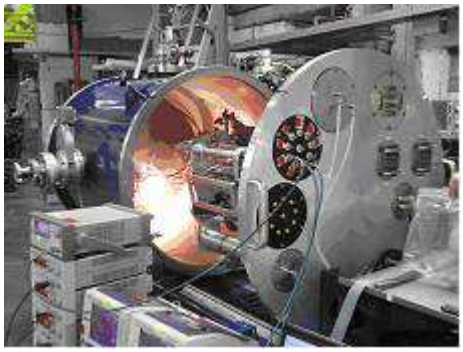
5.1. UCL Heavy Ion Test Facility (Université Catholique de Louvain - Belgique)

The CYClotron of LOuvain la NEuve (CYCLONE) is a multi-particle, variable energy, cyclotron capable of accelerating protons (up to 85 MeV), alpha particles and heavy ions.
For the heavy ions, the covered LET range is between 1.2 MeV.cm².mg^{-1} and 67.7 MeV.cm².mg^{-1}. Heavy ions available are separated in two "Ion Cocktails" named M/Q=5 and M/Q=3.3.



One of the main advantages of the UCL Heavy Ion Test Facility is the fast changing of ion species. Within the same cocktail, it takes only a few minutes to change from one ion to another.

The chamber has the shape of a barrel stretched vertically; its internal dimensions are 71 cm in height, 54 cm in width and 76 cm in depth. One side flange is used to support the board frame (25 X 25 cm) and user connectors.
The chamber is equipped with a vacuum system.



5.2. Dosimetry

To control and monitor the beam parameters, a dosimetry box is placed in front of the chamber.
It contains a faraday cup, 2 Parallel Plate Avalanche Counters (PPAC).
Two additional surface barrier detectors are placed in the test chamber.
The faraday cup is used during beam preparation at high intensity.
A beam uniformity measurement is performed with a collimated surface barrier detector. This detector is placed on a X and Y movement. The final profile is drawn and the ± 10 % width is calculated. The Homogeneity is ± 10 % on a 25 mm diameter.
During the irradiation, the flux is integrated in order to give the delivered total fluence (particule.cm^{-2}) on the device.

5.3. Beam characteristics

The beam flux can vary between a few particles and 1,61E+4 $cm^{-2}.s^{-1}$. The flux is set depending on the device sensitivity. At UCL, available Heavy ions are separated to Ion Cocktails, one for the High LET (M/Q=5) and a second one for the High Range (M/Q=3.3). Here bellow, are given the characteristics of each cocktail. During the campaign, the irradiations were performed with the High LET cocktail ions highlighted in yellow in Table 2 and with the High Range cocktail ions highlighted in yellow in Table 3.

Ion	Energy (MeV)	Range (µm(Si))	LET (MeV.cm².mg^{-1})
$^{15}N^{3+}$	60	59	3.3
$^{20}Ne^{4+}$	78	45	6.4
$^{40}Ar^{8+}$	151	40	15.9
$^{84}Kr^{17+}$	305	39	40.4
$^{124}Xe^{25+}$	420	37	67.7

Table 2: UCL cocktail M/Q=5

Ion	Energy (MeV)	Range (µm(Si))	LET (MeV.cm².mg^{-1})
$^{13}C^{4+}$	131	292	1.1
$^{22}Ne^{7+}$	235	216	3
$^{40}Ar^{12+}$	372	117	10.2
$^{58}Ni^{18+}$	567	100	20.4
$^{83}Kr^{25+}$	756	92	32.6

Table 3: UCL cocktail M/Q=3.3

6. Test Procedure and Setup

6.1. Test procedure

6.1.1. Description of the test method

The target fluence for the SEL tests was 1e+7 ions cm-2. The target fluence for SEU/SET tests was 5e+6 ions cm-2.
The run was terminated when the maximum fluence was reached or when over one hundred errors were detected.
Before each run, a reset command was sent to the Device Under Test (DUT).

6.1.2. SEL Test Principle

A maximum operating voltage value was applied to the DUT: V_{DD}I/O=+3.6V and V_{DD}Core=+1.95V. A square signal of 12.5MHz and 100MHz was applied on the CLK input and the SPWCLK input respectively with PLL bypassed.
To warm the DUT to 125°C, two resistive patches were pasted on the top of the package and a PT1000 was used to control the temperature.
TRAD has developed a fully integrated test bench to perform Single Event Latchup tests (SEL). The GUARD system (Graphical Universal Autorange Delatcher) allows the user to easily protect his device under test and perform SEL characterization.
The power supply was applied to the DUT through the GUARD system.
The threshold current of the GUARD system was set according to the nominal current. If the nominal current exceeded the threshold current, the GUARD system was triggered and the event was counted as SEL. Then, the GUARD system sent a trigger command to the oscilloscope, maintaining the power supply during a defined time, called Time hold, (Th=1ms) and cutting off during a defined time, called Time cut, (Tc = 7 ms). Then, the power supply was restarted with the nominal current expected consumption.
At the end of each run, the test program read the Local Scope Counter of the oscilloscope and downloaded the recorded current waveforms to store them.

Figure 4 shows an example of the SEL detection.

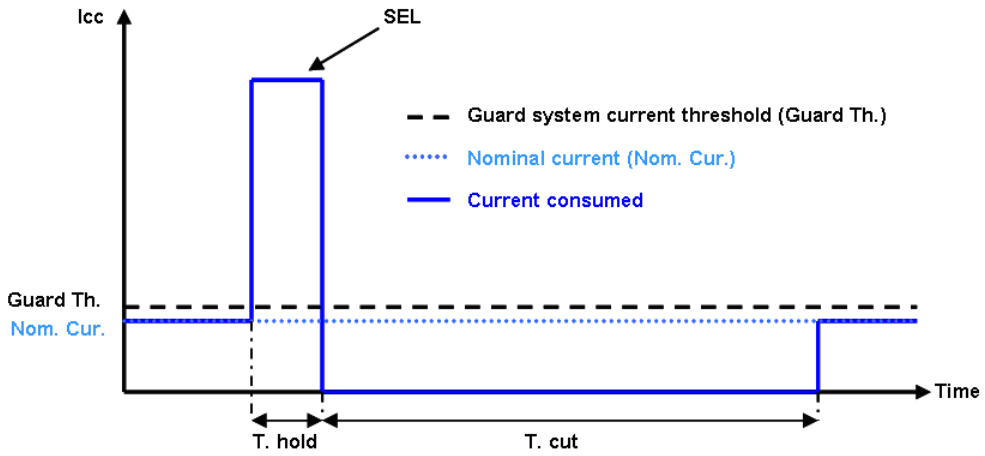


Figure 4: Common SEL characteristic.

6.1.3. SET Test Principle

A +3.3V supply voltage was applied on V_{DD}I/O. On V_{DD}Core, three different voltage values were applied +1.65V, +1.8V and +1.95V. The clock signal CLK was set at a range between 0MHz (for a static test) and 50MHz. The clock signal SPWCLK was set at a range between 10MHz and 100MHz according to the test plan.
A Single Event Transient is an event described by a voltage amplitude and a timing parameter.
The PLL LOCK is a digital output signal, it was monitored and when the internal PLL unlocked, this signal went to zero, thus an event was counted.
For this purpose, one trigger threshold (negative) was used to detect the amplitude voltage due to SET. An SET was detected when the output device voltage became lower than 1.5V. During the test, the internal counter of the oscilloscope was incremented at each detected SET and the waveform of each transient was stored.

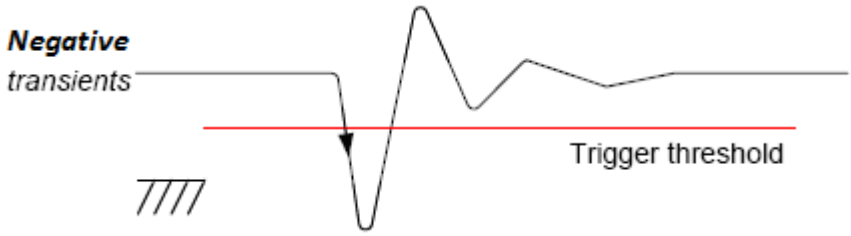


Figure 5: SET detection

At the end of each run, the test program read the Local Scope Counter of the oscilloscope and downloaded the records currents waveforms to store them.

6.1.4. SEU Test Principle

During this test, a nominal voltage value was applied to the DUT: VDDI/O=+3.3V and VDDCore=varied between +1.65 and +1.95V. The clock signal CLK was set to a range between 10MHz and 50MHz according to the test plan, and SPWCLK was set to 100MHz.
As detailed on the next paragraphs, the test was performed in two modes, static mode and dynamic mode. For the static configuration, the 32-bit registers, described on Table 5, were read at the beginning of the run and checked during the irradiation (see §6.1.4.1).
For the dynamic configuration, the SIST (**S**paceWire **I**n-**S**ystem **T**est described in datasheet section 7) of the router SpaceWire was used to send data packets to all ports that had been set in a daisy chain (see §6.1.4.2).
During the irradiation the inputs of the GR718A were set as described, for the static test, on Table 4. In Dynamic testing all these settings were overwritten before the test started by writing to the internal configuration registers of GR718A.

Pins Name	State
CFGLOCK	0
SPWCLKDIV[5:0]	0x01
SPILLIFNOTREADY	0
PNPEN	0
LINKSTARTONREQ	0
AUTODCONNECT	0
STATICROUTEEN	0

Table 4: GR718A input configuration

6.1.4.1. Static Test

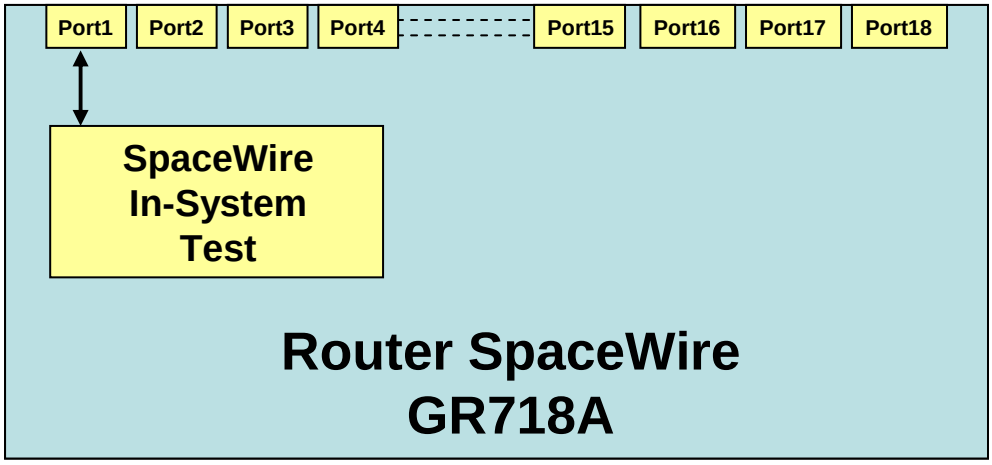


Figure 6: Configuration of the DUT during the static test

Figure 6 gives an overview of the configuration of the DUT during the static test. All ports were setup in internal loop back and two scripts were used, the first to enable the SIST by enabling its clock and the second to disabling it, by disable its clock. These scripts were called "StaticSEE_script3_withSISTclk.tcl" and "StaticSEE_script3_noSISTclk.tcl", respectively. They control the SIST clock with the register SYSTEST.CFG2 bit 4(EN).
The static test was performed in two modes:

- One with the external CLK running during testing.
- One with the external CLK switched OFF during testing.

The CLK frequency ranged between 0MHz and 50MHz and the SPWCLK frequency ranged between 10MHz and 100MHz according to the test plan.

The GR718A has 760x32 user accessible bit registers that could be monitored, they are summarized in Table 5. Each 32-bit register values were compared by the script during the irradiation in order to detect any modification.

Register name	Register acronym	AMBA address
SpaceWire Router registers		
Routing table port mapping, physical addresses 1-19	RTR.RTPMAP	0xFFF20004 - 0xFFF2004C
Routing table port mapping, logical addresses 32-255	RTR.RTPMAP	0xFFF20080 - 0xFFF203FC
Routing table address control, physical addresses 1-19	RTR.RTACTRL	0xFFF20404 - 0xFFF2044C
Routing table address control, logical addresses 32-255	RTR.RTACTRL	0xFFF20480 - 0xFFF207FC
Port control, ports 1-19 (SpaceWire ports and SIST port)	RTR.PCTRL	0xFFF20840 - 0xFFF2084C
Port status, ports 1-19 (SpaceWire ports and SIST port)	RTR.PSTS	0xFFF20884 - 0xFFF208CC
Port timer reload, ports 0-19	RTR.PTIMER	0xFFF20900 - 0xFFF2094C
Port control 2, ports 1-19 (SpaceWire ports and SIST port)	RTR.PCTRL2	0xFFF20984 - 0xFFF209CC

Router configuration / status	RTR.RTRCFG	0xFFF20A00
Time-code	RTR.TC	0xFFF20A04
Version / instance ID	RTR.VER	0xFFF20A08
Initialization divisor	RTR.IDIV	0xFFF20A0C
Configuration write enable	RTR.CFGWE	0xFFF20A10
Timer prescaler reload	RTR.PRESCALER	0xFFF20A14
Interrupt mask	RTR.IMASK	0xFFF20A18
Interrupt port mask	RTR.IPMASK	0xFFF20A1C
Port interrupt pending	RTR.PIP	0xFFF20A20
Interrupt-code generation	RTR.ICODEGEN	0xFFF20A24
Interrupt-code distribution ISR	RTR.ISR	0xFFF20A28
Interrupt-code distribution ISR timer reload	RTR.ISRTIMER	0xFFF20A30
Interrupt-code distribution ACK-to-INT timer reload	RTR.AITIMER	0xFFF20A34
Interrupt-code distribution ISR change timer reload	RTR.ISRCTIMER	0xFFF20A38
SpaceWire link running status	RTR.LRUNSTS	0xFFF20A40
Capability	RTR.CAP	0xFFF20A44
SpaceWire Plug-and-Play - Device Vendor and Product ID	RTR.PNPVEND	0xFFF20A50
SpaceWire Plug-and-Play - Unit Vendor and Product ID	RTR.PNPUVEND	0xFFF20A54
SpaceWire Plug-and-Play - Unit Serial Number	RTR.PNPUSN	0xFFF20A58
Outgoing character counter, ports 1-19	RTR.OCHARCNT	0xFFF20C10, 0xFFF20C20 ... 0xFFF20D30
Incoming character counter, ports 1-19	RTR.ICHARCNT	0xFFF20C14, 0xFFF20C24 ... 0xFFF20D34
Outgoing packet counter, ports 1-19	RTR.OPKTCNT	0xFFF20C18, 0xFFF20C28 ... 0xFFF20D38
Incoming packet counter, ports 1-19	RTR.IPKTCNT	0xFFF20C1C, 0xFFF20C2C ... 0xFFF20D3C
Maximum packet length, ports 0-19	RTR.MAXPLEN	0xFFF20E00 - 0xFFF20E4C
Credit counter, ports 1-18	RTR.CREDCNT	0xFFF20E80 - 0xFFF20EC8
General purpose out, bits 0-31	RTR.GPOA	0xFFF20F00
General purpose out, bits 32-48	RTR.GPOB	0xFFF20F04
General purpose in, bits 0-1	RTR.GPIA	0xFFF20F10
SpaceWire Address Register 0-7	SIST.ADDR[0-7]	0xFFE00200 - 0xFFE0021C
SpaceWire In-System Test registers		
Protocol ID and Polynomial Register	SIST.PID	0xFFE00220
Seed Register	SIST.SEED	0xFFE00224
Packet Length Register	SIST.LEN	0xFFE00228
Control Register	SIST.CTRL	0xFFE0022C
Error Register 0	SIST.ERROR0	0xFFE00230
Error Register 1	SIST.ERROR1	0xFFE00234
Error Register 2	SIST.ERROR2	0xFFE00238
Packet Counter Register	SIST.PKTCNTR	0xFFE0023C

Timer Register 0	SIST.TIMER0	0xFFE00240
Timer Register 1	SIST.TIMER1	0xFFE00244
Status Register	SIST.STAT	0xFFE00248
State Register	SIST.STATE	0xFFE0024C
Transmitter Byte Count Register	SIST.TXBYTECNTR	0xFFE00250
Receiver Byte Count Register	SIST.RXBYTECNTR	0xFFE00254
Time-Code Register	SIST.TIME	0xFFE00258
Protection Register	SIST.PROT	0xFFE0025C
Data Input Registers 0 - 7	SIST.DIN[0-7]	0xFFE00280 - 0xFFE0029C
Data Output Registers 0 - 7	SIST.DOUT[0-7]	0xFFE002A0 - 0xFFE002BC
UART interface registers		
AHB UART status register	UART.STS	0xFFE00004
AHB UART control register	UART.CTRL	0xFFE00008
AHB UART scaler register	UART.SCALE	0xFFE0000C
SPI Controller registers		
Capability register	SPI.CAP	0xFFF22000
Mode register	SPI.MODE	0xFFF22020
Event register	SPI.EVENT	0xFFF22024
Mask register	SPI.MASK	0xFFF22028
Command register	SPI.CMD	0xFFF2202C
Transmit register	SPI.TX	0xFFF22030
Receive register	SPI.RX	0xFFF22034

Table 5: GR718A registers monitored

6.1.4.2. Dynamic Test

For this test, the DUT was configured in two different modes, internal or external loopback:

- Internal loopback is a test mode available in GR718A where the port output is looped back to the port input internally in the device.
- External loopback, the port output data is wired on PCB (or with connectors, to another or the same) port input.

Notice: External loopback in this testing shall not be mixed with the external loop back mode described in section 12 of the datasheet.

In order to set the DUT in external loopback, specific Cobham Gaisler daughter boards were used except on port #1 as illustrated on Figure 7. The internal PLL , fed by the CLK input or SPWCLK input signals, was used to change the clock frequency of the SpaceWire link. The SPWCLKSEL[2:0] input signals of GR718A, described in Table 6, was set before every run to choose the configuration of the internal PLL in order to increase the data rate of the SpaceWire link. When the PLL was bypassed, the data rate was determined by the SPWCLK input signal.

SPWCLKSEL[2:0]	Internal SpaceWire clock
000	SPWCLK (PLL bypassed)
001	2 x CLK (SPWCLK unused)
010	4 x CLK (SPWCLK unused)
011*	8 x CLK (SPWCLK unused)
100*	1 x SPWCLK
101	2 x SPWCLK
110*	4 x SPWCLK
111	8 x SPWCLK

Table 6: Internal SpaceWire clock muxing

*: These SPWCLKSEL configurations were not used during the experiment.

A further modification of the data rate transmission was performed with arguments in the test software. These controlled the link rate speed per port by means of the link rate divider registers in GR718A (RTR.PCTRL.RD). Three modes were used during testing:

- Full: 100% data rate on all ports
- Derated: data rate was divided by 2 on all ports
- Port No.18 Derated: 100% data rate on all ports except Port No. 18.

When derating the data rate in the ports, it was the transmission data that was derated while the clock frequency remained unaffected. Thus comparing error cross sections between the "Full" and "Derated" modes, using the same clock frequency, could provide evidence about the cause of the errors if they were related to the actual data amount passing through the SpaceWire router or not.

With the "Port No.18 Derated" mode, only the last port in the daisy chain was derated. Thus the amount of data passing through the SpaceWire router was equal to the "Derated" mode. However, since all ports before port No.18 run with full data rate, Port No. 18 acted as a bottleneck for all data and all internal FIFOs in all ports became filled-up. Thus in this mode the amount of data stored in the SpaceWire Router, that may have been susceptible to SEUs, was higher compared to the other two modes.

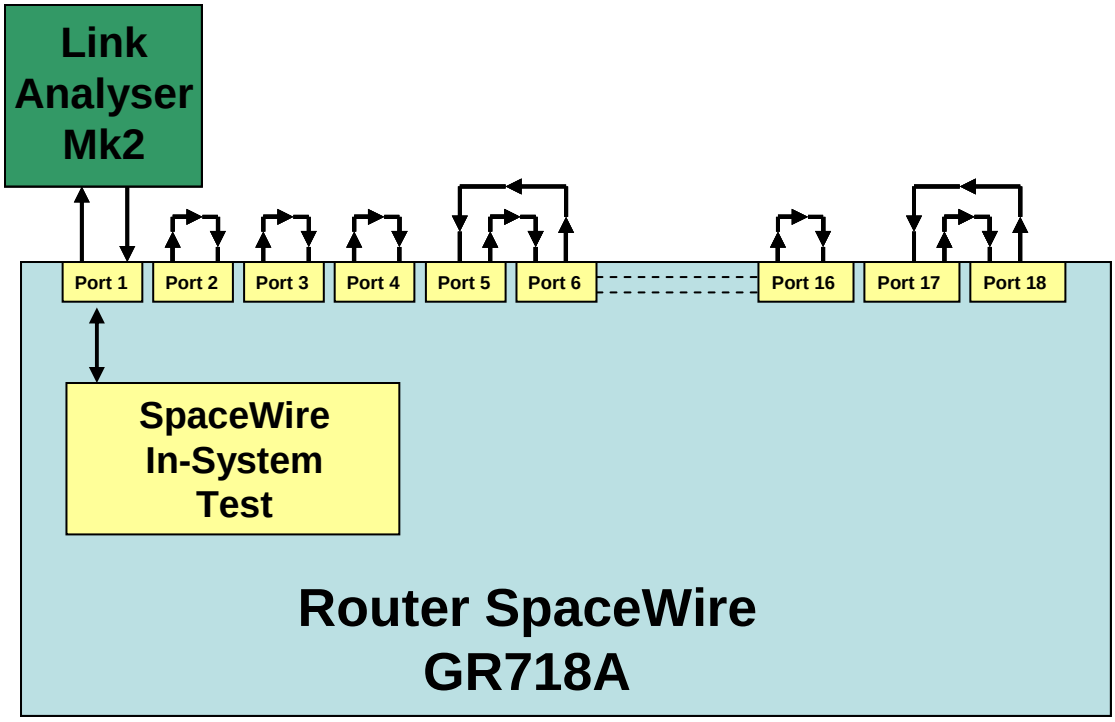


Figure 7: Configuration of the DUT during the dynamic test with external loopback

The GR718A dynamic test software was intended for SEU testing and monitoring the GR718A using the on-chip SpaceWire In System Test (SIST). It is tcl-based for operation for GRMON2 software running on a host computer communicating with the GR718A through its debug interface. The test software initiated and configured the GR718A as well as the SIST engine. The actual testing was carried out by the SIST while the test software monitored status registers, collected error statistics and printed out results to screen as well as log files. The test software monitored not only status and error registers of the SIST but also other essential registers like the PLL status register and the port status registers.

After the test bench initialization, three processes run asynchronously during the dynamic test:

- The SIST engine generates test data (SpaceWire packets) and detects errors when the data are returned back from the SpaceWire Router.
- Each port of the SpaceWire Router maintains its link with the port it is connected to. The port transfers received SpaceWire packets to the router. The packet routed to the port address defined in the header part of the packet.
- The test software on the host computer poll the SIST status registers, the port status registers and the PLL status register. When an error is recorded, the event is reported to the log file and counted. The type of error recorded defines the type of action taken by the test software. The GR718A may be re-initiated or it may proceed without action polling for next event.

At the beginning of each run, it is possible to select which ports to use with the port address defined in the header of the packet. For the majority of runs all ports were used except for ports No. 16 and No. 17. With this configuration the non-used ports were in run-state but with no SpaceWire data being transmitted. With external loopback, port No. 17 received SpaceWire data since it was wired to Port No.18 transmitting SpaceWire data.

The packet format was similar to the commands defined for the RMAP protocol [RMAP]:

- SpW Address (0 to 31 bytes), programmable through the SIST.ADDRx registers
- Logical Address (1 byte), programmable through the SIST.ADDR0 register
- Protocol ID (1 byte), programmable through the SIST.PID field
- Transaction Identifier (2 bytes) (i.e. seed), programmable through the SIST.SEED register
- Data Length (3 bytes), programmable through the SIST.LEN register
- Header CRC (1 byte as per [RMAP], covering header from Logical Address, inclusive)
- Data (0 to 16 MiB-1) (data is a pseudo-random generated bit string based on the seed)
- Data CRC (1 byte as per [RMAP], covering all Data bytes)
- End-Of-Packet

The data field contents are generated from a Linear Feedback Shift Register (LFSR) that is shifted 8 times for each data byte. The implementation uses a Galois version of LFSR.
For this test the data length was set to $08FFFF and the generator polynomial was configured to $g(x)=x^{16}+x^5+x^3+x^2+x^0$.

The link analyser Mk2 of Star Dundee was connected to port 1 to probe the SpaceWire link. It was setup in loop back mode and was set to trigger on all errors. For every error detected a file .lad was saved manually.

6.2. Test bench description

6.2.1. Preparation of test hardware and program

TRAD developed a VHDL code for the FPGA board and a test board to configure the DUT and to communicate with it. Cobham Gaisler developed three specific scripts for dynamic test and two for static test. Loopback boards were used during dynamic tests when the internal loopback system was disabled.

The GUARD System of TRAD was used to monitor the current consumption and to detect potential SELs.

A Star Dundee Link Analyser Mk2 was used to monitor the Space Wire traffic over one spacewire port and to trigger when an event occured. A backup of each event was performed for every error.

The test system was driven by a personal computer through a standard IEEE488 communication interface. All signals were delivered and monitored by this equipment and SEE curves were saved in its memory.
At the end of each test run, data was transferred to the hard disk for storage.
An overall description of the test system is given in Figure 8.

Before performing the heavy ion test, the whole system (delidded sample, test board and software) was assembled and tested by TRAD at V.A.S.C.O (Vacuum System for Californium Operation).

6.3. Test Bench details

The test bench consisted of: a main board (Figure 9) and loopback daughter boards (Figure 10) developed by Cobham Gaisler; one board developed by TRAD; an FPGA board with a Xilinx FPGA Spartan3; a GUARD System; a SpaceWire link analyser; two oscilloscopes and a laptop.
The test board developed by TRAD (Figure 11) was used to configure the DUT with the FPGA board and to communicate through UART with it.
The Space Wire Link Analyser Mk2 was used to detect and to store the errors on the Space Wire link.
One oscilloscope was set to detect the potential loss of LOCK signal and the second one to capture the current waveforms if a latchup occurred.
The laptop was used to save the detected errors, but also to configure and to communicate with the Space Wire Link Analyser Mk2, the FPGA board and the DUT through the UART using GRMON2 software.

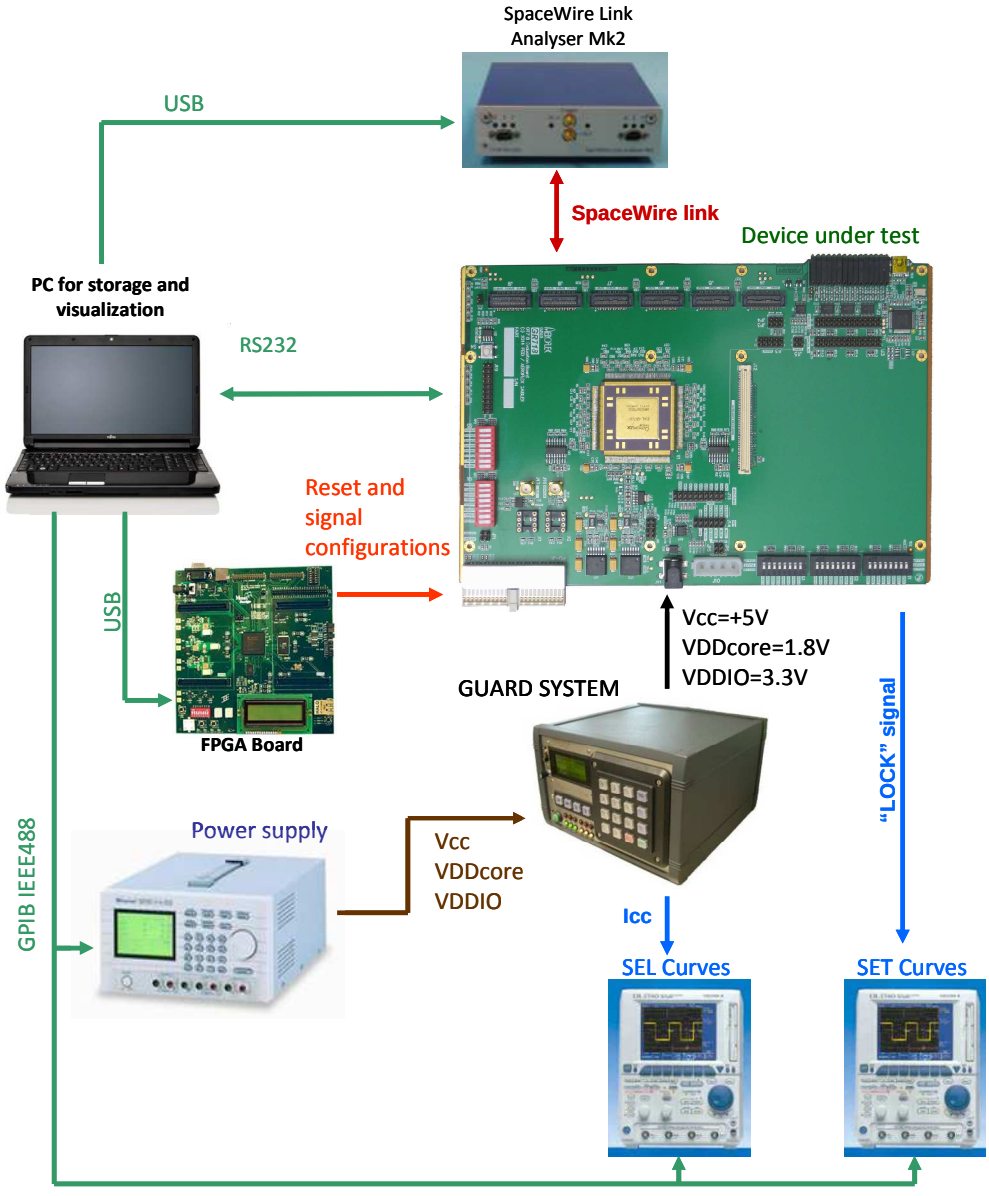


Figure 8: Test system description

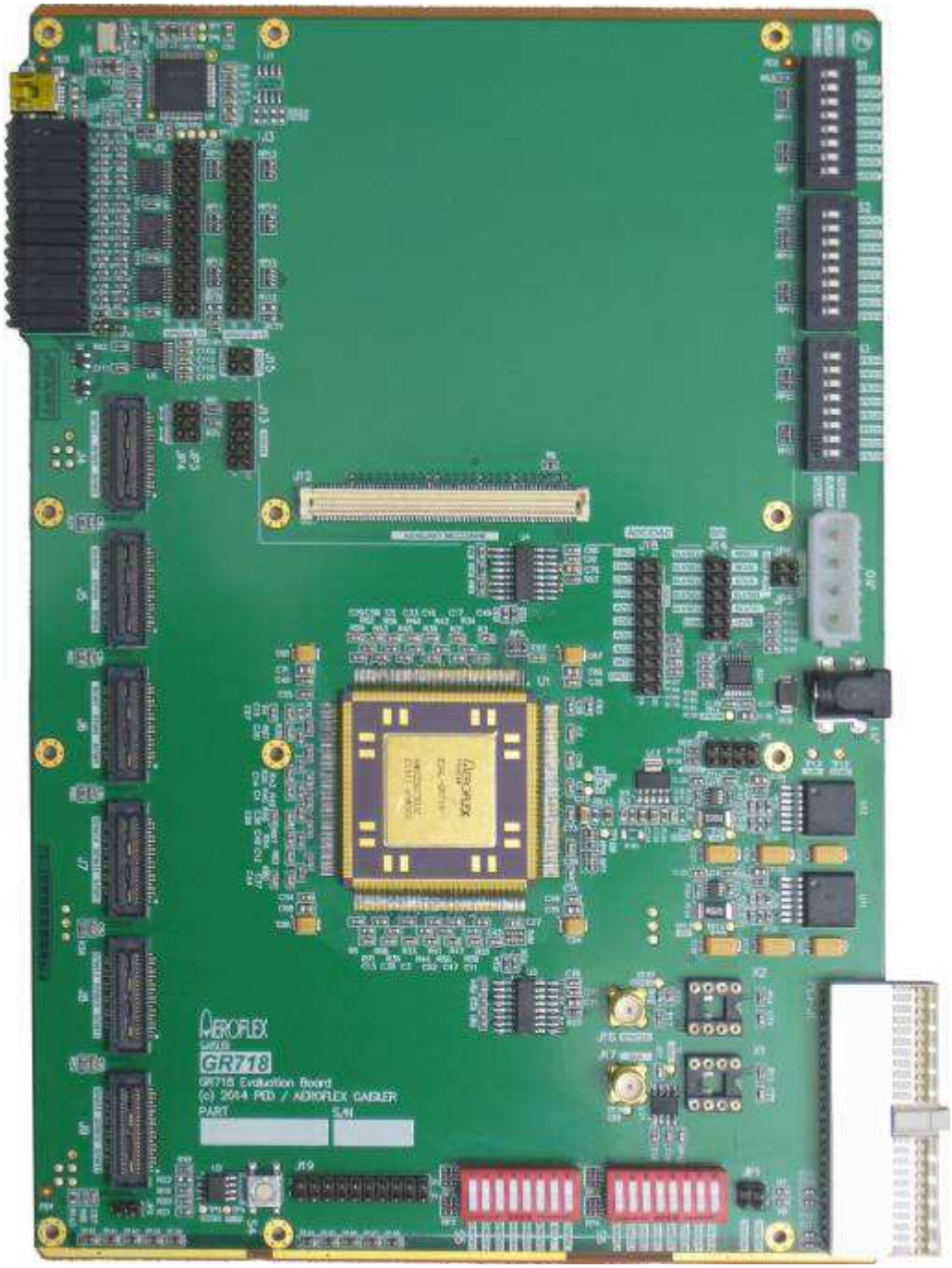


Figure 9: Main Test board developed by Cobham Gaisler, top view

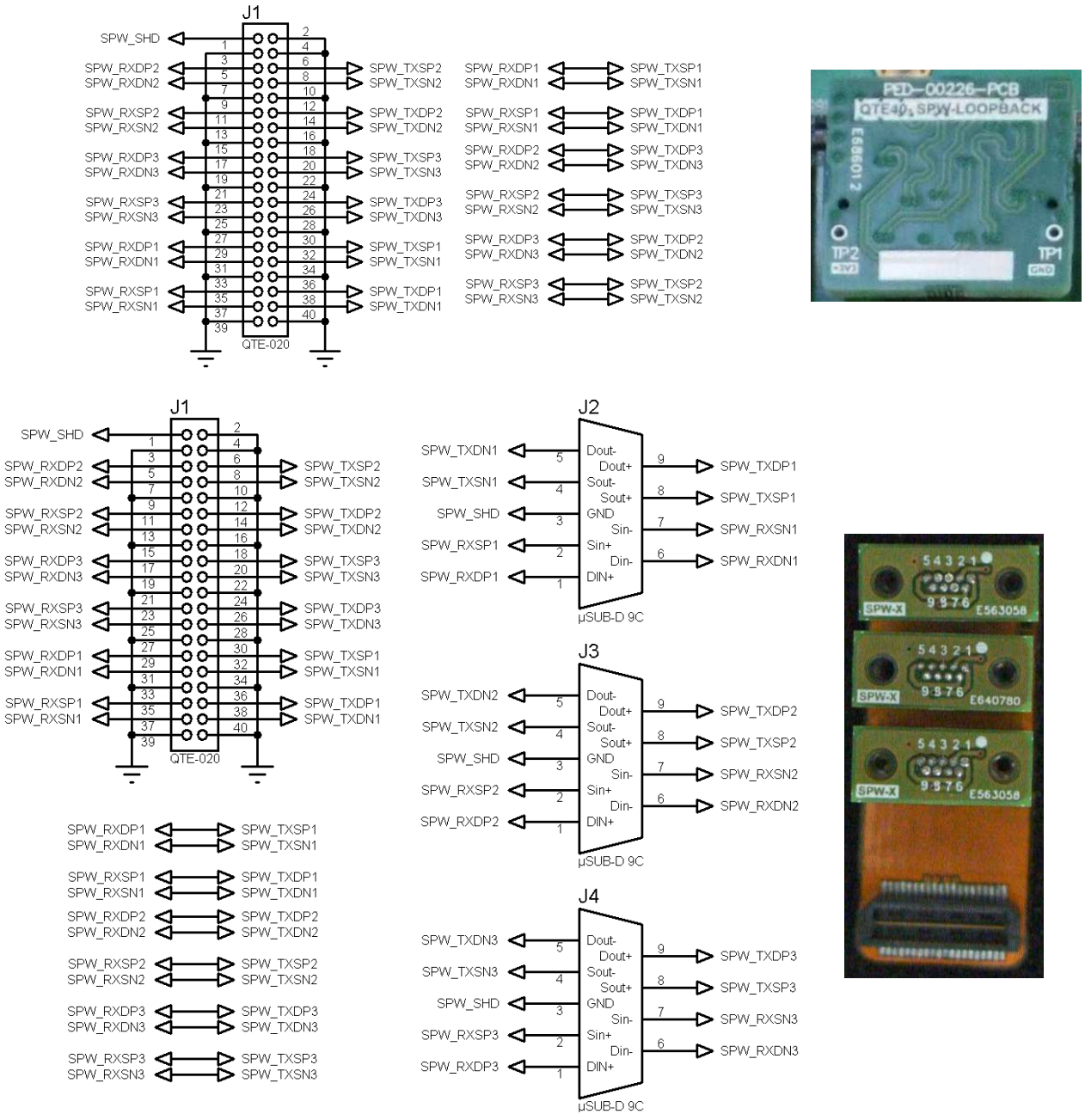
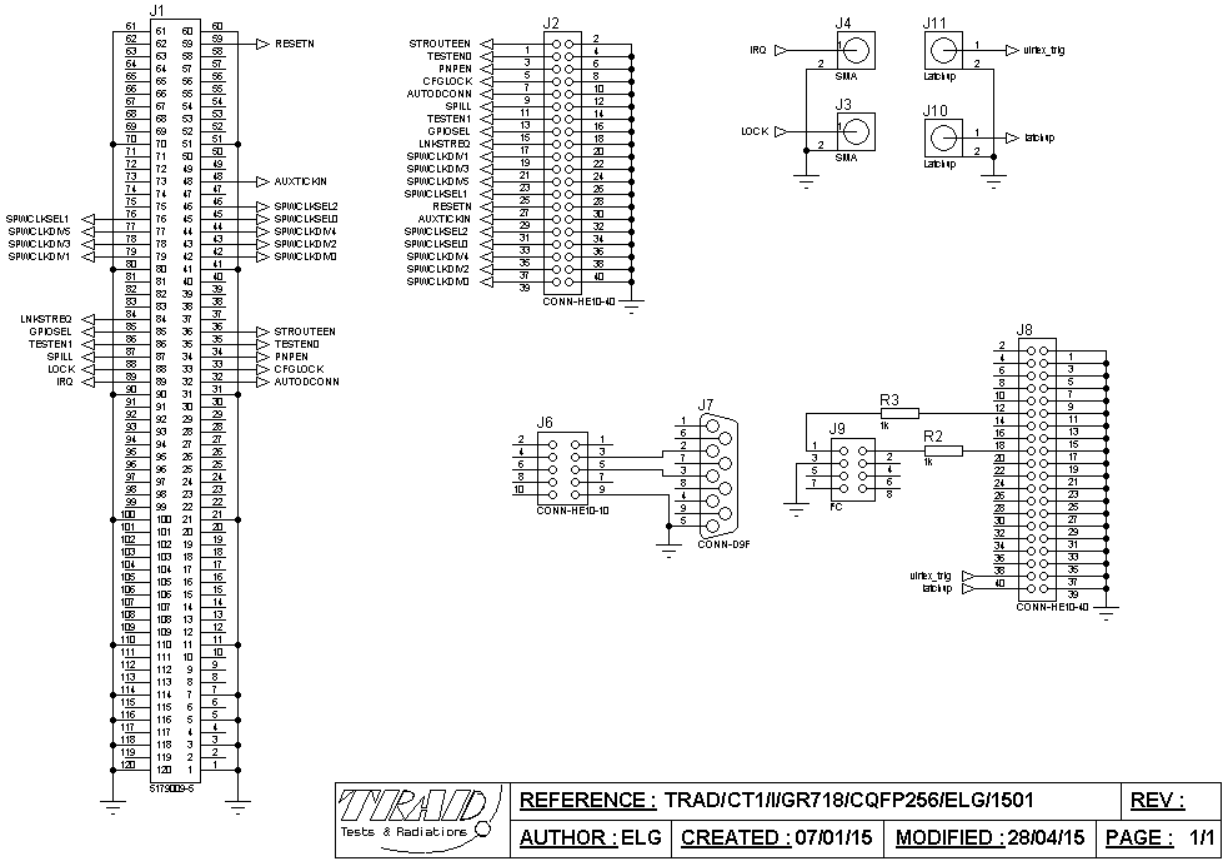


Figure 10: Test boards developed by Cobham Gaisler

The loopback daughter boards shown on Figure 10, were plugged on the six Samtec connectors of the main board to loopback the eighteen ports of router. One flex board was plugged on Samtec connector of port#1, 2 and 3, in order to connect the SpaceWire Link Analyser on the port#1, for the port#2 and 3 the boards (observable on the right hand side on Figure 10, noted SPW-X) are used to allow the external loopback connection.



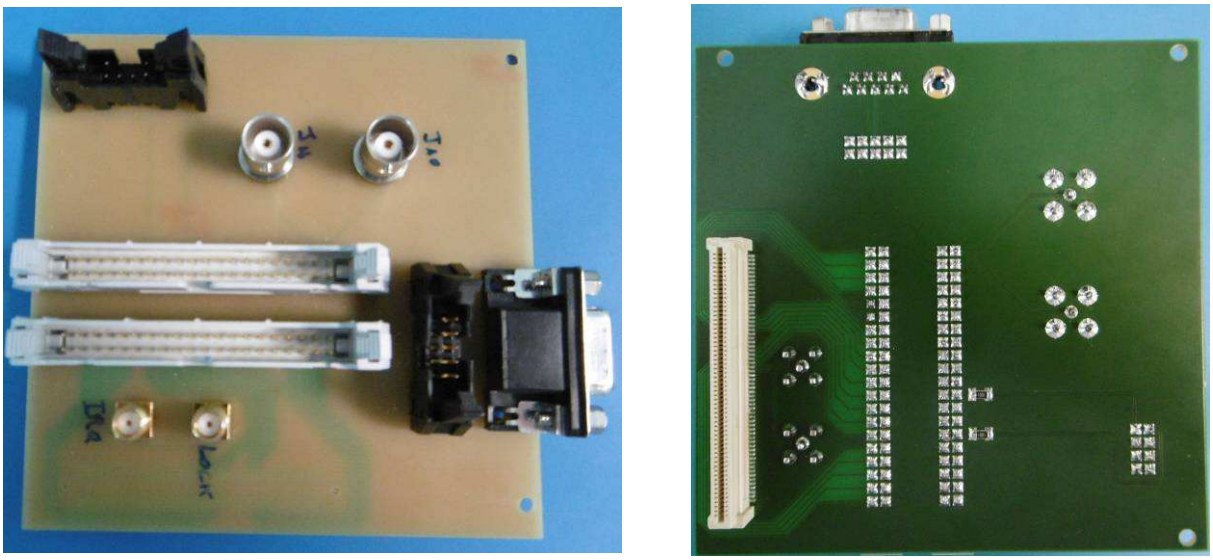


Figure 11: Test board developed by TRAD

The TRAD test board shown on Figure 11, was plugged on the white Samtec connector (name J1) of the main board. The FPGA can be connected on the two HE10-40 connectors (name J2 and J8), but for the test only J2 was used. The SMA connector J3 was connected on the oscilloscope to monitor the LOCK signal. The Sub-D connector J7 and the HE10 connector J6 were used to connect the serial communication of the laptop.

The HE10 connectors J8 and J9 can be used to read with the FPGA board, the consumption for each power supply through I²C link.

6.4. Test equipment identification

The tests were carried out with evaluation test boards developed by Cobham Gaisler and with an additional TRAD test bench.

COMPUTER	PO-TE-059
REF. TEST BOARD	TRAD/CT1/I/GR718/CQFP256/ELG/1501 GR718 Development Board Rev 1.0 Cobham Gaisler loopback boards
EQUIPMENT	ME-77, SM-92, MI-55, MI-60
TEST PROGRAM	GR718_TI_XXX1_V10.spf GR718_TI_XXX1_V10.bat GR718_TI_XXX1_V10.bit GR718_TI_XXX1_V10.mcf SIST_test_SEE_TRAD0v4b.tcl* SIST_test_SEE_TRAD0v4c.tcl* SIST_test_SEE_TRAD0v4d.tcl* StaticSEE_script3_noSISTclk.tcl StaticSEE_script3_withSISTclk.tcl

*: These three test programs are identical w.r.t testing but with different formats of reporting

6.4.1. Device setup and Test conditions

The trigger threshold used during SEL test is shown in the following table:

	V_{DD}I/O	V_{DD}Core
Guard System channel	1	2
Vcc	3.6V	1.95V
$I_{threshold}$	600mA	500mA
T_{hold}	1ms	1ms
T_{cut}	7ms	7ms
Temperature	125°C*	125°C*

Table 7: SEL detection threshold

*: This was targeted temperature, but was not achieved in all tests

7. RESULTS

7.1. Summary of runs.

The choice of the configuration tested and the fluence for each run were taken with the supervision of Mr F. Sturesson from Cobham Gaisler to optimise test time. The fluence, where loss of communication occurred had to be corrected to compensate the time for the run where no error counting took place. The following runs terminated abnormally: 9, 18, 19, 21, 26, 31 and 49. For that reason, their effective fluence had to be calculated. These effective fluences were used to calculate the cross-sections of SEUs.
Hereafter are presented the runs performed during this campaign. The main table of runs was divided into multiple tables to allow better visibility of the results.

GR718A CLK= 0MHz to 50MHz ; SPWCLK= 100MHz SEL: VDDI/O=+3.6V and VDDCore=+1.95V SEU, SET: VDDI/O=+3.3V and VDDCore=+1.65V to +1.95V																						SEU			SET		SEL			
Run	Part	T°	Type	Baud Rate	PLL	Mode	CLK (MHz)	Data Rate ports 1-15 (Mbps)	Data Rate port 18 (Mbps)	Script	Vcore	Ion	Energy (MeV)	Tilt (°)	Eff. LET (MeV.cm²/mg)	Eff. Range (µm Si)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Estimated Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	Lost UART Com	Post analysis Data	Cross Section (cm²/device)	Lock	Cross Section (cm²/device)	Vcore	Cross Section (cm²/device)	Vio	Cross Section (cm²/device)
High LET M/Q=5																														
1	1	125	SEL	FULL	0	Static	12,5	100	100	NoSist	1,95	124Xe 26+	420	0	67.70	37.0	6.97E+03	262	1.83E+06	-	1.978	1.978	No	55	3.01E-05	0	-	0	<5.48E-07	0	<5.48E-07
2	1	25	SET/SEU	FULL	0	Static	50	100	100	NoSist	1,95	124Xe 26+	420	0	67.70	37.0	9.78E+03	212	2.08E+06	3.72E+05	2.257	4.235	Yes	16	4.30E-05	0	<4.80E-07	-	-	-	-
3	1	25	SET/SEU	FULL	0	Static	50	100	100	NoSist	1,95	124Xe 26+	420	0	67.70	37.0	9.15E+03	42	3.84E+05	2.01E+05	0.416	4.651	Yes	11	5.46E-05	0	<2.60E-06	-	-	-	-
4	1	25	SET/SEU	FULL	0	Static	0	100	100	WithSist	1,95	124Xe 26+	420	0	67.70	37.0	9.97E+03	154	1.54E+06	-	1.863	6.314	Yes	-	-	0	<6.51E-07	-	-	-	-
5	1	25	SET/SEU	FULL	0	Static	0	100	100	WithSist	1,95	124Xe 26+	420	0	67.70	37.0	9.55E+03	211	2.02E+06	-	2.183	8.497	No	1	4.96E-07	0	<4.96E-07	-	-	-	-
6	1	25	SET/SEU	FULL	0	Static	0	100	100	WithSist	1,65	124Xe 26+	420	0	67.70	37.0	9.46E+03	213	2.00E+06	-	2.166	10.664	No	2	1.00E-06	0	<5.00E-07	-	-	-	-
7	1	25	SET/SEU	FULL	0	Static	50	100	100	NoSist	1,65	124Xe 26+	420	0	67.70	37.0	9.26E+03	217	2.00E+06	-	2.166	12.830	No	171	8.55E-05	0	<5.00E-07	-	-	-	-
8	1	25	SET/SEU	FULL	2	Dyn	20	40	40	Dyn 4b	1,8	124Xe 26+	420	0	67.70	37.0	2.42E+03	588	1.42E+06	-	1.542	14.372	No	80	5.62E-05	0	<7.03E-07	-	-	-	-
9	1	25	SET/SEU	FULL	2	Dyn	20	40	40	Dyn 4b	1,8	124Xe 26+	420	0	67.70	37.0	4.34E+03	336	1.46E+06	1.44E+06	1.580	15.951	No	53	3.69E-05	1	6.86E-07	-	-	-	-
10	1	25	SET/SEU	Derated 18	2	Dyn	20	40	20	Dyn 4b	1,8	124Xe 26+	420	0	67.70	37.0	4.62E+03	649	3.00E+06	-	3.250	19.201	No	204	6.80E-05	0	<3.33E-07	-	-	-	-
11	1	25	SET/SEU	Derated 18	4	Dyn	50	200	100	Dyn 4b	1,8	124Xe 26+	420	0	67.70	37.0	5.01E+02	499	2.51E+05	-	0.271	19.472	No	85	3.39E-04	0	<3.99E-06	-	-	-	-
12	1	25	SET/SEU	Derated 18	4	Dyn	50	200	100	Dyn 4b	1,8	84 Kr 17+	305	0	40.40	39.0	6.73E+02	156	1.05E+05	-	0.068	19.540	Yes	-	-	0	<9.52E-06	-	-	-	-
13	1	25	SET/SEU	Derated 18	4	Dyn	50	200	100	Dyn 4b	1,8	84 Kr 17+	305	0	40.40	39.0	9.58E+02	337	3.23E+05	-	0.209	19.749	No	93	2.88E-04	0	<3.10E-06	-	-	-	-
14	1	25	SET/SEU	FULL	4	Dyn	50	200	200	Dyn 4b	1,8	84 Kr 17+	305	0	40.40	39.0	1.12E+03	400	4.47E+05	-	0.289	20.038	No	70	1.57E-04	0	<2.24E-06	-	-	-	-
15	1	25	SET/SEU	Derated	4	Dyn	50	100	100	Dyn 4b	1,8	84 Kr 17+	305	0	40.40	39.0	9.86E+02	451	4.45E+05	-	0.287	20.325	No	74	1.66E-04	0	<2.25E-06	-	-	-	-
16	1	25	SET/SEU	FULL	2	Static	50	100	100	NoSist	1,65	84 Kr 17+	305	0	40.40	39.0	4.69E+03	249	1.17E+06	9.80E+05	0.758	21.083	Yes	80	8.17E-05	0	<8.53E-07	-	-	-	-
17	1	25	SET/SEU	FULL	2	Static	50	100	100	WithSist	1,65	84 Kr 17+	305	0	40.40	39.0	3.96E+03	259	1.03E+06	8.27E+05	0.665	21.748	Yes	56	6.77E-05	0	<9.72E-07	-	-	-	-
18	3	80	SEL	FULL	0	Static	12,5	100	100	NoSist	1,95	124Xe 26+	420	0	67.70	37.0	1.05E+04	951	1.00E+07	8.62E+06	10.832	10.832	No	219	2.54E-05	-	-	0	<1.00E-07	0	<1.00E-07
19	3	80	SEL	FULL	0	Static	12,5	100	100	NoSist	1,95	124Xe 26+	420	60	135.40	18.5	7.35E+03	1363	1.00E+07	5.09E+06	21.664	32.496	No	136	2.67E-05	-	-	0	<1.00E-07	0	<1.00E-07
20	3	25	SET/SEU	FULL	2	Dyn	20	40	40	Dyn 4b	1,8	124Xe 26+	420	0	67.70	37.0	5.27E+03	950	5.00E+06	-	5.416	37.912	No	301	6.02E-05	0	<2.00E-07	-	-	-	-
21	1	85	SEL	FULL	0	Static	12,5	100	100	NoSist	1,95	124Xe 26+	420	0	67.70	37.0	1.04E+04	968	1.00E+07	5.38E+06	10.832	32.580	No	126	2.34E-05	-	-	0	<1.00E-07	0	<1.00E-07
22	1	85	SEL	FULL	0	Static	12,5	100	100	NoSist	1,95	124Xe 26+	420	60	135.40	18.5	7.78E+03	1286	1.00E+07	-	21.664	54.244	No	270	2.70E-05	-	-	0	<1.00E-07	0	<1.00E-07
23*	1	125	SEL	FULL	0	Static	12,5	100	100	NoSist	1,95	124Xe 26+	420	60	135.40	18.5	7.86E+03	1911	1.50E+07	-	32.496	86.740	No	-	-	-	-	0	<6.67E-08	0	<6.67E-08
24	1	125	SEL	FULL	0	Static	12,5	100	100	NoSist	1,95	124Xe 26+	420	60	135.40	18.5	7.75E+03	1080	8.37E+06	-	18.125	104.866	No	244	2.92E-05	-	-	0	<1.20E-07	0	<1.20E-07
25	1	25	SET/SEU	FULL	2	Static	50	100	100	NoSist	1,65	124Xe 26+	420	0	67.70	37.0	2.02E+03	365	7.39E+05	6.94E+05	0.800	105.666	Yes	111	1.60E-04	0	<1.35E-06	-	-	-	-
26	1	25	SET/SEU	FULL	2	Dyn	20	40	40	Dyn 4c	1,65	124Xe 26+	420	0	67.70	37.0	5.32E+02	1178	6.27E+05	-	0.679	106.345	Yes	83	1.32E-04	0	<1.59E-06	-	-	-	-
27	1	25	SET/SEU	FULL	2	Dyn	20	40	40	Dyn 4c	1,65	124Xe 26+	420	0	67.70	37.0	9.92E+02	432	4.29E+05	-	0.464	106.810	No	58	1.35E-04	0	<2.33E-06	-	-	-	-

Table 8: GR718A test results, High LET M/Q=5

▨: This run should not be taken into account
*: During this run, the temperature was increased gradually from 95°C to 125°C, once the temperature stabilized at 125°C the run was stopped. Run 24 was started directly at 125°C.

GR718A CLK= 0MHz to 50MHz ; SPWCLK= 16MHz to 100MHz VDDI/O=+3.3V and VDDCore=+1.65V to +1.95V																					SEU			SET	
Run	Type	Baud Rate	PLL	Mode	CLK (MHz)	SPWCLK (MHz)	Data Rate ports 1-15 (Mbps)	Data Rate port 18 (Mbps)	Script	Vcore	Ion	Energy (MeV)	Tilt (°)	Eff. LET (MeV.cm²/mg)	Eff. Range (µm Si)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Estimated Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	Lost UART Com	Post analysis Data	Cross Section (cm²/device)	Lock	Cross Section (cm²/device)
High Range M/Q=3.3																									
28	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,65	83 Kr 25+	756	0	32.60	92.0	5.06E+03	397	2.00E+06	-	1.043	38.955	No	102	5.10E-05	1	5.00E-07
29	SET/SEU	FULL	2	Static	12,5	100	25	25	NoSist	1,65	83 Kr 25+	756	0	32.60	92.0	5.10E+03	393	2.00E+06	-	1.043	39.998	No	32	1.60E-05	125	6.25E-05
30	SET/SEU	FULL	2	Static	20	100	40	40	NoSist	1,65	83 Kr 25+	756	0	32.60	92.0	5.21E+03	193	1.00E+06	-	0.522	40.520	No	33	3.30E-05	24	2.40E-05
31	SET/SEU	FULL	2	Static	20	100	40	40	NoSist	1,65	83 Kr 25+	756	0	32.60	92.0	5.07E+03	396	2.00E+06	7.71E+05	1.043	41.563	No	16	2.08E-05	34	1.70E-05
32	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,65	83 Kr 25+	756	0	32.60	92.0	5.01E+03	400	2.00E+06	-	1.043	42.606	No	98	4.90E-05	0	<5.00E-07
33	SET/SEU	FULL	2	Static	12,5	100	25	25	NoSist	1,65	83 Kr 25+	756	0	32.60	92.0	4.68E+03	199	9.31E+05	-	0.485	43.092	Yes	-	-	64	6.88E-05
34	SET/SEU	FULL	2	Static	0	100	0	0	WithSist	1,65	83 Kr 25+	756	0	32.60	92.0	4.98E+03	403	2.00E+06	-	1.043	44.135	No	0	<5.00E-07	0	<5.00E-07
35	SET/SEU	FULL	2	Static	0	100	0	0	WithSist	1,4	83 Kr 25+	756	0	32.60	92.0	1.01E+04	199	2.00E+06	-	1.043	45.178	No	0	<5.00E-07	0	<5.00E-07
36	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,95	83 Kr 25+	756	0	32.60	92.0	9.99E+03	202	2.00E+06	1.73E+06	1.043	46.221	Yes	58	3.36E-05	0	<5.00E-07
37	SET/SEU	Derated 18	2	Dyn	20	100	40	20	Dyn 4d	1,8	83 Kr 25+	756	0	32.60	92.0	1.90E+03	781	1.48E+06	-	0.774	46.996	No	69	4.65E-05	13	8.76E-06
38	SET/SEU	Derated 18	8	Dyn	25	100	200	100	Dyn 4d	1,8	83 Kr 25+	756	0	32.60	92.0	2.10E+03	378	7.94E+05	-	0.414	47.410	No	71	8.94E-05	0	<1.26E-06
39	SET/SEU	Derated 18	4	Dyn	50	100	200	100	Dyn 4d	1,8	83 Kr 25+	756	0	32.60	92.0	1.97E+03	297	5.85E+05	-	0.305	47.715	No	80	1.37E-04	0	<1.71E-06
40	SET/SEU	FULL	4	Dyn	50	100	200	200	Dyn 4d	1,8	83 Kr 25+	756	0	32.60	92.0	1.03E+03	52	5.36E+04	-	0.028	47.743	Yes	-	-	0	<1.87E-05
41	SET/SEU	FULL	4	Dyn	50	100	200	200	Dyn 4d	1,8	83 Kr 25+	756	0	32.60	92.0	1.01E+03	457	4.60E+05	-	0.240	47.983	No	72	1.56E-04	0	<2.17E-06
42	SET/SEU	FULL	4	Dyn	50	100	200	200	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	1.87E+03	845	1.58E+06	-	0.515	48.498	No	71	4.50E-05	0	<6.34E-07
43	SET/SEU	Derated	4	Dyn	50	100	100	100	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	3.07E+03	549	1.69E+06	-	0.550	49.048	No	69	4.09E-05	0	<5.93E-07
44	SET/SEU	Derated 18	4	Dyn	50	100	200	100	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	3.03E+03	348	1.06E+06	-	0.344	49.392	No	82	7.77E-05	0	<9.48E-07
45	SET/SEU	Derated 18	2	Dyn	25	100	50	25	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	3.79E+03	389	1.47E+06	-	0.481	49.873	No	28	1.90E-05	0	<6.79E-07
46	SET/SEU	Derated 18	8	Dyn	25	100	200	100	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	2.95E+03	532	1.57E+06	-	0.513	50.386	No	75	4.77E-05	0	<6.36E-07
47	SET/SEU	Derated 18	2	Dyn	20	100	40	20	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	3.22E+03	622	2.00E+06	-	0.653	51.039	No	46	2.30E-05	0	<5.00E-07
48[1]	SET/SEU	Derated 18	4	Dyn	50	100	200	100	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	3.19E+03	537	1.71E+06	-	0.559	51.598	No	70	4.09E-05	1	5.84E-07
49	SET/SEU	Derated 18	2	Dyn	50	100	100	50	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	3.06E+03	432	1.32E+06	1.29E+06	0.431	52.029	No	75	5.84E-05	0	<7.57E-07
50	SET/SEU	Derated 18	8	Dyn	12.5	100	100	50	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	3.98E+03	504	2.00E+06	-	0.653	52.682	No	55	2.75E-05	1	5.00E-07
51	SET/SEU	Derated 18	0	Dyn	12.5	100	100	50	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	3.07E+03	653	2.00E+06	-	0.653	53.335	No	43	2.15E-05	0	<5.00E-07
52[2]	SET/SEU	Derated 18	8	Dyn	12.5	100	100	50	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	3.08E+03	651	2.00E+06	-	0.653	53.988	No	39	1.95E-05	0	<5.00E-07
53	SET/SEU	FULL	2	Static	12,5	100	25	25	NoSist	1,65	58 Ni 18+	567	0	20.40	100.0	1.01E+04	495	5.01E+06	-	1.636	55.624	No	40	7.98E-06	0	<1.99E-07
54	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,65	58 Ni 18+	567	0	20.40	100.0	1.03E+04	488	5.00E+06	-	1.632	57.256	No	125	2.50E-05	0	<2.00E-07
55	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,95	58 Ni 18+	567	0	20.40	100.0	1.50E+04	114	1.71E+06	-	0.558	57.814	Yes	-	-	0	<5.85E-07
56	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,95	58 Ni 18+	567	0	20.40	100.0	9.98E+03	227	2.27E+06	2.11E+06	0.739	58.554	Yes	29	1.38E-05	0	<4.41E-07
57[3]	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,95	58 Ni 18+	567	0	20.40	100.0	1.01E+04	101	1.00E+06	-	0.326	58.880	No	-	-	0	<1.00E-06
58	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,95	58 Ni 18+	567	0	20.40	100.0	1.00E+04	101	1.00E+06	-	0.326	59.206	No	16	1.60E-05	0	<1.00E-06
59	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,65	40 Ar 12+	372	0	10.20	117.0	1.03E+04	488	5.00E+06	-	0.816	60.022	No	5	1.00E-06	0	<2.00E-07
60	SET/SEU	FULL	2	Static	12,5	100	25	25	NoSist	1,65	40 Ar 12+	372	0	10.20	117.0	1.57E+04	320	5.00E+06	-	0.816	60.838	No	2	4.00E-07	0	<2.00E-07
61	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,95	40 Ar 12+	372	0	10.20	117.0	1.60E+04	314	5.00E+06	-	0.816	61.654	No	2	4.00E-07	0	<2.00E-07
62	SET/SEU	FULL	4	Dyn	50	100	200	200	Dyn 4d	1,8	40 Ar 12+	372	0	10.20	117.0	1.01E+04	499	5.00E+06	-	0.816	62.470	No	10	2.00E-06	0	<2.00E-07
63	SET/SEU	Derated 18	4	Dyn	50	100	200	100	Dyn 4d	1,8	40 Ar 12+	372	0	10.20	117.0	1.04E+04	483	5.00E+06	-	0.816	63.286	No	11	2.20E-06	0	<2.00E-07
64	SET/SEU	Derated 18	4	Dyn	50	100	200	100	Dyn 4d	1,8	22 Ne 7+	235	0	3.00	216.0	1.60E+04	627	1.00E+07	-	0.480	63.766	No	0	<1.00E-07	0	<1.00E-07
65	SET/SEU	Derated 18	4	Dyn	50	100	200	100	Dyn 4d	1,8	22 Ne 7+	235	60	6.00	108.0	7.94E+03	1261	1.00E+07	-	0.960	64.726	No	0	<1.00E-07	0	<1.00E-07
66	SET/SEU	FULL	4	Dyn	50	100	200	200	Dyn 4d	1,8	22 Ne 7+	235	60	6.00	108.0	7.95E+03	1259	1.00E+07	-	0.960	65.686	No	0	<1.00E-07	0	<1.00E-07
67	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,65	22 Ne 7+	235	60	6.00	108.0	8.07E+03	1240	1.00E+07	-	0.960	66.646	No	0	<1.00E-07	0	<1.00E-07
68	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,65	83 Kr 25+	756	0	32.60	92.0	5.13E+03	739	3.79E+06	3.60E+06	1.979	68.626	Yes	172	4.77E-05	0	<2.64E-07
69	SET/SEU	FULL	2	Static	50	100	100	100	WithSist	1,65	83 Kr 25+	756	0	32.60	92.0	5.10E+03	981	5.00E+06	-	2.608	71.234	No	257	5.14E-05	1	2.00E-07
70	SET	FULL	2	Static	0	16	32	32	WithSist	1,65	83 Kr 25+	756	0	32.60	92.0	5.23E+03	121	6.33E+05	-	0.330	71.564	No	0	<1.58E-06	30	4.74E-05
71	SET	FULL	2	Static	0	16	32	32	WithSist	1,8	83 Kr 25+	756	0	32.60	92.0	5.06E+03	79	4.00E+05	-	0.209	71.773	No	0	<2.50E-06	32	8.00E-05
72	SET	FULL	2	Static	0	16	32	32	WithSist	1,95	83 Kr 25+	756	0	32.60	92.0	4.96E+03	104	5.16E+05	-	0.269	72.042	No	0	<1.94E-06	31	6.01E-05
73	SET	FULL	2	Static	10	20	40	40	WithSist	1,65	83 Kr 25+	756	0	32.60	92.0	5.09E+03	239	1.22E+06	-	0.635	72.676	No	17	1.40E-05	31	2.55E-05
74	SET	FULL	2	Static	10	30	60	60	WithSist	1,65	83 Kr 25+	756	0	32.60	92.0	9.08E+03	553	5.00E+06	-	2.608	75.284	No	67	1.34E-05	0	<2.00E-07
75[4]	SET	FULL	2	Static	10	25	50	50	WithSist	1,65	83 Kr 25+	756	0	32.60	92.0	9.90E+03	507	5.00E+06	-	2.608	77.892	No	124	2.48E-05	3	6.00E-07

Table 9: GR718A test results, High Range M/Q=3.3, Part No. 3

[1]: The internal loopback option was enabled

[2]: Only port#1 and port#18 were used, to verify the functionality of the SIST test engine by minimizing the number of ports tested (Request of Mr Sturesson from Cobham Gaisler).

[3]: Problem during the stop run process, thus no data have been saved

[4]: The changes in registers were observed after the stop of beam.

GR718A CLK= 12.5MHz to 50MHz ; SPWCLK= 15MHz to 100MHz VDDI/O=+3.3V and VDDCore=+1.65V to +1.95V																					SEU			SET	
Run	Type	Baud Rate	PLL	Mode	CLK (MHz)	SPWCLK (MHz)	Data Rate ports 1-15 (Mbps)	Data Rate port 18 (Mbps)	Script	Vcore	Ion	Energy (MeV)	Tilt (°)	Eff. LET (MeV.cm²/mg)	Eff. Range (µm Si)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Estimated Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	Lost UART Com	Post analysis Data	Cross Section (cm²/device)	Lock	Cross Section (cm²/device)
High Range M/Q=3.3																									
76	SET/SEU	Derated 18	4	Dyn	50	100	200	100	Dyn 4d	1,8	22 Ne 7+	235	60	6.00	108.0	8.12E+03	1233	1.00E+07	-	0.960	107.770	No	0	<1.00E-07	0	<1.00E-07
77	SET/SEU	FULL	4	Dyn	50	100	200	200	Dyn 4d	1,8	22 Ne 7+	235	60	6.00	108.0	7.66E+03	1308	1.00E+07	-	0.960	108.730	No	2	2.00E-07	0	<1.00E-07
78	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,65	22 Ne 7+	235	60	6.00	108.0	7.95E+03	1259	1.00E+07	-	0.960	109.690	No	0	<1.00E-07	0	<1.00E-07
79	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,65	40 Ar 12+	372	0	10.20	117.0	1.50E+04	336	5.00E+06	-	0.816	110.506	No	8	1.60E-06	0	<2.00E-07
80	SET/SEU	FULL	2	Static	12,5	100	50	50	NoSist	1,65	40 Ar 12+	372	0	10.20	117.0	1.54E+04	327	5.00E+06	-	0.816	111.322	No	1	2.00E-07	0	<2.00E-07
81	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,95	40 Ar 12+	372	0	10.20	117.0	1.62E+04	310	5.00E+06	-	0.816	112.138	No	1	2.00E-07	0	<2.00E-07
82	SET/SEU	FULL	4	Dyn	50	100	200	200	Dyn 4d	1,8	40 Ar 12+	372	0	10.20	117.0	1.57E+04	640	1.00E+07	-	1.632	113.770	No	20	2.00E-06	0	<1.00E-07
83	SET/SEU	Derated 18	4	Dyn	50	100	200	100	Dyn 4d	1,8	40 Ar 12+	372	0	10.20	117.0	1.51E+04	665	1.00E+07	-	1.632	115.402	No	36	3.60E-06	0	<1.00E-07
84	SET/SEU	Derated 18	2	Dyn	20	100	40	20	Dyn 4d	1,8	40 Ar 12+	372	0	10.20	117.0	1.01E+04	499	5.00E+06	-	0.816	116.218	No	5	1.00E-06	0	<2.00E-07
85	SET/SEU	Derated 18	2	Dyn	20	100	40	20	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	5.06E+03	991	5.00E+06	-	1.632	117.850	No	89	1.78E-05	0	<2.00E-07
86	SET/SEU	FULL	2	Static	12,5	100	25	25	NoSist	1,65	58 Ni 18+	567	0	20.40	100.0	1.07E+04	467	5.00E+06	-	1.632	119.482	No	52	1.04E-05	0	<2.00E-07
87	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,65	58 Ni 18+	567	0	20.40	100.0	1.01E+04	498	5.00E+06	-	1.632	121.114	No	113	2.26E-05	0	<2.00E-07
88	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,95	58 Ni 18+	567	0	20.40	100.0	1.03E+04	487	5.00E+06	-	1.632	122.746	No	69	1.38E-05	0	<2.00E-07
89	SET/SEU	FULL	4	Dyn	50	100	200	200	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	5.20E+03	386	2.00E+06	-	0.653	123.398	No	106	5.30E-05	0	<5.00E-07
90	SET/SEU	Derated 18	4	Dyn	50	100	200	100	Dyn 4d	1,8	58 Ni 18+	567	0	20.40	100.0	5.36E+03	374	2.00E+06	-	0.653	124.051	No	137	6.85E-05	0	<5.00E-07
91	SET/SEU	Derated 18	2	Dyn	20	100	40	20	Dyn 4d	1,8	83 Kr 25+	756	0	32.60	92.0	5.28E+03	949	5.00E+06	-	2.608	126.659	No	189	3.78E-05	44	8.80E-06
92	SET/SEU	FULL	2	Static	20	100	40	40	NoSist	1,65	83 Kr 25+	756	0	32.60	92.0	1.04E+04	484	5.00E+06	-	2.608	129.267	No	114	2.28E-05	84	1.68E-05
93	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,65	83 Kr 25+	756	0	32.60	92.0	5.80E+03	403	2.34E+06	1.93E+06	1.218	130.485	Yes	90	4.66E-05	0	<4.28E-07
94	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,65	83 Kr 25+	756	0	32.60	92.0	5.23E+03	384	2.00E+06	-	1.043	131.529	No	109	5.45E-05	1	5.00E-07
95	SET/SEU	FULL	2	Static	12,5	100	25	25	NoSist	1,65	83 Kr 25+	756	0	32.60	92.0	9.77E+03	206	2.00E+06	-	1.043	132.572	No	31	1.55E-05	121	6.05E-05
96	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,95	83 Kr 25+	756	0	32.60	92.0	9.68E+03	75	7.26E+05	-	0.378	132.950	Yes	-	-	0	<1.38E-06
97	SET/SEU	FULL	2	Static	50	100	100	100	NoSist	1,95	83 Kr 25+	756	0	32.60	92.0	1.02E+04	197	2.00E+06	-	1.043	133.993	No	66	3.30E-05	0	<5.00E-07
98	SET/SEU	Derated 18	4	Dyn	50	100	200	100	Dyn 4d	1,8	83 Kr 25+	756	0	32.60	92.0	1.97E+03	249	4.90E+05	-	0.256	134.249	No	81	1.65E-04	0	<2.04E-06
99	SET/SEU	FULL	4	Dyn	50	100	200	200	Dyn 4d	1,8	83 Kr 25+	756	0	32.60	92.0	9.56E+02	616	5.89E+05	-	0.307	134.556	No	65	1.10E-04	0	<1.70E-06
100	SET/SEU	Derated 18	4	Dyn	50	100	200	100	Dyn 4d	1,8	22 Ne 7+	235	0	3.00	216.0	1.57E+04	147	2.30E+06	-	0.110	134.667	No	0	<4.34E-07	0	<4.34E-07
101	SET/SEU	Derated 18	4	Dyn	50	100	200	100	Dyn 4d	1,8	22 Ne 7+	235	60	6.00	108.0	7.87E+03	1270	1.00E+07	-	0.960	135.627	No	0	<1.00E-07	0	<1.00E-07
102	SET	FULL	2	Static	50	15	30	30	WithSist	1,65	83 Kr 25+	756	0	32.60	92.0	1.00E+04	451	4.52E+06	3.41E+06	2.360	137.987	Yes	165	4.84E-05	205	4.53E-05
103	SET	FULL	2	Static	50	20	40	40	WithSist	1,65	83 Kr 25+	756	0	32.60	92.0	1.02E+04	310	3.17E+06	-	1.654	139.641	Yes	-	-	31	9.77E-06
104	SET	FULL	2	Static	50	25	50	50	WithSist	1,65	83 Kr 25+	756	0	32.60	92.0	1.03E+04	487	5.00E+06	5.87E+05	2.608	142.249	Yes	28	4.77E-05	0	<2.00E-07
105	SET	Derated 18	8	Dyn	50	25	200	100	Dyn 4d	1,8	83 Kr 25+	756	0	32.60	92.0	4.98E+03	201	1.00E+06	-	0.522	142.771	No	118	1.18E-04	1	1.00E-06
106	SET	FULL	2	Static	50	15	30	30	WithSist	1,65	58 Ni 18+	567	0	20.40	100.0	1.58E+04	3165	5.00E+07	4.76E+06	16.320	159.091	Yes	101	2.12E-05	2	4.00E-08
107	SET	FULL	2	Static	50	20	40	40	WithSist	1,65	58 Ni 18+	567	0	20.40	100.0	1.57E+04	2000	3.14E+07	7.35E+06	10.257	169.348	Yes	151	2.05E-05	0	<3.18E-08

Table 10: GR718A test results, High Range M/Q=3.3, Part No. 1

The test results are described hereunder.

7.2. SEL test results.

The SEL test was performed at 80°C, 85°C and 125°C on one part.

Two heating resistors were used to heat the DUT at 125°C. But during run No. 18 one of the two heating resistors broke. With one heating resistor the temperature of part No. 3 couldn't go above 80°C. The first time, two runs were performed at 85°C on part No. 1, in order to be close to the condition of part No. 3. The second time, the temperature was increased up to 125°C during run 23. When the temperature was stabilized at 125°C, run 23 was stopped and a new run was performed.

No SEL was observed during this test under Xenon irradiation with a total fluence equal to 1E+7 cm^{-2}:
- with a particle angle of 60° (LET = 135.4 MeV.cm²/mg and range = 18.5µm).
- with a particle angle of 0° (LET = 67.7 MeV.cm²/mg and range = 37µm).

During run No. 1 the two heating resistors broke and the run had to be stopped. After replacing the heating resistors, part No. 1 was tested at 125°C under Xenon irradiation with an incident angle of 60° and a total fluence equal to 8.37E+6 cm^{-2}. No SEL was observed during the run.
A total fluence of 1E+7 was not reached, because one of the two heating resistors broke and the temperature of 125°C could no longer be maintained.

Run No.	Part No.	V_{DD}Core (V)	V_{DD}IO	Temperature (°C)	Effective LET (MeV.cm²/mg)	Effective Range (µm Si)	Run Fluence (cm-2)
1	1	1.95	3.6	125	67.7	37	1.83E+06
18	3	1.95	3.6	80	67.7	37	1.00E+07
19	3	1.95	3.6	80	135.4	18.5	1.00E+07
21	1	1.95	3.6	85	67.7	37	1.00E+07
22	1	1.95	3.6	85	135.4	18.5	1.00E+07
23	1	1.95	3.6	95→125	135.4	18.5	1.50E+07*
24	1	1.95	3.6	125	135.4	18.5	8.37E+06*

Table 11: SEL conditions

*The accumulated fluence of these two test runs with temperature at 125C was >1E+7 ions/cm².
Thus test plan was completed for one device at maximum LET.

7.3. SET test results

SETs, being PLL un-lock events recorded on the LOCK output signal, were observed during the irradiation down to the Nickel Heavy Ion (LET = 20.4 MeV.cm²/mg and range = 100µm).

Table 12 describes the baseline configurations used during the experiment.

Configurations	Vcore (V)	Vio (V)	Baud rate*	Mode	CLK (MHz)	SPWCLK (MHz)	PLL
1	1.8	3.3	Port No. 18 Derated	Dynamic	50	100	CLKx4
2	1.8	3.3	Full	Dynamic	50	100	CLKx4
3	1.95	3.3	Full	Static	50	100	CLKx2
4	1.65	3.3	Full	Static	50	100	CLKx2
5	1.65	3.3	Full	Static	12.5	100	CLKx2
6	1.8	3.3	Port No. 18 Derated	Dynamic	20	100	CLKx2

Table 12: Baseline PLL conditions

*Baud rate has no effect on results for SET (PLL).

During the experiment, additional configurations were performed in order to investigate on the LOCK signal results with respect to bias, input frequency CLK and SPWCLK, data transfer rate and PLL configuration. The additional configurations are described in Table 13.
The PLL's ability maintaining its lock condition showed sensitivity to heavy ions up to Krypton Heavy Ion (LET = 32.6 MeV.cm²/mg and range = 92µm).

Configurations	Vcore (V)	Vio (V)	Baud rate*	Mode	CLK (MHz)	SPWCLK (MHz)	PLL
7	1,65	3.3	Full	Static	0	16	SPWCLKx2
8	1,8	3.3	Full	Static	0	16	SPWCLKx2
9	1,95	3.3	Full	Static	0	16	SPWCLKx2
10	1,65	3.3	Full	Static	10	20	SPWCLKx2
11	1,65	3.3	Full	Static	10	30	SPWCLKx2
12	1,65	3.3	Full	Static	10	25	SPWCLKx2
13	1,65	3.3	Full	Static	50	15	SPWCLKx2
14	1,65	3.3	Full	Static	50	20	SPWCLKx2
15	1,65	3.3	Full	Static	50	25	SPWCLKx2

Table 13: Additional PLL conditions

*: Baud rate has no effect on results for SET (PLL).

7.3.1. SET Cross sections

LET Eff (MeV.cm².mg^{-1})	SET Cross Section (cm²/device)											
	Configuration 1		Configuration 2		Configuration 3		Configuration 4		Configuration 5		Configuration 6	
	Part No. 1	Part No. 3	Part No. 1	Part No. 3	Part No. 1	Part No. 3	Part No. 1	Part No. 3	Part No. 1	Part No. 3	Part No. 1	Part No. 3
67.7	<3.99E-06	-	-	-	-	-	<1.35E-06	-	-	-	<3.33E-07	-
40.4	<3.10E-06	-	<2.24E-06	-	-	-	<8.53E-07	-	-	-	-	-
32.6	<2.04E-06	<1.71E-06	<1.70E-06	<1.87E-05	<5.00E-07	<5.00E-07	5.00E-07	<5.00E-07	6.05E-05	6.25E-05	8.80E-06	8.76E-06
20.4	<5.00E-07	<9.48E-07	<5.00E-07	<6.34E-07	<2.00E-07	<4.41E-07	<2.00E-07	<2.00E-07	<2.00E-07	<1.99E-07	<2.00E-07	<5.00E-07
10.2	<1.00E-07	<2.00E-07	<1.00E-07	<2.00E-07	<2.00E-07	<2.00E-07	<2.00E-07	<2.00E-07	<2.00E-07	<2.00E-07	<2.00E-07	-
6	<1.00E-07	<1.00E-07	<1.00E-07	<1.00E-07	-	-	<1.00E-07	<1.00E-07	-	-	-	-

Table 14: SET cross section results

SET Cross Section (cm²/device)				
LET Eff (MeV.cm².mg^{-1})	32.6		20.4	
Part No.	1	3	1	3
Configuration 7	-	4.74E-05	-	-
Configuration 8	-	8.00E-05	-	-
Configuration 9	-	6.01E-05	-	-
Configuration 10	-	2.55E-05	-	-
Configuration 11	-	<2.00E-07	-	-
Configuration 12	-	6.00E-07	-	-
Configuration 13	4.53E-05	-	4.00E-08	-
Configuration 14	9.77E-06	-	<3.18E-08	-
Configuration 15	<2.00E-07	-	-	-

Table 15: SET cross section results - additional configuration

To conclude on this additional test (with configuration 7 to 15), it was observed that the input clock frequency into the PLL (SPWCLK in this case) is observed to be most critical for LOCK events and when the frequency is lower, there is a higher sensitivity. The clock frequency of the other clock (CLK) did not affect the results nor the PLL multiplication factor. This is observable directly on the cross section give on Table 15. With 20MHz frequency and below, LOCK events were observed with a quite significant cross section. During testing, the frequency was set below the specified range, 20MHz, in order to be able to better measure the cross section area for the node(s) causing these events. This was achieved with configuration 7, 8, 9 and 13.

In configuration 7, 8 and 9 the SEU sensitivity was tested with three different supply levels of Vcore (1.65V, 1.8V and 1.95V). The highest cross section was recorded with Vcore=1.8V (configuration 8), but the difference between the three supply levels were minor. It is not within the scope of this report to investigate this further.

No events were recorded with LET of 67.7 MeV.cm2/mg and 40.4 MeV.cm2/mg using the M/Q=5 ion cocktail. This may indicate that the results can be sensitive to the choice of ion cocktail. To conclude on this further testing would have been needed. This is not within the scope of this report.

7.3.2. Worst Cases SET Observed

The event bellow shows a transient on the lock pin which indicates a potential loss of LOCK of the internal PLL. The width of the pulse was of 1.63µs. That was the maximum width observed on Lock pin. It occurred on Part No. 1 during run No. 94 event No. 1 (Kr, 32.4 MeV.cm²/mg).

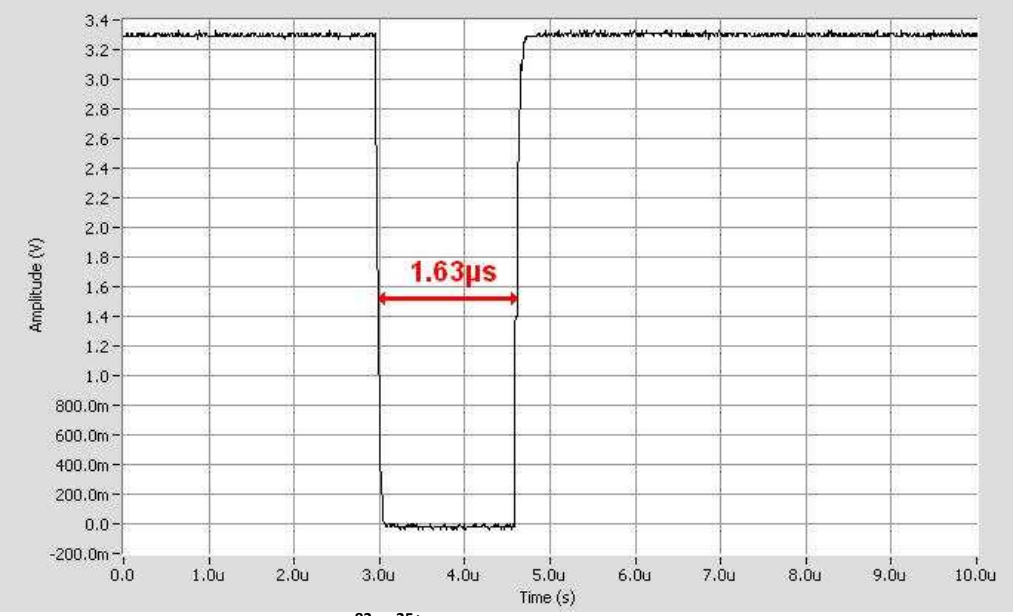


Figure 12: SET curve on Lock pin, Ion $^{83}Kr^{25+}$ (LET of 32.4MeV.mg/cm²), Part 1, Run No. 94, Event No. 1

For the other events, the width of the pulse varied between 410ns and 1.63µs. In all events, the LOCK signal recovered to its high level. Thus no event was recorded where the internal PLL could not recover itself to normal operation.

7.4. SEU test results

The result of the Link Analyser has not been taken into account due to the fact that it triggered every time that the script reseted the part. The script performed a reset of the part under following conditions:

- Port status errors
- PLL unlock
- end of SIST sequence
- unexpected response from SIST at register read and writes

The Link Analyser also triggered when burst errors occurred, the system did not have time to rearm after such errors.
SEU cross-section curves versus LET have been calculated for the configurations of interest described in Table 12.
As SETs were observed on LOCK signal, additional explanations have to be given concerning their impact on the SEU result. A lost of lock signal, in static testing, is not expected to cause any SEU error since the SpaceWire clock domain using the clock from the PLL is in standby mode. Some status registers in the SpaceWire ports may change state, but it is hard to correlate such events to the PLL event.
In dynamic mode, a loss of PLL lock was detected by an internal status register (RTR.GPIA.LL bit, see datasheet), which was polled by the test software continuously during testing. The status register was then cleared by the test SW. In post analysis of dynamic test runs, all errors reported by the SIST have been disregarded where a loss of the PLL lock has been recorded at the same time.

7.4.1. SEU Cross sections in Dynamic Mode

The reported number of errors per test run (SEU) in dynamic tests corresponded to any type of error in a SpaceWire packet reported by the SIST. This may be a bit error in the data, a SpaceWire protocol error or any other type of error. When the SIST reported more than one error on the same SPW packet, it was only counted as one error. Thus the reported data provides an overall error rate for any type of erroneous SpaceWire packet.
Table 16 summarizes the cross section for three configurations of interest. SEUs were observed during the irradiation down to the Neon Heavy Ion with a particular angle of 60° (LET = 6 MeV.cm²/mg and range = 108µm).
These results seem to indicate that input frequency plays a more important role than data transfer rate between ports.

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²/device)					
	Configuration 1		Configuration 2		Configuration 6	
	Part No. 1	Part No. 3	Part No. 1	Part No. 3	Part No. 1	Part No. 3
67.7	3.39E-04	-	-	-	6.80E-05	-
40.4	2.88E-04	-	1.57E-04	-	-	-
32.6	1.65E-04	1.37E-04	1.10E-04	1.56E-04	3.78E-05	4.65E-05
20.4	6.85E-05	7.77E-05	5.30E-05	4.50E-05	1.78E-05	2.30E-05
10.2	3.60E-06	2.20E-06	2.00E-06	2.00E-06	1.00E-06	-
6	<1.00E-07	<1.00E-07	2.00E-07	<1.00E-07	-	-

Table 16: SEU cross section results in Dynamic Mode

The following figures present the plots of the cross section of SEUs versus LET for the indicated configurations.
Points represented by an arrow pointing down indicate that no events were observed at the corresponding LET. The evaluated cross section is then lower than one divided by the effective fluence (value corresponding to one event at the tested fluence).

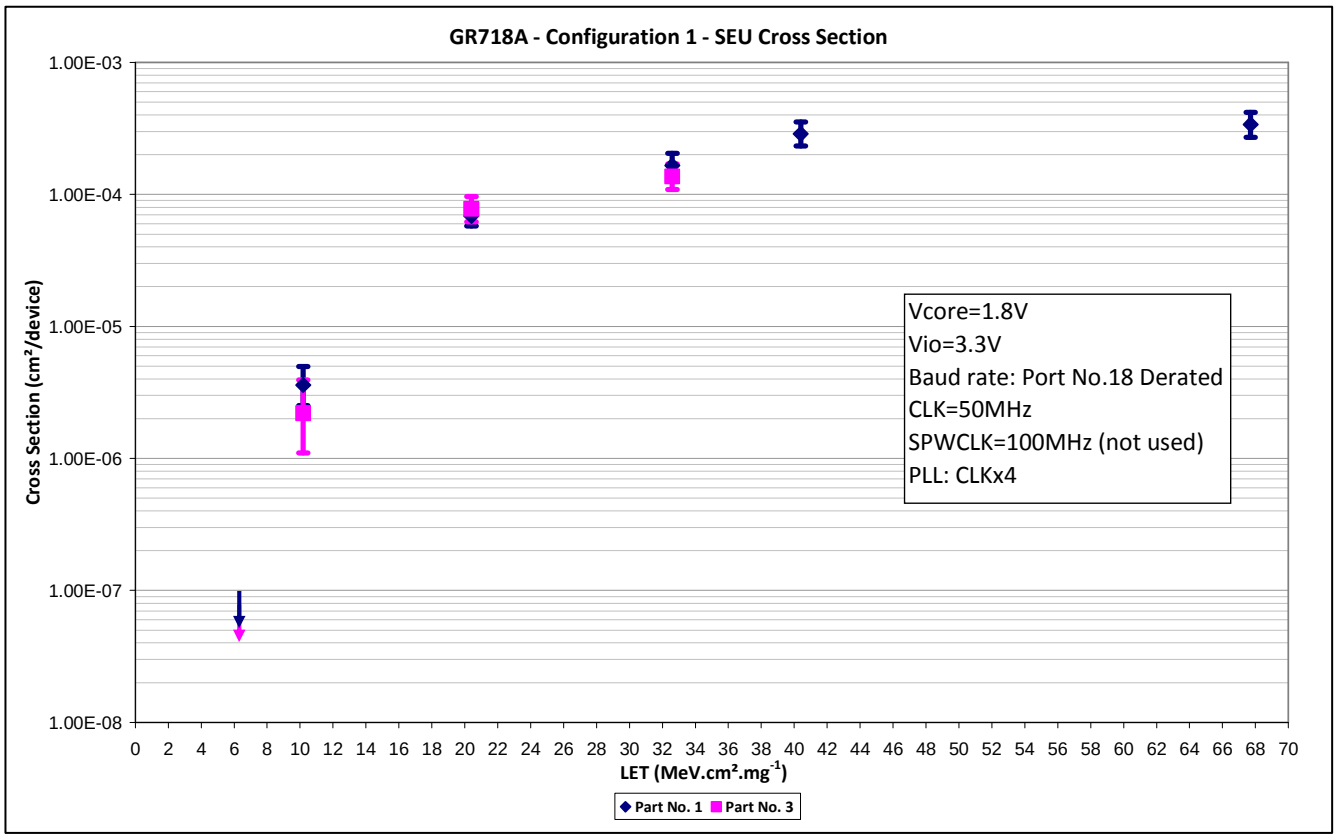


Figure 13: Configuration 1 SEU cross section curve for GR718A

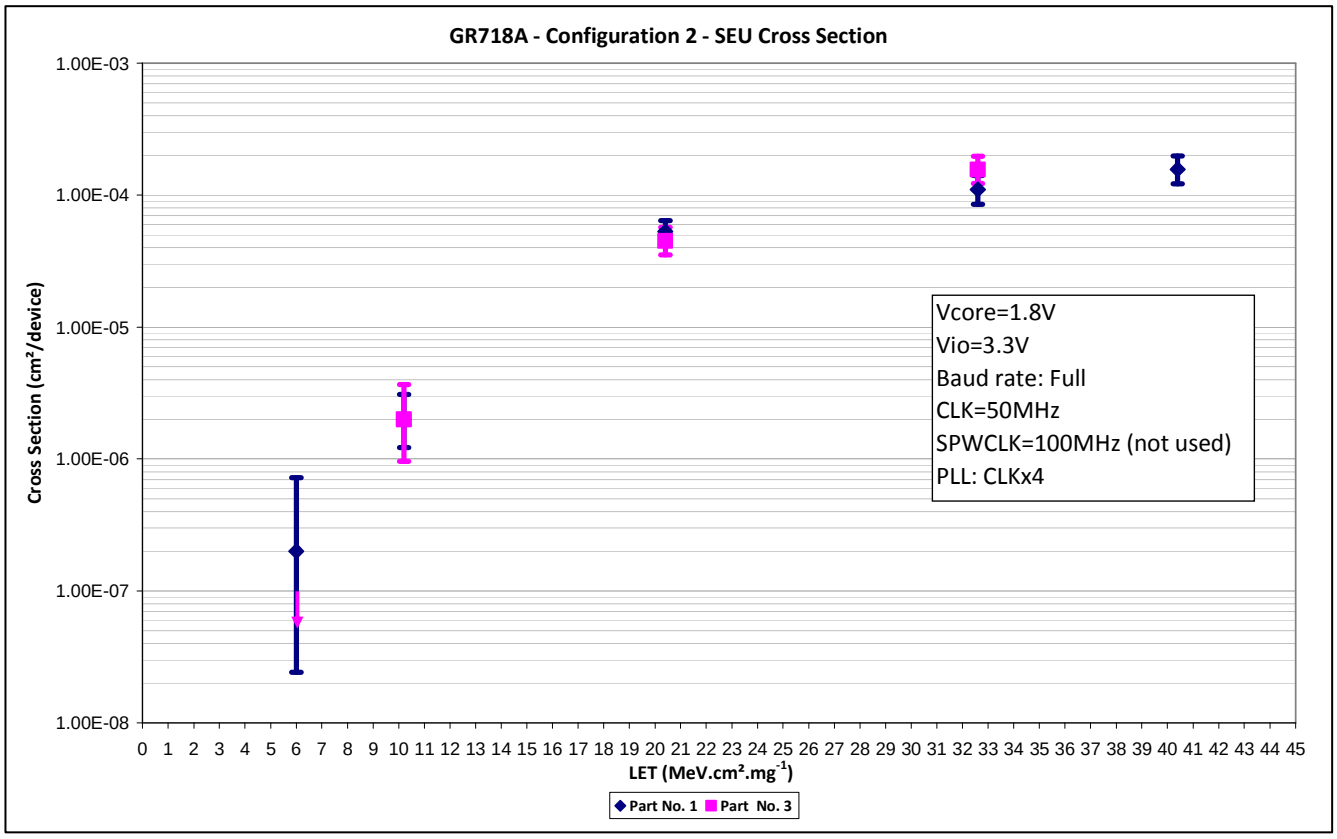


Figure 14: Configuration 2 SEU cross section curve for GR718A

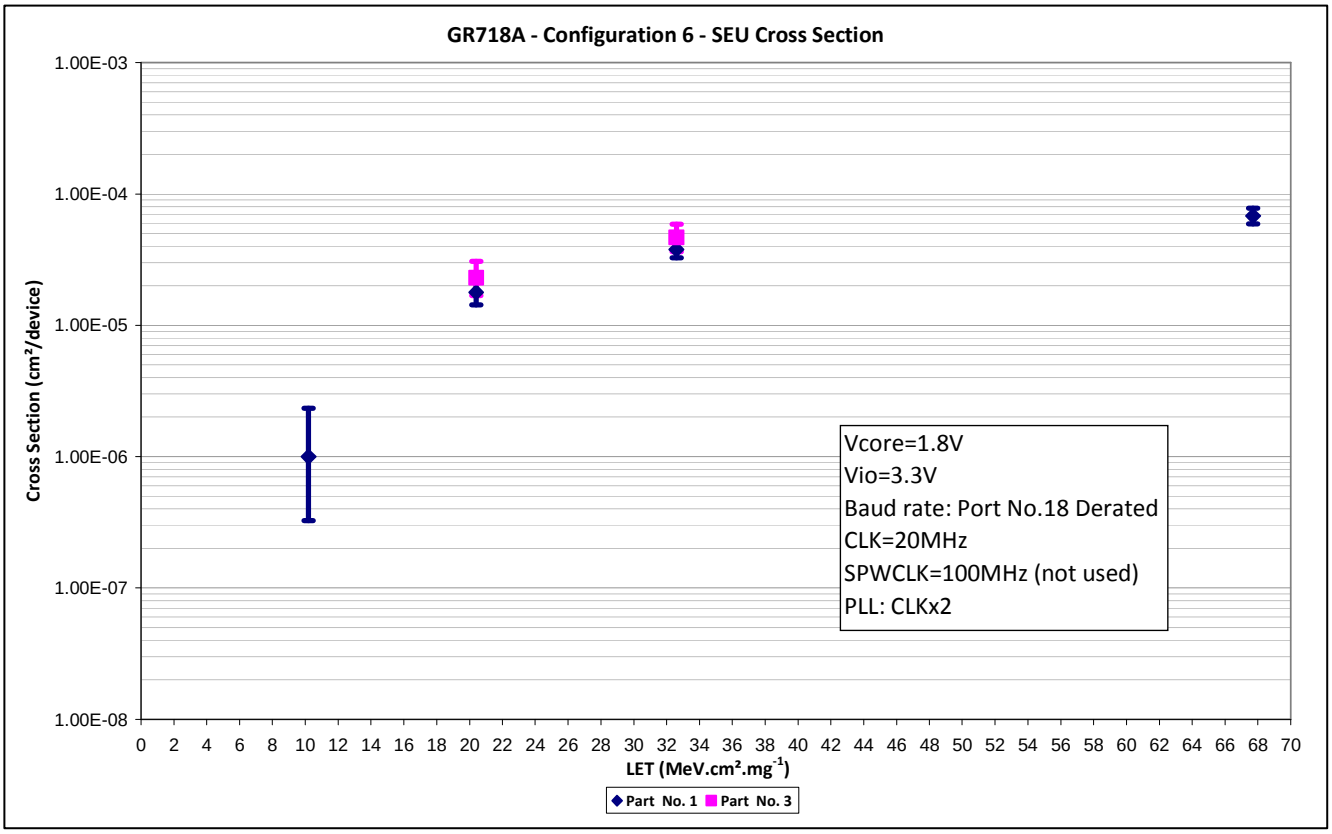


Figure 15: Configuration 6 SEU cross section curve for GR718A

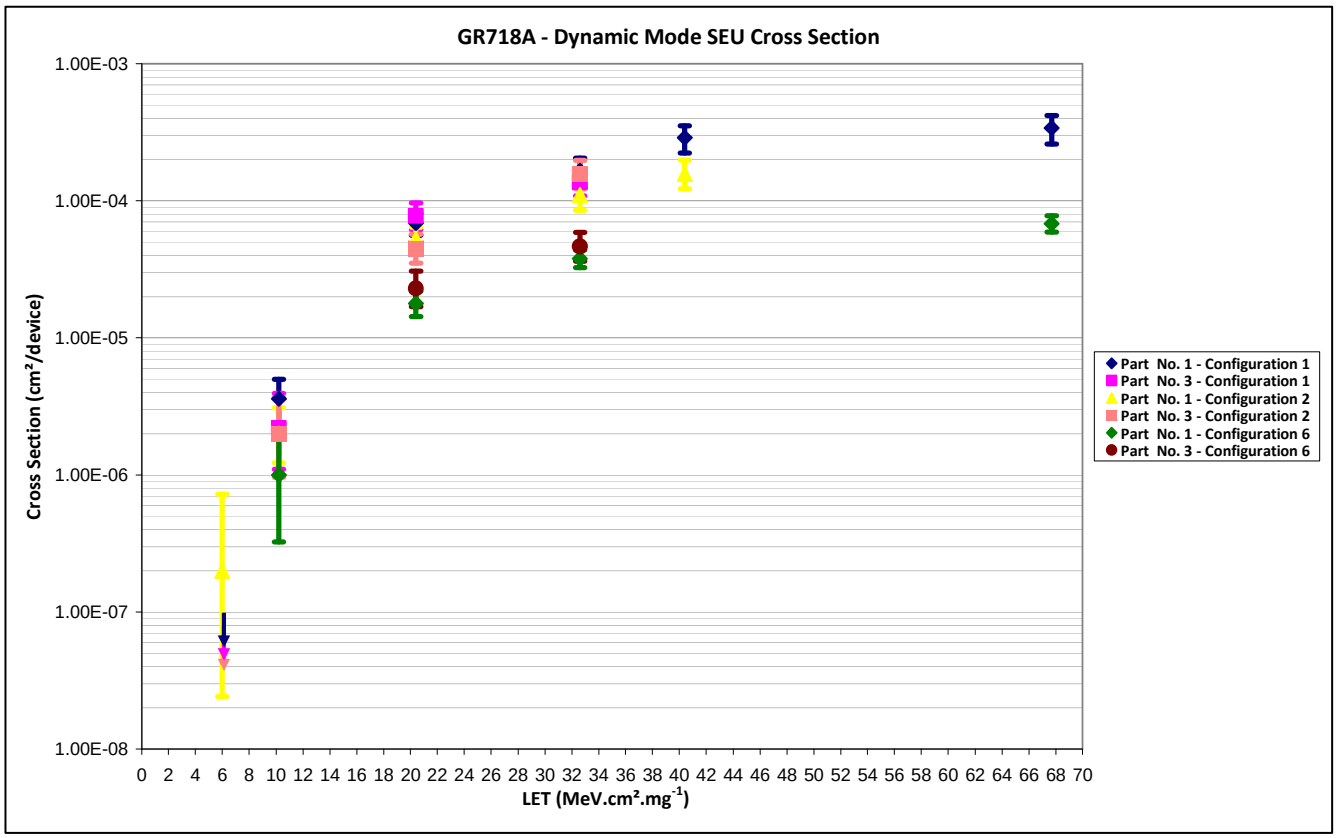


Figure 16: Dynamic Mode SEU cross section curve for GR718A

7.4.2. SEU Cross sections in Static Mode

During the SEE test campaign, some changes in registers were not produced by the interaction of one heavy ion but by changes in associated registers. For example, changes in the router mappings registers were reflected in the combined mapping registers. Therefore, post analysis of the data has been performed to remove error counts due to change in associated registers not linked to SEU events.
Table 17 summarizes the SEU cross section per device for three configurations of interest which showed sensitivity versus heavy ions. The SEU cross section per bit can be estimated from the data in Table 17 assuming 760x32 bits were monitored. However this calculation will not be fully accurate because some upsets may trigger change of state on several status registers. It was not calculated on the report.
SEUs were observed during the irradiation down to the Argon Heavy Ion (LET = 10.2 MeV.cm²/mg and range = 117µm).

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²/device)					
	Configuration 3		Configuration 4		Configuration 5	
	Part No. 1	Part No. 3	Part No. 1	Part No. 3	Part No. 1	Part No. 3
67.7	-	-	1.60E-04	-	-	-
40.4	-	-	8.17E-05	-	-	-
32.6	3.30E-05	3.36E-05	5.06E-05*	4.82E-05*	1.55E-05	1.60E-05
20.4	1.38E-05	1.45E-05*	2.26E-05	2.50E-05	1.04E-05	7.98E-06
10.2	2.00E-07	4.00E-07	1.60E-06	1.00E-06	2.00E-07	4.00E-07
6	-	-	<1.00E-07	<1.00E-07	-	-

*: Two runs were used to calculate the cross-section.

Table 17: SEU cross section results in Static Mode

The following figures present the plots of the cross section of SEUs versus LET for the tested configurations. Points represented by an arrow pointing down indicate that no events were observed at the corresponding LET.
The evaluated cross section is then lower than one divided by the effective fluence (value corresponding to one event at the tested fluence).
These results seem to indicate that the input frequency and the Core voltage influence the SEU sensitivity of the device.

Some few Irradiation tests were also performed in static mode with no system clock running (CLK=0):

- With Krypton Ion (LET =32.6 MeV.cm²/mg) no SEUs were recorded.
- With Xenon Ion (LET =67.7 MeV.cm²/mg) in total 3 SEUs were recorded.

The calculated SEU cross section with Vcore = 1.65V was 1.0E-6 cm²/device. This result was compared with results for configurations 4 (50 MHz) and 5 (12.5MHz). The SEU sensitivity was significantly lower when no system clock was running. The LET threshold was higher and the SEU cross section was lower. Irradiation was also performed in static mode without CLK, two SEUs were observed with a Vcore of 1.65V and one SEU was observed with a Vcore of 1.95V only for Xenon heavy ion on part 1.

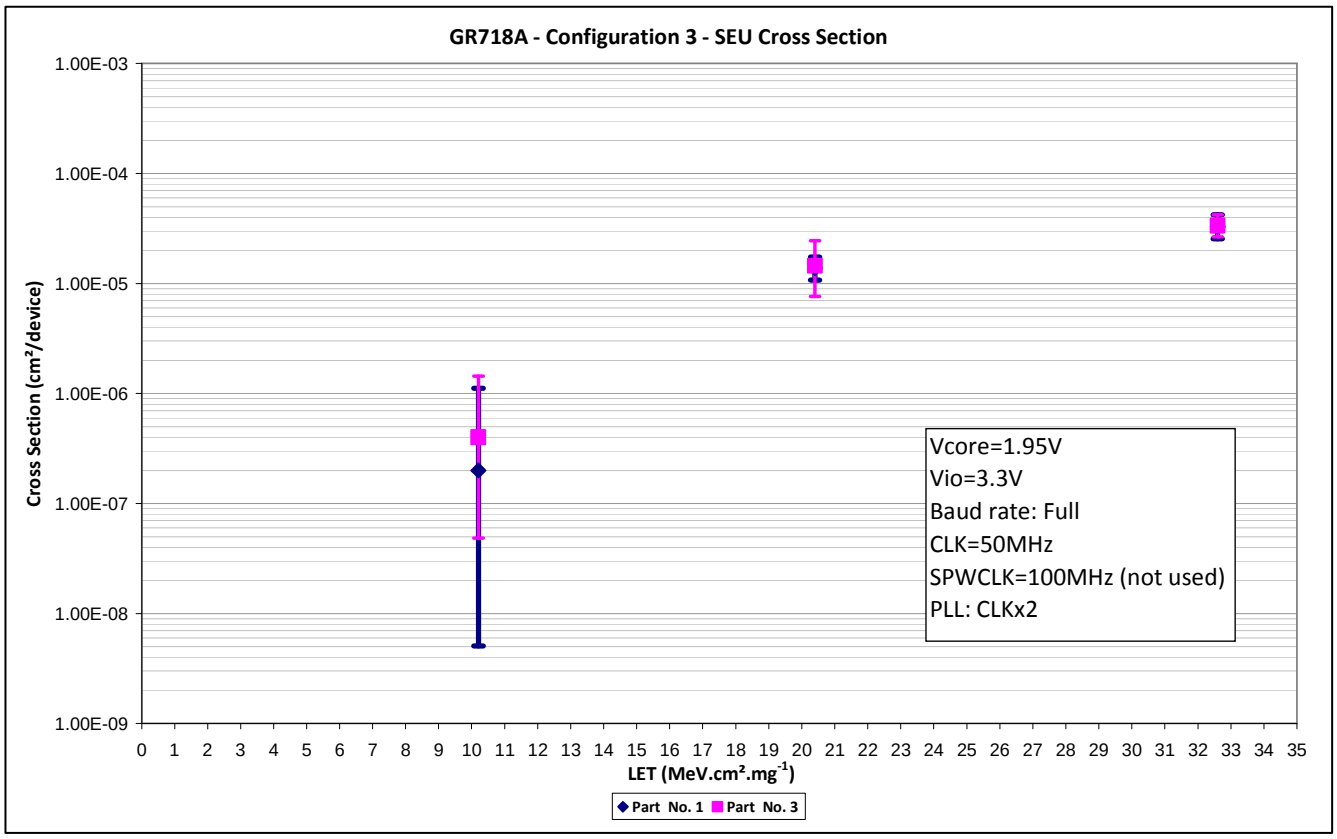


Figure 17: Configuration 3 SEU cross section curve for GR718A

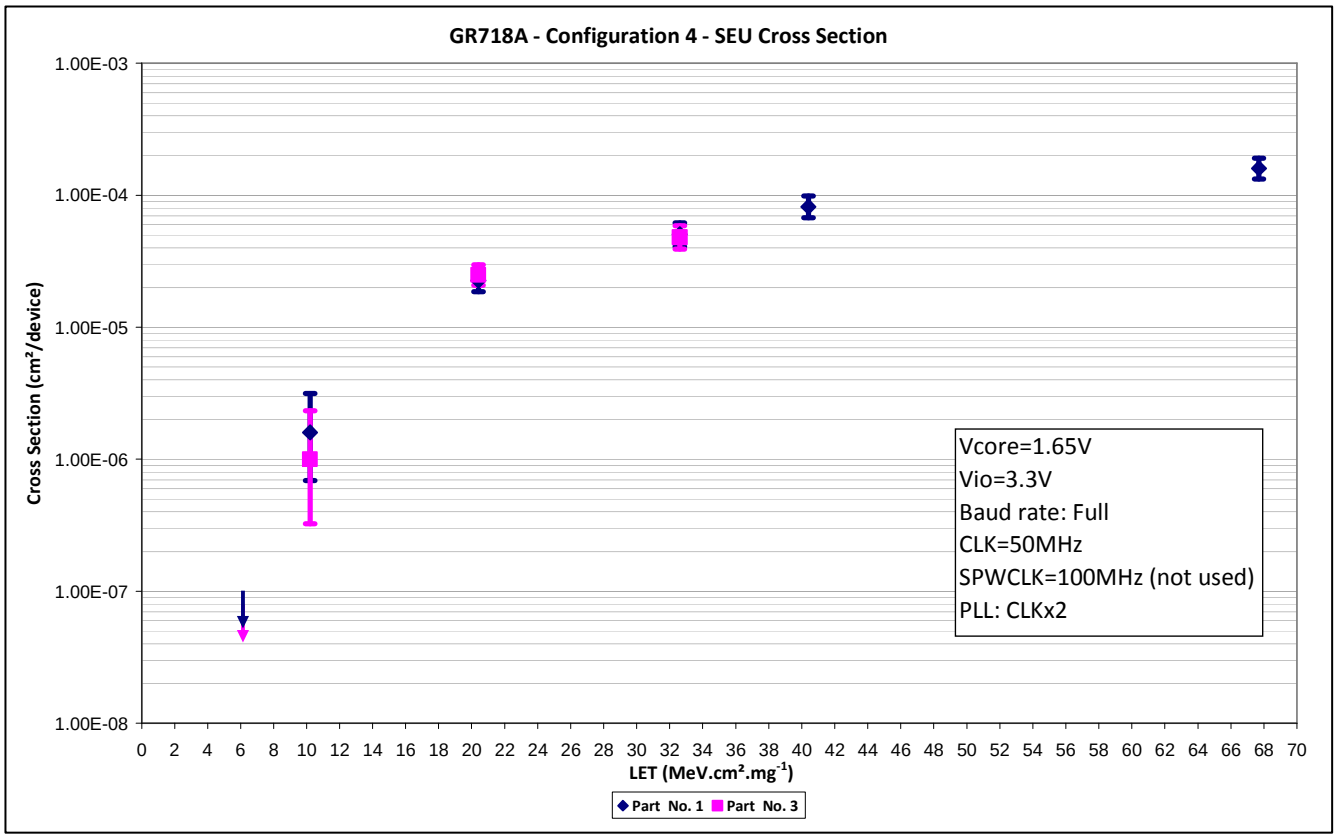


Figure 18: Configuration 4 SEU cross section curve for GR718A

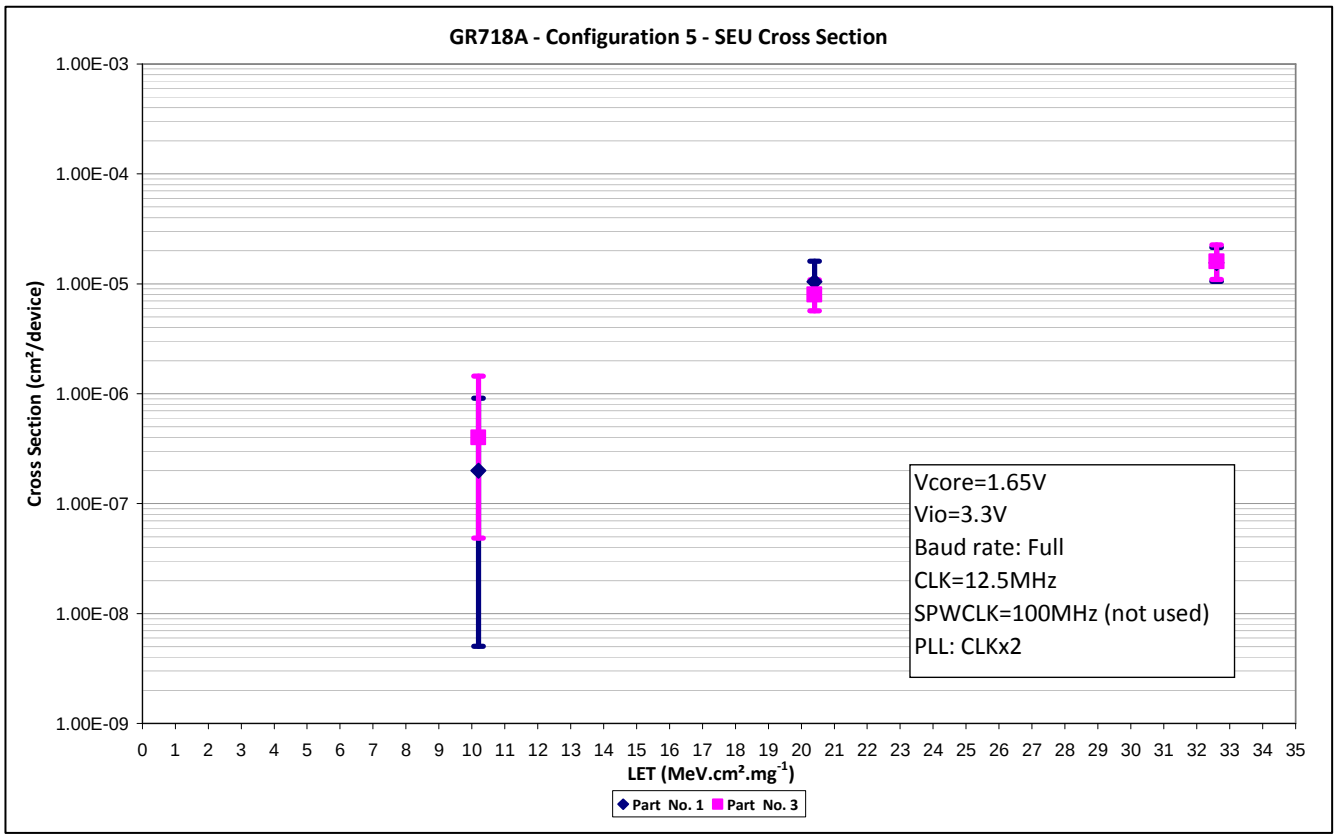


Figure 19: Configuration 5 SEU cross section curve for GR718A

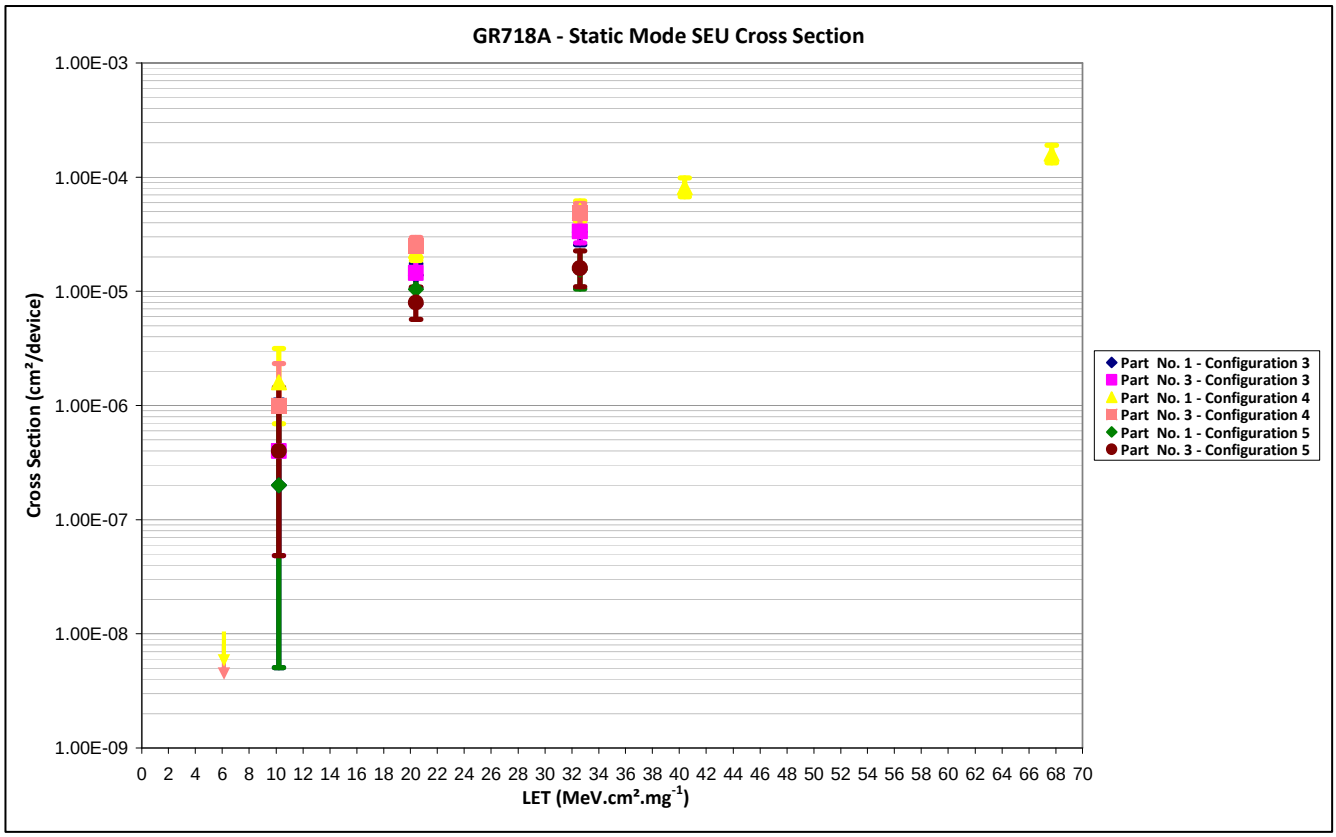


Figure 20: Static Mode SEU cross section curve for GR718A

7.5. UART Link events

During the irradiation, communication interruptions occurred between the GRMON2 software and the DUT. When this lost of communication occurred the software froze, therefore the irradiation had to be stopped before the end of the run.

Loss of communication was observed during the irradiation down to the Nickel Heavy Ion (LET= 20.4 MeV.cm²/mg and range = 100µm). The cross section for UART link events was not calculated but since the majority of test runs (82%) passed without any loss of communication the error cross section for UART link events must be lower than all other type of SEU and SET events reported.

7.6. Weibull fit

7.6.1. Weibull fit of SEU Cross sections in Dynamic mode

On this paragraph, a Weibull fit of SEU dynamic cross section configuration 1, 2, 6 and static cross section configuration 3, 4 and 5 is performed using OMERE.

The next table shows the Weibull fit for the SEU dynamic cross section configuration 1:

	Vcomp Xsection
w	28.35
s	2.67
LET threshold	6
Saturation cross section	3.39 E-4

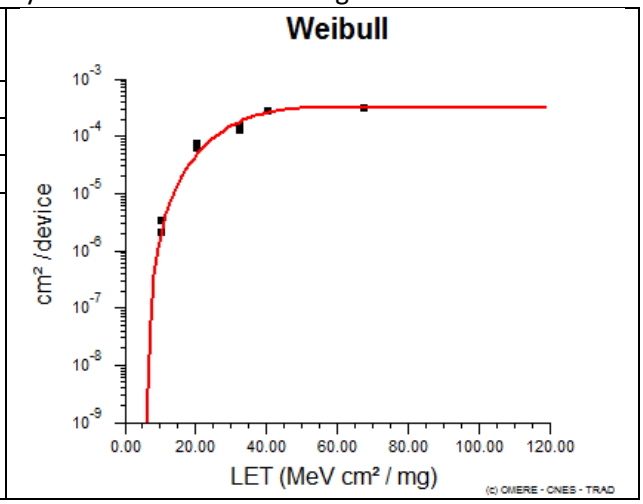


Table 18: SEU dynamic cross section configuration 1

The next table shows the Weibull fit for the SEU dynamic cross section configuration 2:

	Vcomp Xsection
w	21.70
s	3.2
LET threshold	3.88
Saturation cross section	1.57 E-4

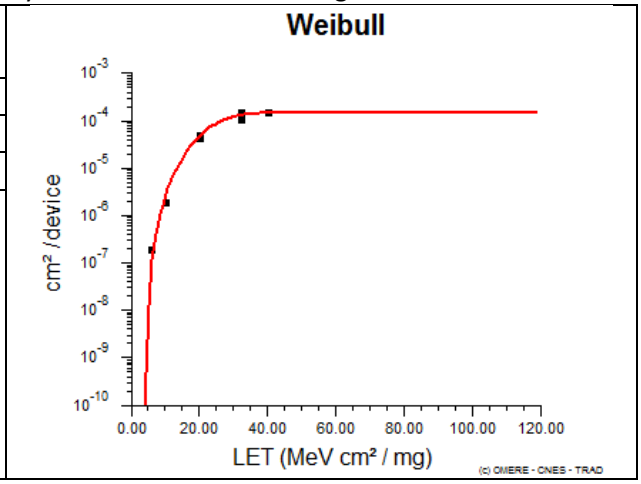


Table 19: SEU dynamic cross section configuration 2

The next table shows the Weibull fit for the SEU dynamic cross section configuration 6:

	Vcomp Xsection
w	22.78
s	1.85
LET threshold	7.94
Saturation cross section	6.8 E-5

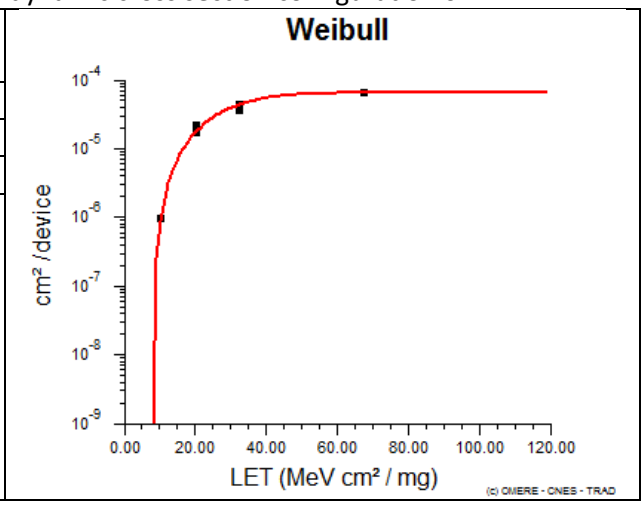


Table 20: SEU dynamic cross section configuration 6

7.6.2. Weibull fit of SEU Cross sections in Static mode

The next table shows the Weibull fit for the SEU static cross section configuration 3:

	Vcomp Xsection
w	18.18
s	3.97
LET threshold	4.78
Saturation cross section	3.36 E-5

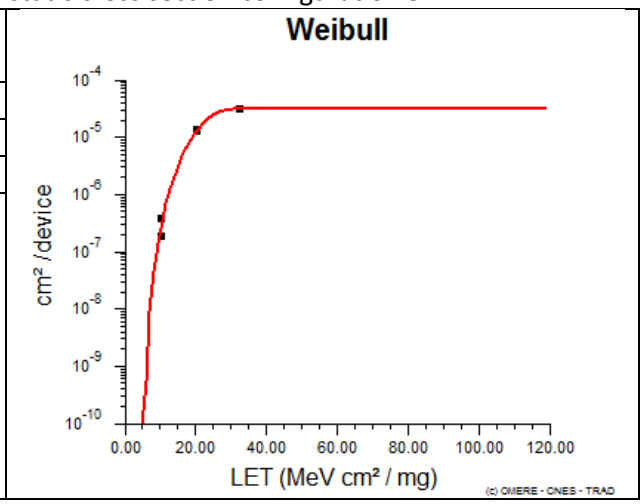


Table 21: SEU static cross section configuration 3

The next table shows the Weibull fit for the SEU static cross section configuration 4:

	Vcomp Xsection
w	33.98
s	2.47
LET threshold	6
Saturation cross section	1.6 E-4

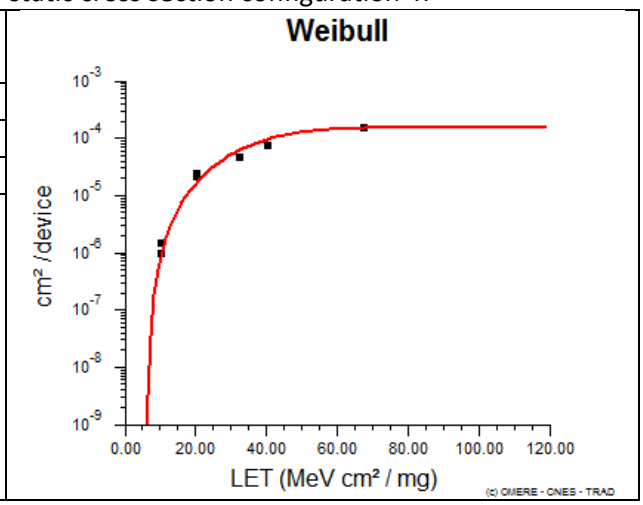


Table 22: SEU static cross section configuration 4

The next table shows the Weibull fit for the SEU static cross section configuration 5:

	Vcomp Xsection
w	14.27
s	2.77
LET threshold	6.9
Saturation cross section	1.6 E-5

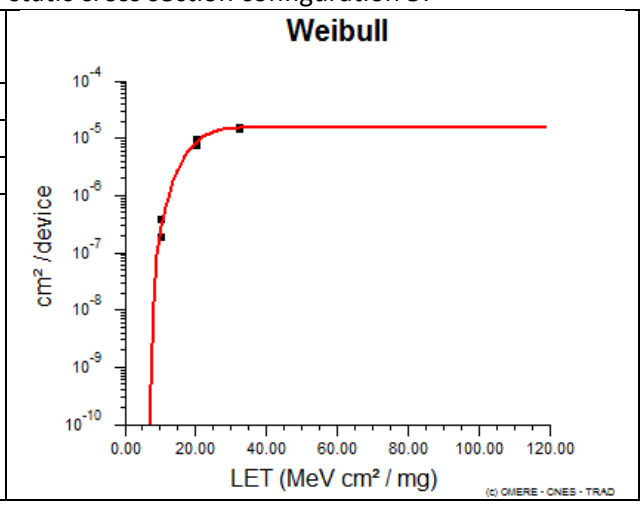


Table 23: SEU static cross section configuration 5

8. Conclusion

Heavy ions test were performed on GR718A. The aim of the test was to evaluate the sensitivity of the device against SEL, SEU and SET.

During this campaign, 169krad were deposited on part No. 1 and 77krad on part No. 3. Both devices remained fully functional.

SEL were tested with fluence of 1e+7 ions/cm2.
No SELs were observed with an LET value of 135.4 MeV.cm²/mg and range 18.5 µm (Xenon heavy ions tilted by 60 degrees) and a temperature >80°C. One sample was also tested at 125°C with no failures.
No SELs were observed with an LET value of 67.7MeV.cm²/mg and range 37 µm (Xenon heavy ions) and a temperature >80°C.

SETs (PLL LOCK signal) were observed on the GR718A at a minimum LET of 20.4 MeV.cm²/mg (Nickel heavy ions) with low input frequency. Within operational range (20-50MHz) few events have been recorded, all with an LET of 32.4 MeV.cm2/mg or above.

SEUs were observed on the GR718A with a minimum LET of 6 MeV.cm²/mg (Neon heavy ions).

Loss of communication with the DUT on the UART link was observed at a minimum LET of 20.4 MeV.cm²/mg (Nickel heavy ions). The error cross section for these events were much lower than the SEU cross sections recorded in e.g. static and dynamic mode.

According to SEUs:

- In dynamic mode the DUT showed difference of sensitivity when one port was derated or not (Configurations 1 and 2). The error cross section was slightly higher with port No.18 derated
- In static mode the sensitivity of the DUT increased with lower voltage on V_{DD}Core (Configurations 3 and 4).
- In static mode the sensitivity of the DUT increased with higher clock frequency (Configuration 4 and 5).
- In dynamic mode the sensitivity of the DUT increased with higher clock frequency (Configuration 1 and 6).
- Testing in static mode with no system clock running demonstrated the hardness of the SEU hardened FFs provided in the DARE 180nm library used in the design.

Conditions	Weibull parameters			
	W	S	LET threshold	Saturation Cross-section
Configuration 1: Dynamic mode, Vcore=1.8V, Vio=3.3V, Baud rate: Port No.18 Derated, CLK=50MHz, PLL: CLKx4	28.35	2.67	6	3.39E-4
Configuration 2: Dynamic mode, Vcore=1.8V, Vio=3.3V, Baud rate: FULL, CLK=50MHz, PLL: CLKx4	21.70	3.2	3.88	1.57E-4
Configuration 3: Static mode, Vcore=1.95V, Vio=3.3V, Baud rate: FULL, CLK=50MHz, PLL: CLKx2	18.18	3.97	4.78	3.36E-5
Configuration 4: Static mode, Vcore=1.65V, Vio=3.3V, Baud rate: FULL, CLK=50MHz, PLL: CLKx2	33.98	2.47	6	1.6E-4
Configuration 5: Static mode, Vcore=1.65V, Vio=3.3V, Baud rate: FULL, CLK=12.5MHz, PLL: CLKx2	14.27	2.77	6.9	1.6E-5
Configuration 6: Dynamic mode, Vcore=1.8V, Vio=3.3V, Baud rate: Port No.18 Derated, CLK=20MHz, PLL: CLKx2	22.78	1.85	7.94	6.8E-5

After completion of this study, Cobham Gaisler has made a new revision of the SpaceWire Router, GR718B. The new revision has been designed with new SEU mitigation concepts. Thus the results reported in this study for GR718A will not be fully representative to GR718B.
Detailed post analysis performed by Cobham Gaisler of all the test data collected in this study has served as input for the design of the new die revision, GR718B. The reporting of this analysis is not within the scope of this report.