HIREX ENGINEERING
A company of ALTER TECHNOLOGY

SINGLE EVENT EFFECTS
TEST REPORT

Test Type:	Heavy ion
Test facility:	RADEF, JYFL, University of Jyvaskyla, Jyvaskyla, Finland
Test Date:	August 2014, October 2014
Part Type:	AD976A
Part Description:	16-Bit, 200 kSPS, BiCMOS A/D Converter
Part Manufacturer:	Analog Devices, USA

ESA contract n° 4000105495/12/NL/SFe dated 27/2/2012

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Written by :	Benjamin Crouzat	Design Engineer		
Authorized by:	F.X. Guerre			

DOCUMENTATION CHANGE NOTICE

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Contributors to this work:

Benjamin Crouzat — Hirex Engineering
Mehdi Kaddour

SEE TEST REPORT

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1 Glossary

DUT: Device under test.

Fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.
In this document, Fluence is expressed in ions per cm2.

Flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.
In this document, Flux is expressed in ions per cm2*s.

Single-Event Effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.
Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL.

Single-Event Transient (SET): A soft error caused by the transient signal induced by a single energetic particle strike.

Single-Event Latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.
SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.
An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.
Single-Event Latch-up (SEL) cross-section: the number of events per unit fluence. For chip SEL cross-section, the dimensions are cm2 per chip.

Error cross-section: the number of errors per unit fluence. For device error cross-section, the dimensions are cm2 per device. For bit error cross-section, the dimensions are cm2 per bit.

Tilt angle: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis
Weibull fit: $F(x) = A\ (1- \exp\{-[(x-x_0)/W]^s\})$ with:

x = effective LET in MeV/(mg/cm^2);
$F(x)$ = SEE cross-section in cm^2;
A = limiting or plateau cross-section;
x_0 = onset parameter, such that $F(x) = 0$ for $x < x_0$;
W = width parameter;
s = a dimensionless exponent.

Error bars: error bars are computed using a confidence level of 95% and a beam flux uncertainty of +/-10% as recommended by Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100.

2 Introduction

This report presents the results of Heavy Ions test program carried out on AD976A part type from Analog Devices, USA. AD976A samples were used for heavy ions testing at RADEF, JYFL, University of Jyvaskyla, Jyvaskyla, Finland.
This work was performed for ESA under ESA contract n° 4000105495/12/NL/SFe dated 27/2/2012.

3 Applicable and Reference Documents

3.1 Applicable Documents

AD-1. Hirex proposal « Test Methods, Requirements, and Guidelines for Evaluation of Radiation Sensitivity of Analog to Digital Converters (ADC), Digital to Analog Converters (DAC) and Vertical Power MOSFETs» HRX/PRO/3624 Issue 01 /2011/10/12

AD-2. AD976A Analog Devices, USA datasheet, Rev. C 1999

3.2 Reference Documents

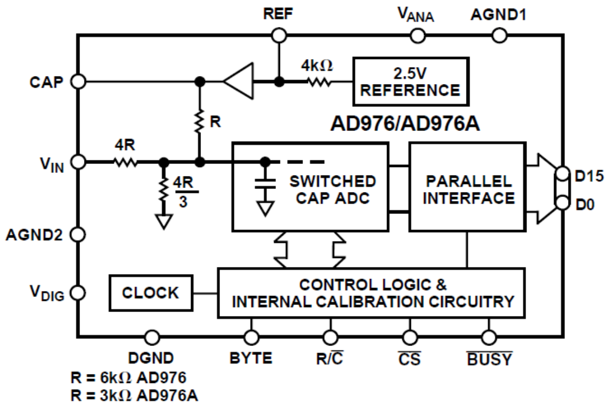
RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

4 DEVICE INFORMATION

4.1 Device description

AD976A is an 16-Bit, 200 kSPS, BiCMOS A/D Converters.

Functional diagram



Part type:	AD976A
Manufacturer:	Analog Devices, USA
Manufacturer lot number:	C6X410965
Datecode:	1306
Package:	DIL-28
Top marking:	AD5962-9756401QXA logo Q 1306 A E233220
Die dimensions:	5535.4µ x 2973.5µ

4.2 Sample preparation

Samples are opened mechanically.

4.3 Sample identification

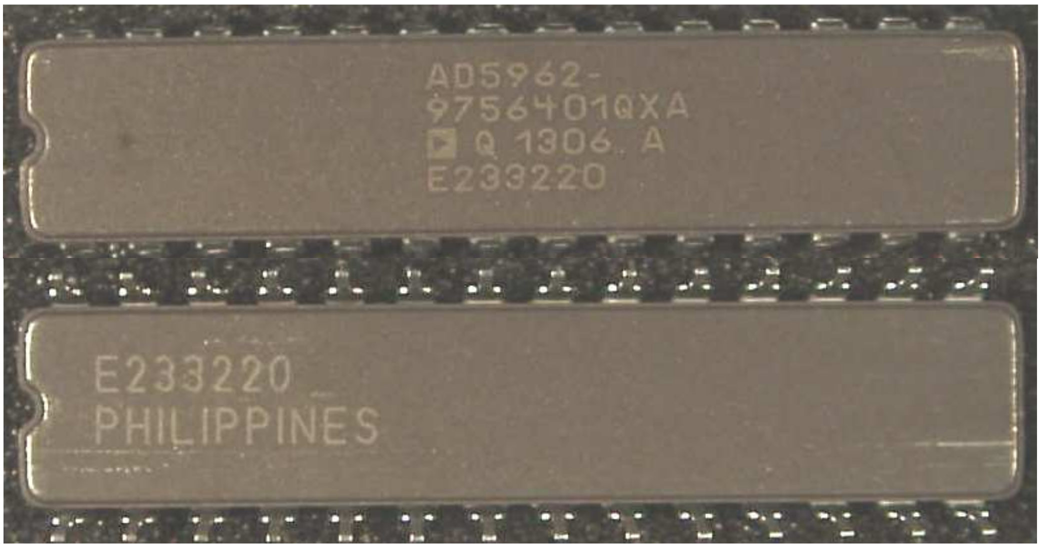


Photo 1 – Device top & bottom view

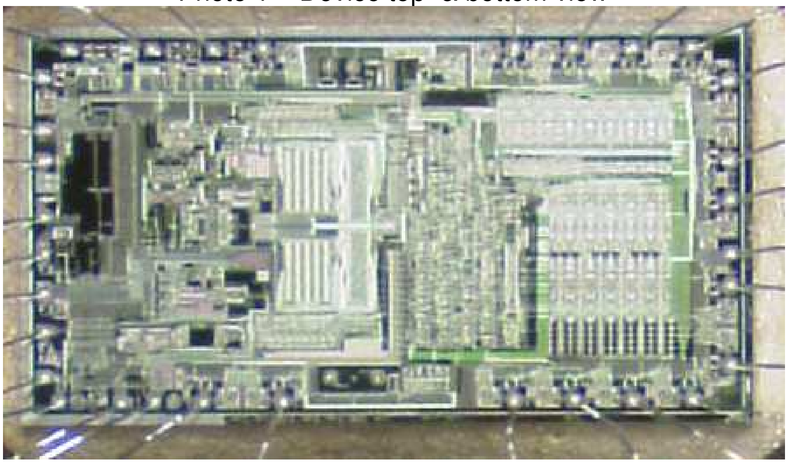


Photo 4 – Die full view

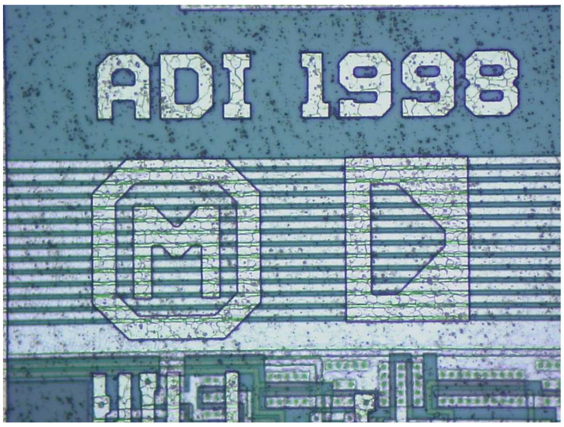


Photo 3 – Die Marking1

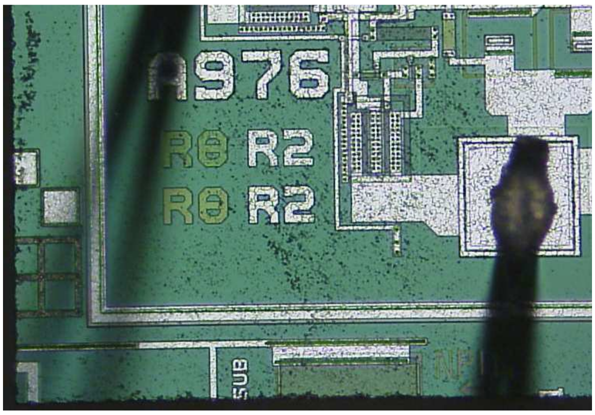


Photo 4 – Die marking2

Figure 1: AD976A device identification

5 RADEF Facility

Test at the cyclotron accelerator was performed at University of Jyvaskyla (JYFL) (Finland) under HIREX Engineering responsibility.
The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.
The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula,

$$130\ Q^2/M,$$

where Q is the ion charge state and M is the mass in Atomic Mass Units.

Test chamber

Irradiation of components is performed in a vacuum chamber with an inside diameter of 75 cm and a height of 81 cm.
The vacuum in the chamber is achieved after 15 minutes of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the X, Y and Z directions. The possibility of rotation around the Y-axis is provided by a round table. The free movement area reserved for the components is 25 cm x 25 cm, which allows one to perform several consecutive irradiations for several different components without breaking the vacuum.
The assembly is equipped with a standard mounting fixture. The adapters required to accommodate the special board configurations and the vacuum feed-throughs can also be made in the laboratory's workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components.
A CCD camera with a magnifying telescope is located at the other end of the beam line to determine accurate positioning of the components. The coordinates are stored in the computer's memory allowing fast positioning of various targets during the test.

Beam quality control

For measuring beam uniformity at low intensity, a CsI(TI) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis.
A set of four collimated PIN-CsI(TI) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.
Two beam wobblers and/or a 0.5 microns diffusion Gold foil can be used to achieve good beam homogeneity. The foil is placed 3 m in front of the chamber. The wobbler-coils vibrate the beam horizontally and vertically, the proper sweeping area being attained with the adjustable coil-currents.

Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI(TI) detectors. Three collimators of different size and shape are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.
At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(TI) detectors.

Ion	LET^{SRIM} at surface [$MeV.cm^2.mg^{-1}$]	Range [µm]	Beam energy [MeV]
$^{20}Ne^{6+}$	3.63	146	186
$^{40}Ar^{12+}$	10.2	118	372
$^{56}Fe^{15+}$	18.5	97	523
$^{82}Kr^{22+}$	32.1	94	768
$^{131}Xe^{35+}$	60.0	89	1217

SRIM-2003.26

Table 1 – Ion beam setting

6 Test Set-up

Test system Figure 2 shows the principle of the Heavy Ion test system.
The test system is based on a Virtex4 FPGA (Xilinx). It runs at 50 MHz. The test board has 168 I/Os which can be configured using several I/O standards.
The test board includes the voltage/current monitoring and the latch-up management of the DUT power supplies up to 24 independent channels.

A SEL event is detected when one of the monitored power supply channel current exceeds the corresponding given threshold current within a few microseconds; it is then followed by a device under test power reset after a given off time.

The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.

Test board has been designed so that 2 samples can be eventually tested at the same time to heavy Two AD976A parts are mounted on the daughter board as shown in Figure 3 and AD976A design schematic is shown in **Erreur ! Source du renvoi introuvable.**.

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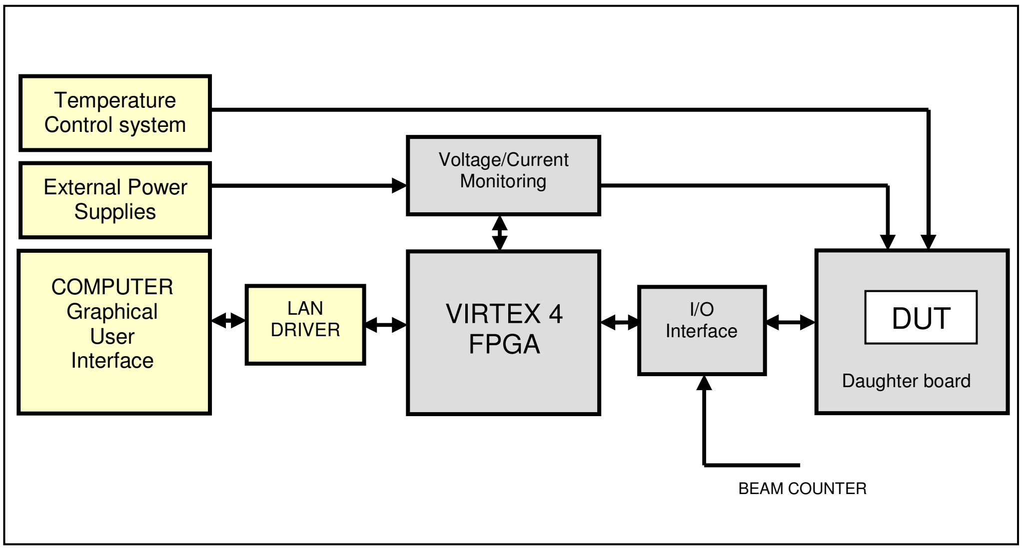


Figure 2: AD976A , Heavy ion test set-up

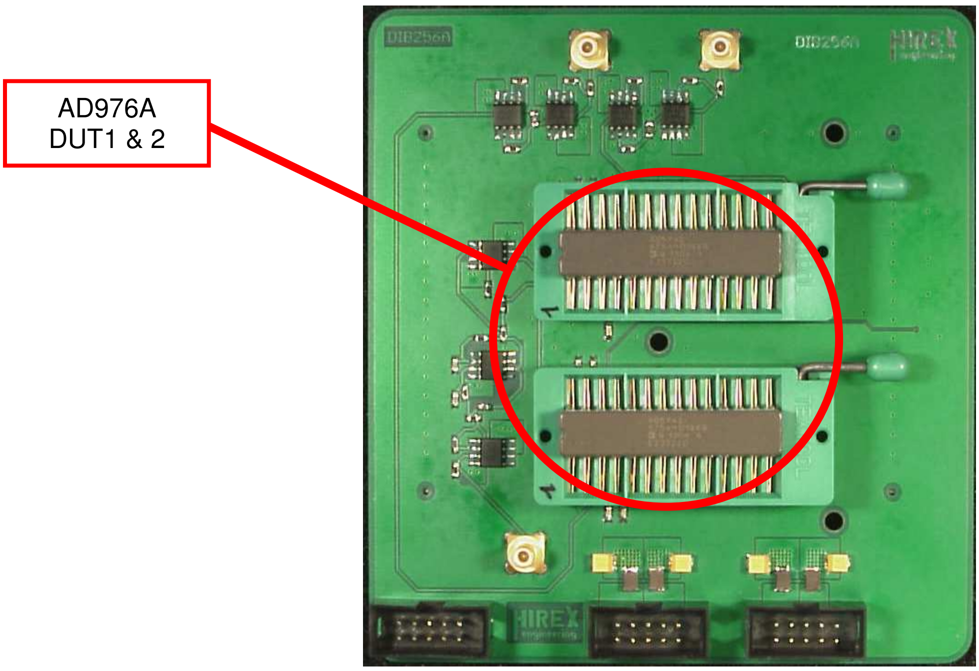


Figure 3: Daughter board (DIB256A) photo

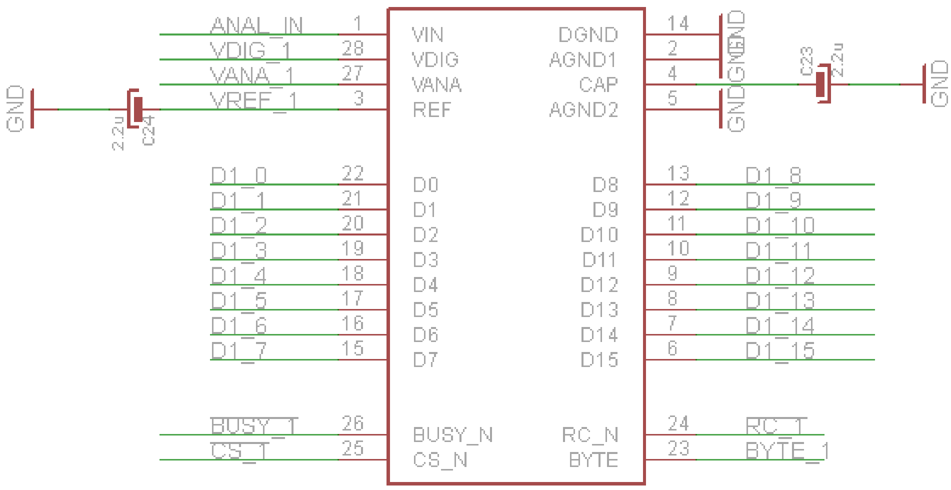


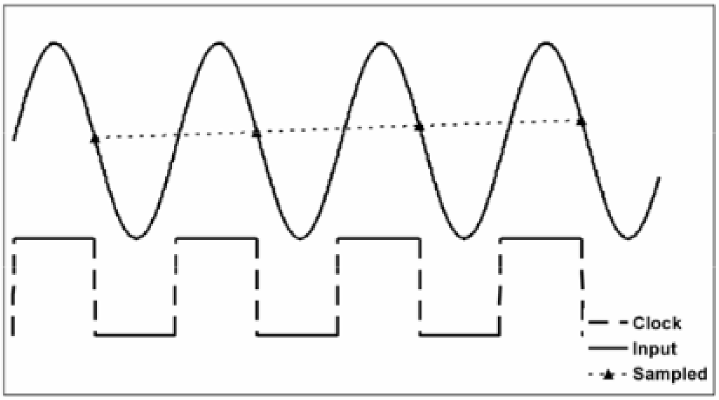
Figure 4: AD976A design schematic

7 Test methods

For this AD converter testing, a sinewave signal is used at AD976A input.
in addition to characterize the SEE behavior of the AD976A , the objective of this test was also to compare the efficiency of different test methods based on different sets of sinewave input frequency and DUT sampling frequency. 3 test methods have then been implemented.

- beat frequency: With the input frequency f_{in} set very close to the sampling frequency, the output code of the ADC is a slow moving sine wave, changing at a rate of 1 LSB per clock cycle.
Input sine frequency f_{in} and sampling frequency f_s must repond to:

$$f_{in}=f_s/(2^N*PI) \text{ with } N=16$$



- 4points: DUT sampling frequency being fixed, the selected frequency of the sinewave input is such that only 4 points of the sine output are converted continuously.
Input sinewave frequency f_{in} and sampling frequency f_s must repond to:

$$f_{in}=f_s/4$$

- Hirex method: DUT sampling frequency being fixed, input frequency f_{in} is set to a much lower value than f_s with f_sa multiple of f_{in}, leading to a significant number of points converted by sinewave input period.
Input sinewave frequency f_{in} and sampling frequency f_s must repond to:
$f_{in}=f_s/m$ with m integer
In the present test, m was typically set to 128.

8 Error detection and recording

For beat frequency, detection when the output shifts from the expected value is done by comparing with the previous clock conversion as it should differ only by 1 LSB and trig the data recording.

For 4 points method, this is achieved by comparing the output with the 4 clock times before output (or a multiple of 4).

For Hirex method, as for 4 points, this is achieved by comparing the output with the m clock times before output (or a multiple of m).

2048 conversions values before the detection trig and 2048 after are recorded wich allows for checking the occurrence of successive conversions in error if any. A conversion is considered in error when the output comparison with the word taken as a reference exhibits a difference higher than the set threshold. This threshold is set by checking that no detection occurs in absence of beam.Wave generation hardware
A specific board has been designed to produce a clock signal of frequency f_s in phase with a sine signal at the desired input frequency f_{in}, so that the three test methods can be implemented easily.
Wave generation board principle is shown in Figure 5.

A single oscillator is used to produce the system's clock. This clock feeds the FPGA's Direct Digital Synthesis (DDS) block on one hand, and the external Digital to Analog Converter (DAC).
The DDS combined to the Signal processing block can produce square and/or sinus waveforms independantly with an accuracy inferior to the millihertz for each signal frequency.
We can also set the amplitude and the offset of these output signals before the analogic conversion. The waveforms are then converted via the DAC, amplified and symetrised if needed before entering the DUT.
The major benefit of this system is to generate two different waveforms from one single system clock. Then we can create two signals at the exact same frequency with no chance to see any unwanted phase shift. Moreover the system allows us to set the phase shift between these two signals very precisely if we want some phase shift. This can be usefull for the 4 points testing method : we can choose what are the 4 points on the sinewave we want to observe.

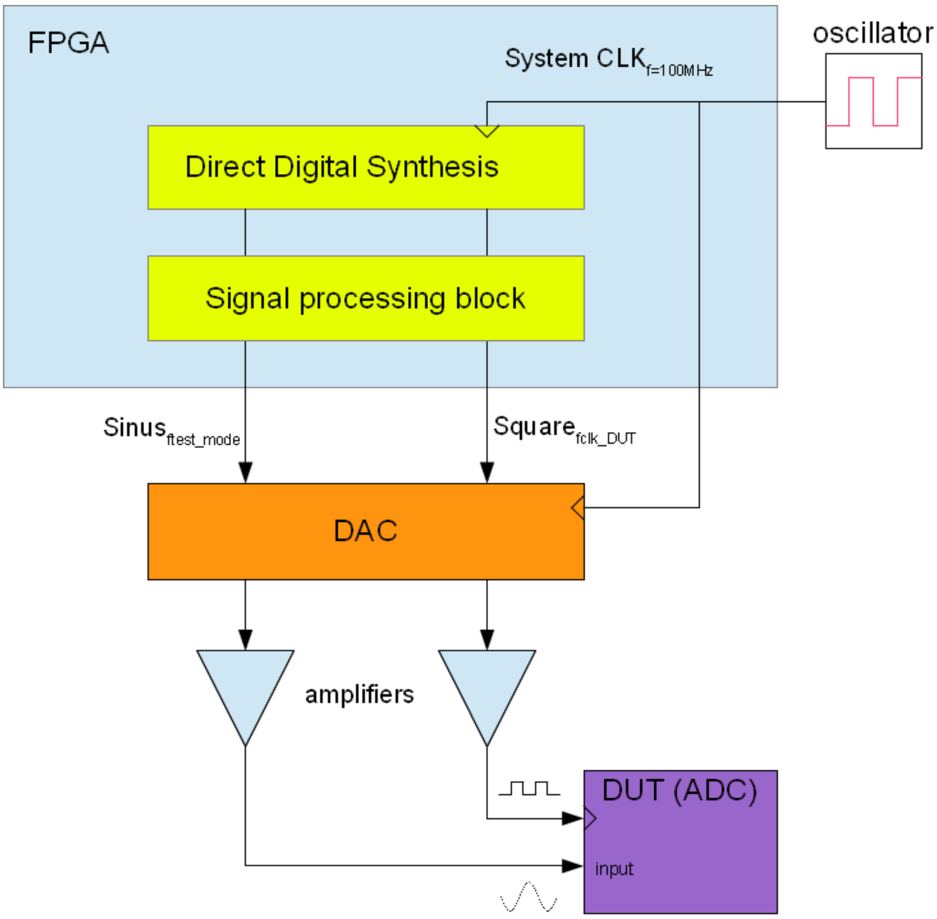


Figure 5 – Wave generation schematic

9 Bias conditions

- Vdig 5V
- Vana 3.3V
- Room temperature
- Internal reference
- INmax +/-10Vpp

Figure 6 – Bias conditions

10 SEE Test Results

1 sample is tested at a time (DUT1 or DUT2) using bias conditions of Figure 6.
The three test methods have been applied with the following sets of frequencies during 2 test campaigns in August 2014 (W35) and October 2014(W44).

	Input sinus			AD976A
	4points	hirex	beat freq	conversion frequency
W35	50 000 Hz	1 560 Hz		200 000 Hz
W44			199 999.03 Hz	

Input sinewave amplitude was adjusted closed to fullscale. Value of 1 LSB corresponds to 305 µV.

10.1 SEU

Figure 7 show the different digital output waveforms for the three different methods.
The presence of noise at DUT output requires to apply a detection threshold without exposure between 30 and 95 LSBs.
Because of a limitation in test software, the output value is compared to the previous one 2 clocks before instead of 1 clock for beat frequency event detection. Impact on the word output comparison with the previous output value is then 2 LSBs instead of 1. Practically it does not change the test method as the threshold set includes also the noise level which is as a minimum 30 LSBs.
Run details and results are provided in Table 2. All runs were performed with normal incidence beam (no tilt).
Event cross sections have been calculated by taking into account the number of events with a detection threshold of 70LSBs. Table provides also the low and up limits computed with 95% confidence level and a 10% uncertainty on fluence.
In Table 2 for each run, the detection threshold level in LSBs is noted (column “threshold (LSBs)”) togeteher with the number of events detected (column ‘Nb events above threshold”). As this threshold is not identical for all runs and to ease comparison, we have extracted the number of events which would have been triggered with a threshod of 70LSBs: see column “NB events above 70LSBs”.
Column ‘period’ refers to the number of clocks to which output value is compared to the current conversion output.
In addition, the table provides the error bar values computed as indicated in §1.
Figure 8 show the event cross-section for each test method implemented during this exercise. As it can be observed these methods give similar cross-section curves. However for W35, both Hirex method and 4 points method show a lower values that can be expected with krypton. Careful analysis of the data did not reveal any discrepanciy and then beam calibration might be questionned.

Figure 9 shows the amplitude distribution in % for thr three methods (all runs cumulated)

week	run	radef run_number	test_mode	Ion	power_config	temperature	board_id	DUT_part_id	period	threshold (LSBs)	LET	fluence	run_duration	Nb events above threshold	Nb events above 70 LSBs	up	low	let	X-section	X-section up	X-section low
35	2	148	4 points	Kr	5V	Room	1	1	32	30	32.1	1.29E+05	104	194	102	123.8	83.2	32.2	7.91E-04	9.60E-04	6.45E-04
35	25	167	4 points	Fe	5V	Room	1	1	4	70	18.5	1.36E+05	61	111	111	133.7	91.3	18.5	8.16E-04	9.83E-04	6.71E-04
35	30	226	4 points	Ne	5V	Room	1	1	4	55	3.63	2.27E+05	105	107	88	108.4	70.6	3.63	3.88E-04	4.78E-04	3.11E-04
35	19	161	4 points	Xe	5V	Room	1	1	4	65	60	1.04E+05	209	103	99	120.5	80.5	60	9.52E-04	1.16E-03	7.74E-04
35	41	236	4 points	Ar	5V	Room	1	1	4	55	10.2	1.69E+05	121	102	86	106.2	68.8	10.2	5.09E-04	6.28E-04	4.07E-04
35	16	159	4 points	Xe	5V	Room	1	2	4	60	60	9.89E+04	193	101	87	107.3	69.7	60	8.80E-04	1.09E-03	7.05E-04
35	6	152	4 points	Kr	5V	Room	1	2	32	42	32.1	1.70E+05	154	197	129	153.3	107.7	32.2	7.59E-04	9.02E-04	6.34E-04
35	26	168	4 points	Fe	5V	Room	1	2	4	70	18.5	1.43E+05	64	109	109	131.5	89.5	18.5	7.62E-04	9.19E-04	6.26E-04
35	33	228	4 points	Ne	5V	Room	1	2	4	55	3.63	2.55E+05	133	103	90	110.6	72.4	3.63	3.53E-04	4.34E-04	2.84E-04
35	45	240	4 points	Ar	5V	Room	1	2	4	55	10.2	1.74E+05	66	112	99	120.5	80.5	10.2	5.69E-04	6.93E-04	4.62E-04
44	2	21	beat freq	Ne	5V	Room	1	1	2	70	3.63	1.56E+06	507	546	546	593.8	501.2	3.63	3.50E-04	3.81E-04	3.21E-04
44	7	24	beat freq	Ar	5V	Room	1	1	2	72	10.2	4.56E+05	445	262	262	295.7	231.2	10.2	5.75E-04	6.49E-04	5.07E-04
44	8	25	beat freq	Fe	5V	Room	1	1	2	73	18.5	4.01E+05	768	277	277	311.6	245.3	18.5	6.91E-04	7.77E-04	6.12E-04
44	11	28	beat freq	Kr	5V	Room	1	1	2	73	32.1	3.09E+05	255	251	251	284.0	220.9	32.2	8.12E-04	9.19E-04	7.15E-04
44	12	29	beat freq	Xe	5V	Room	1	1	2	73	60	2.96E+05	496	314	314	350.7	280.2	60	1.06E-03	1.18E-03	9.47E-04
44	3	22	beat freq	Ne	5V	Room	1	2	2	70	3.63	6.87E+05	222	201	201	230.8	174.2	3.63	2.93E-04	3.36E-04	2.54E-04
44	5	23	beat freq	Ar	5V	Room	1	2	2	70	10.2	5.05E+05	519	303	303	339.1	269.8	10.2	6.00E-04	6.72E-04	5.34E-04
44	9	26	beat freq	Fe	5V	Room	1	2	2	72	18.5	3.35E+05	653	260	260	293.6	229.4	18.5	7.76E-04	8.76E-04	6.85E-04
44	10	27	beat freq	Kr	5V	Room	1	2	2	72	32.1	2.77E+05	507	260	260	293.6	229.4	32.2	9.39E-04	1.06E-03	8.28E-04
44	13	30	beat freq	Xe	5V	Room	1	2	2	72	60	2.37E+05	416	287	287	322.2	254.8	60	1.21E-03	1.36E-03	1.07E-03
35	1	147	Hirex's classic	Kr	5V	Room	1	1	256	95	32.1	2.96E+05	240	204	204	234.0	177.0	32.2	6.89E-04	7.91E-04	5.98E-04
35	10	155	Hirex's classic	Xe	5V	Room	1	1	128	70	60	1.13E+05	171	112	112	134.8	92.2	60	9.91E-04	1.19E-03	8.16E-04
35	28	170	Hirex's classic	Fe	5V	Room	1	1	128	70	18.5	1.29E+05	72	103	103	124.9	84.1	18.5	7.98E-04	9.68E-04	6.52E-04
35	37	232	Hirex's classic	Ne	5V	Room	1	1	128	60	3.63	1.45E+05	217	88	64	81.7	49.3	3.63	4.40E-04	5.62E-04	3.39E-04
35	40	235	Hirex's classic	Ar	5V	Room	1	1	128	60	10.2	1.75E+05	117	100	81	100.7	64.3	10.2	4.63E-04	5.75E-04	3.68E-04
35	9	154	Hirex's classic	Kr	5V	Room	1	2	128	45	32.1	2.36E+05	228	188	142	167.4	119.6	32.2	6.02E-04	7.09E-04	5.07E-04
35	11	156	Hirex's classic	Xe	5V	Room	1	2	128	70	60	9.19E+04	140	103	103	124.9	84.1	60	1.12E-03	1.36E-03	9.15E-04
35	27	169	Hirex's classic	Fe	5V	Room	1	2	128	70	18.5	1.41E+05	67	103	103	124.9	84.1	18.5	7.30E-04	8.86E-04	5.96E-04
35	38	233	Hirex's classic	Ne	5V	Room	1	2	128	60	3.63	1.72E+05	179	91	62	79.5	47.5	3.63	3.60E-04	4.62E-04	2.76E-04
35	39	234	Hirex's classic	Ar	5V	Room	1	2	128	60	10.2	1.70E+05	157	98	75	94.0	59.0	10.2	4.41E-04	5.53E-04	3.47E-04

In the column “above 70LSBs”, a red mark means that the threshold was higher than 70LSBs and was the one in the “threshold” column.

Table 2 – RADEF, August 2014(W35) and October(W44), AD976A , run table

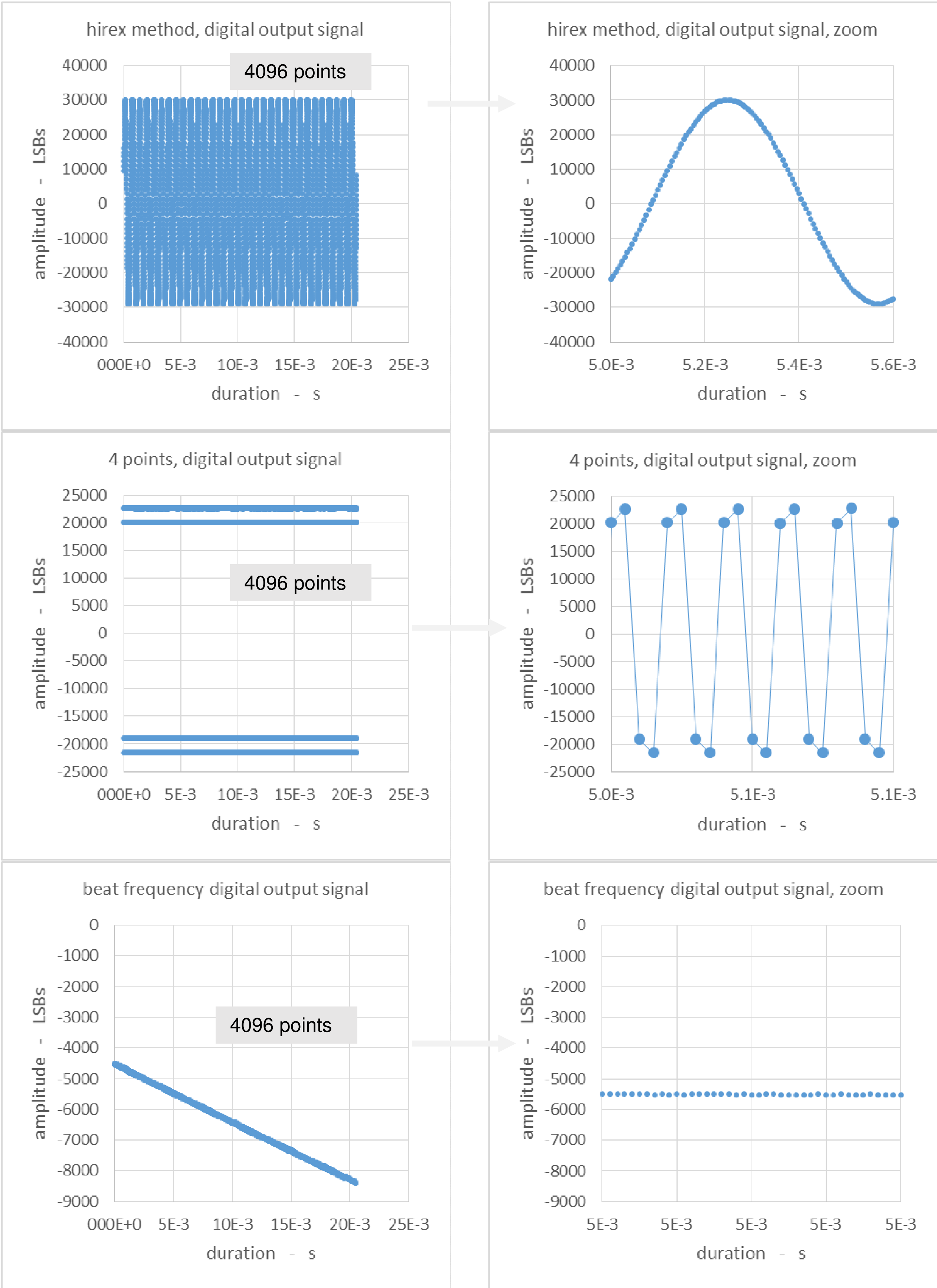


Figure 7 – Digital output waveform with the 3 different methods

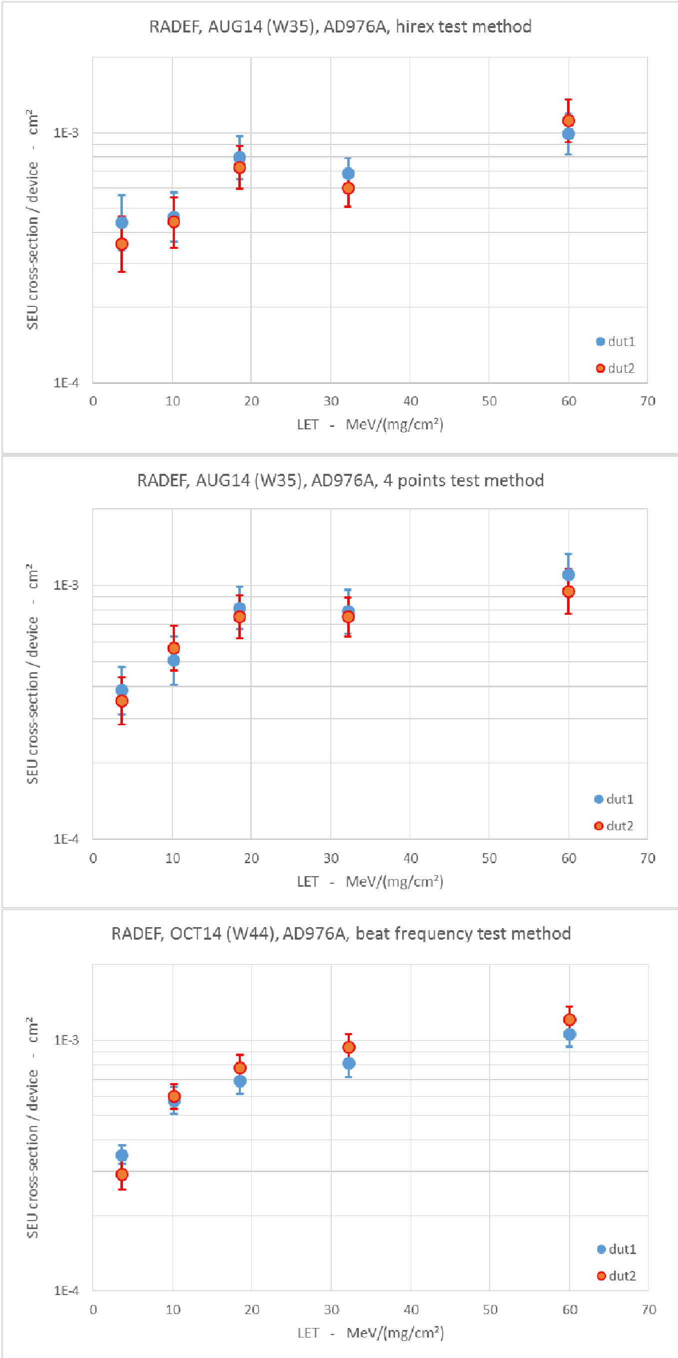


Figure 8 – SET event cross-section for the three test methods

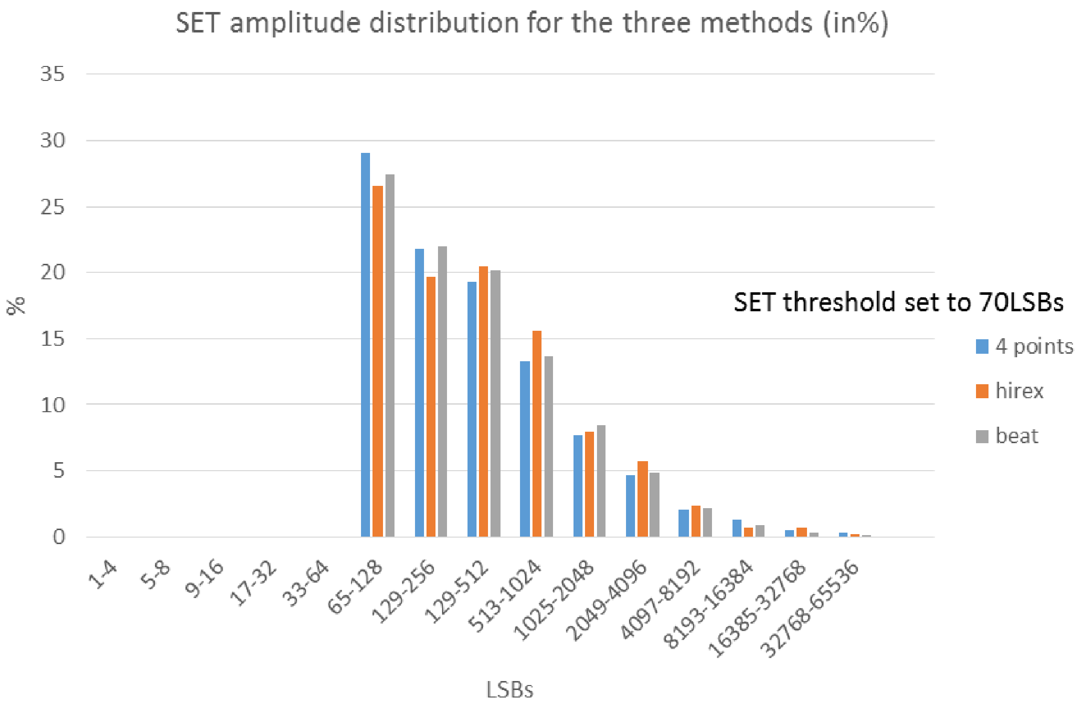


Figure 9 – radef August / October 2014, SET amplitude distribution in % for the three methods

10.1.1 Hirex method

Figure 10 shows the worstcase conversion error amplitude of w35, run039 time stamped at 5110.928800540s.
Most of the events are only 1 conversion in error. In run009, run010 and run040, 1 event was 2 successive conversions in error, all the others were 1 conversion in error.

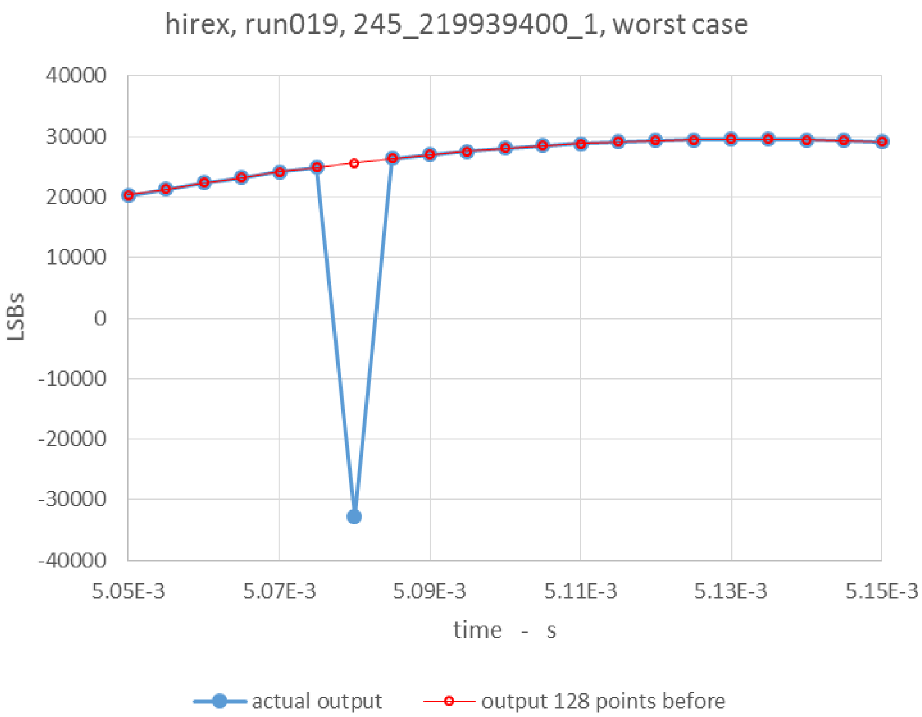


Figure 10 – W35, run039, worstcase single conversion error (error amplitude is 58440LSBs)

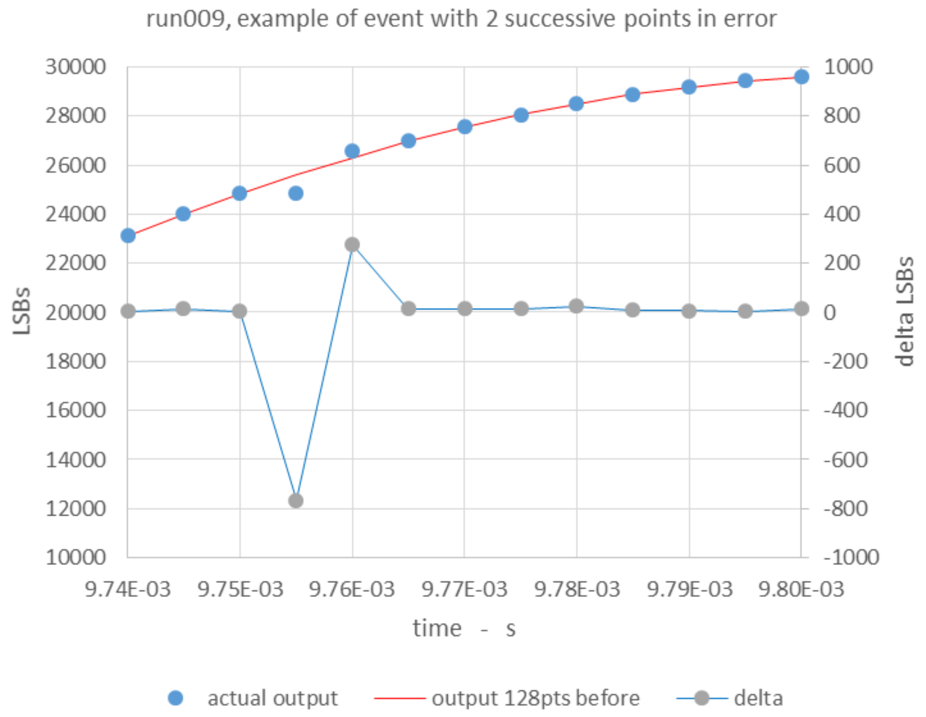


Figure 11 – W35, run009, example of two successive conversions event

10.1.2 <u>4 points method</u>

Most of the events are only 1 conversion in error. In run006, run025 and run026, 1 event was 2 successive conversions in error and all the others were 1 single conversion in error.
Figure 12 shows the worstcase conversion error amplitude of w35, run002 time stamped at 3654.824320960s.

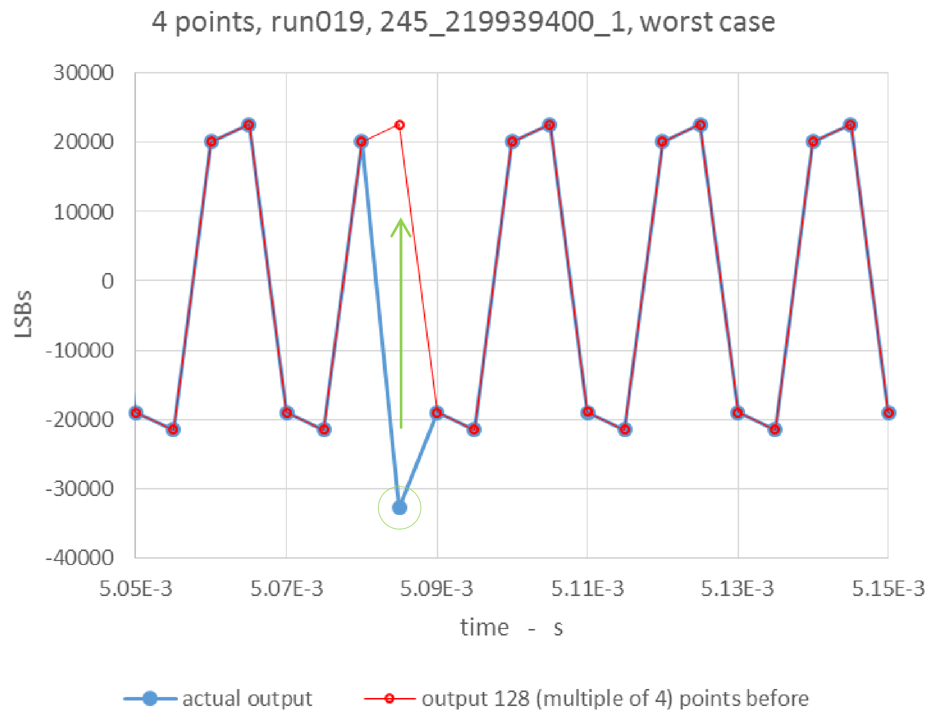


Figure 12 – W35, run019, worstcase single conversion error (error amplitude is -55392LSBs)

10.1.3 Beat frequency

All events are only 1 conversion in error.
Figure 13 shows the worstcase conversion error amplitude of w44, run012 time stamped at 6797.016412760s.

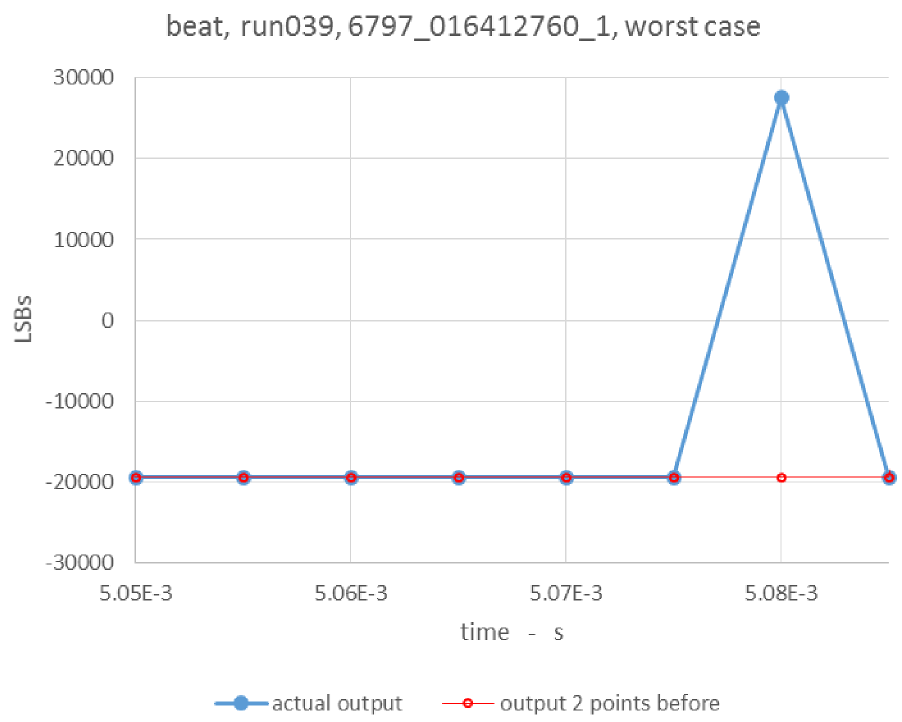


Figure 13 – W44, run012, worstcase single conversion error (error amplitude is 47039LSBs)

10.2 SEL

No latchup has been detected for any run with LETs up to 60MeV/(mg/cm²)
As an example, Figure 14 show the recorded supply current plots recorded for 1 DUT under exposure with Xenon (LET =60).

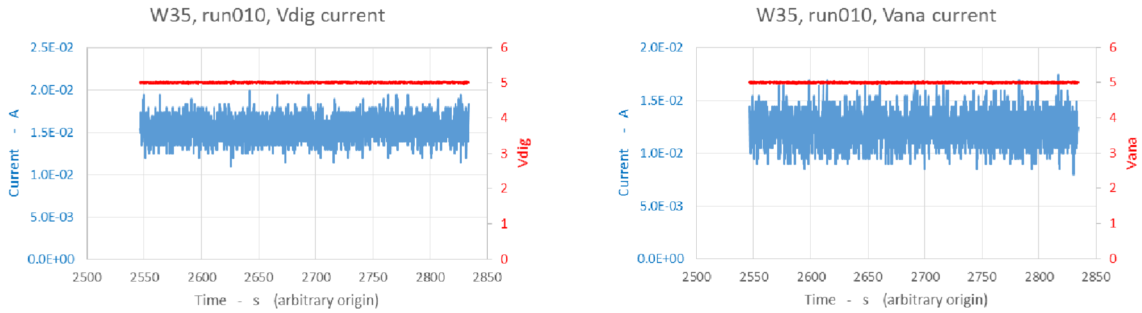


Figure 14 – radef, August 2014 (W35), AD976A , hirex run010, Xenon, dut1 supply currents

11 Conclusion

Three test methods, hrx method, 4 points method and beat frequency method have been implemented and give similar results in term of SEU cross-section curve as a function of LET. Most events are single conversion errors. No event with 2 successive errors have been observed with the beat frequency method while few have been observed with both 4 points and hirex methods.