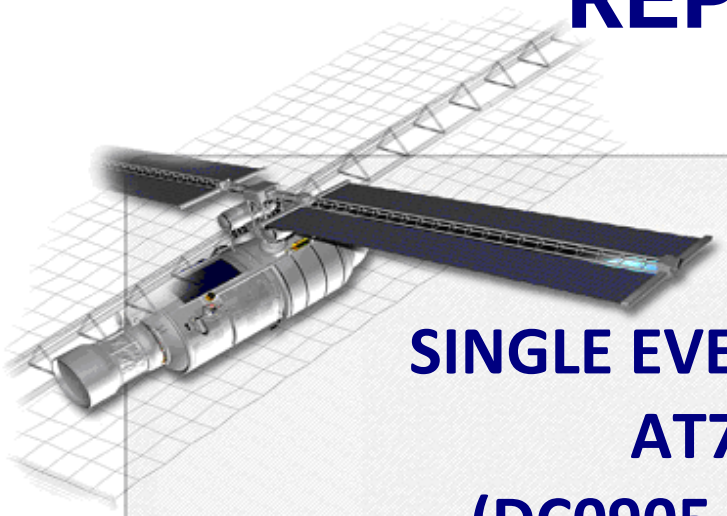
HEAVY IONS TEST REPORT



SINGLE EVENT EFFECTS
AT7913
(DC0905 - DC1229)
SpaceWire Remote Terminal Controller
From
ATMEL

TRAD/TI/AT7913/XXX1/ESA/ELG/1211		Labège, 30th January 2015
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Revision 0:	First Issue dated of 16/07/2014
Revision 1:	Multiple modifications following comments by C. Poivey and J. Ilstad of 17/09/2014
Revision 2:	Add results of second campaign
Revision 3:	Multiple modifications following comments by C. Poivey of 10/12/2014

To:	**ESA** **POIVEY Christian**	Project/Program: COO2 Ref: ESA contract 4000105666

CONTENTS

FIGURES

TABLES

1. Introduction

This report includes the test results of the heavy ion Single Event Effects (SEEs) test sequence carried out on the AT7913, a SpaceWire Remote Terminal Controller from ATMEL.

This test was performed on two global campaigns for ESA at U.C.L. in Louvain-La-Neuve. The first campaign was performed from the 04th till the 05th of June 2014 with the participation of the ESA Technical Officer Christian Poivey and the second campaign was performed from 29th September till the 1st October. During the test two samples were irradiated.

This test was performed for ESA on the AT7913 susceptible to show Single Event Upset (SEUs), Multiple Bit Upset (MBU) and Single Event Functional Interrupt (SEFI) induced by heavy ions.

2. Documents

2.1. Applicable documents

Technical Proposal: TRAD/P/ESA/COO2/AV/220713 rev.1.
Irradiation test plan: TRAD/ITP/ESA/COO2/ELG/130114 Rev.0

2.2. Reference documents

Data Sheet: RTC-100-0012, December 2009, Version 2.4
User Manual: SpaceWire Link Analyser Mk2, Software Version 4.10
User Manual: SPW-RTC Development Unit, Rev. 1.0, 2008-04-10
User Manual: LEON-FT SEU32 Test software, Rev. 1.3-TRAD, 2013-12-13
Schematic: GR-SPWRTC-DEV, Rev. 0.0, 2007-10-18

3. Organization of Activities

The devices for the test were supplied by ESA (4 Parts) and procurred by TRAD (4 parts). The delidding of the parts was performed by TRAD. The testing board and the testing software were developed by TRAD. Before the campaign the samples were checked-out and the test bench was validated with a californium test at TRAD. The heavy ions campaign was performed by TRAD under the supervision of Mr Poivey from ESA. The next table summarises the responsible entity for each activity of this project.

1	Procurement of Test Samples	ESA and TRAD
2	Preparation of Test Samples (delidding)	TRAD
3	Preparation of Test Hardware and Test Program	TRAD
4	Samples Check out	TRAD
5	Accelerator Test	ESA and TRAD
6	Heavy Ion Test Report	TRAD

Table 1: Organization of activities

4. Parts information

4.1. Device description

The AT7913E SpaceWire RTC is a complex system with multiple functions, like FIFO Interface, GPIO and Leon PIO, LEON2-FT Processor, External memory controller, ADC/DAC interface, Space wire interface, CAN interface, on chip memory, 32-bit Timer and UART serial link.

4.2. Identification

Type:	AT7913
Manufacturer:	ATMEL
Function:	SpaceWire Remote Terminal Controller

4.3. Procurement information

Packaging:	MCGA 349	
Date Code:	0905	1229
Part number:	5,6,15 & 16	
Lot No.:		1T5901-1A
Sample size:	4 parts supplied by ESA. No part was irradiated.	4 parts procured by TRAD. 2 parts were irradiated

4.4. Sample Preparation

All parts were delidded by TRAD. A functional test sequence was performed on delidded samples to check that devices were not degraded by the delidding operation.
During the functional test, all parts were tested with all peripherals with the SEE test bench.
The bounding of one part was damaged during the delidding operation and when the functional test was performed, the sample could not be programmed.

4.5. Sample pictures

4.5.1. External view of DC0905

Figure 1: package marking (top)

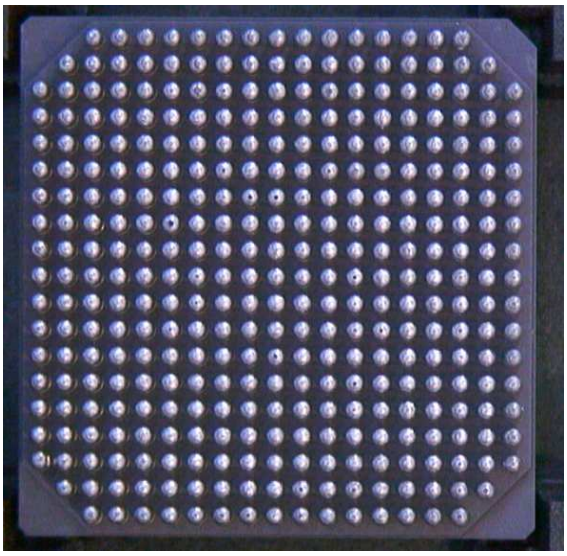


Figure 2: package marking (bottom)

4.5.2. External view of DC1229

Figure 3: package marking of DC1229 (top)

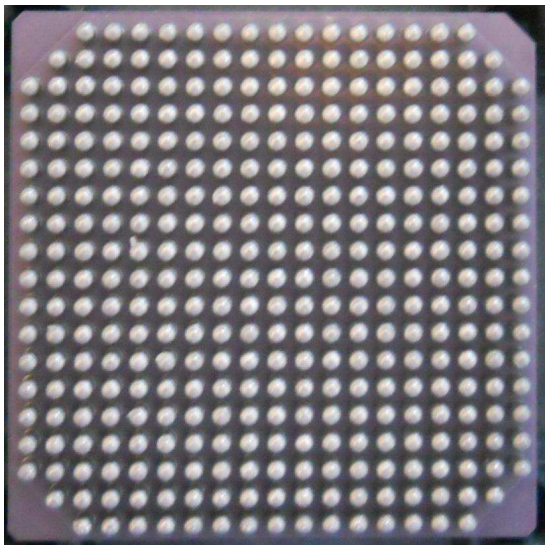


Figure 4: package marking of DC1229 (bottom)

4.5.3. Internal view of DC0905

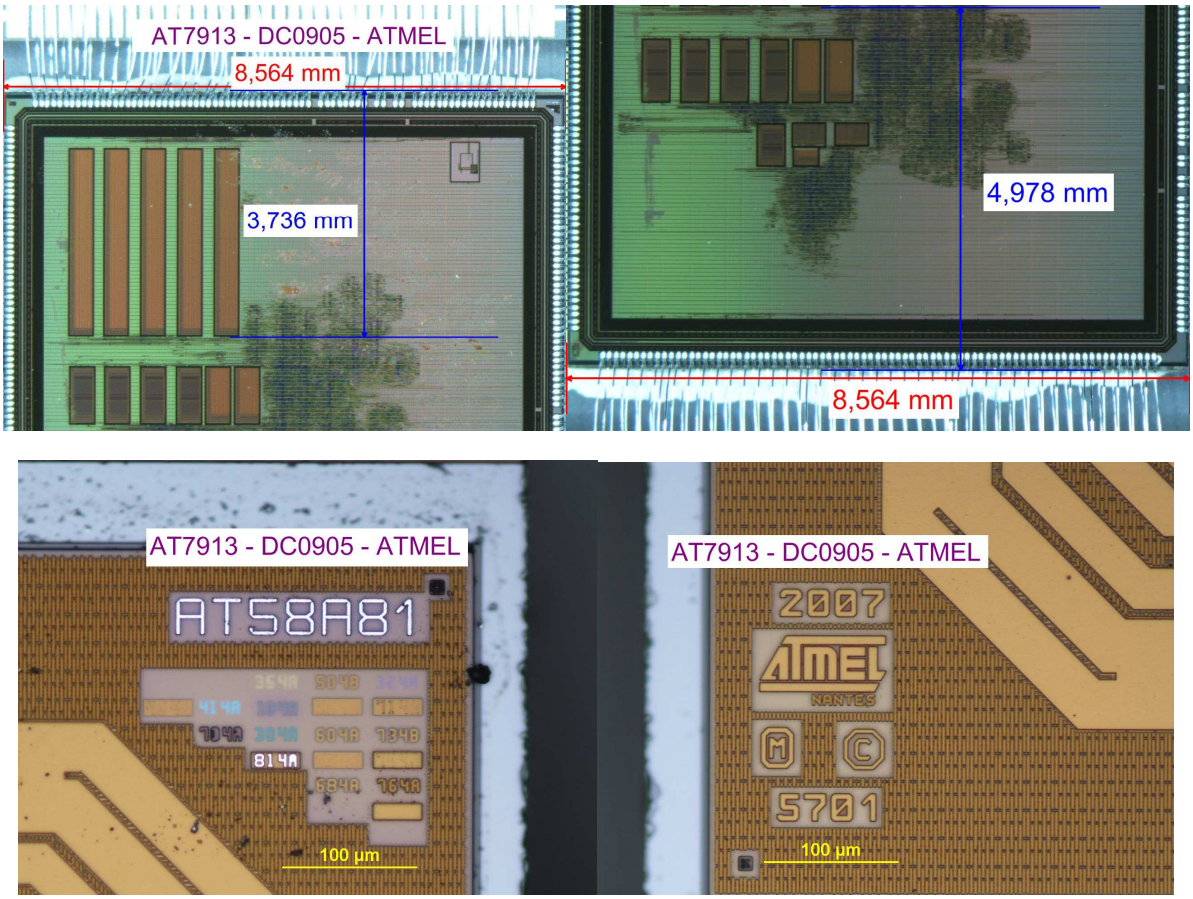


Figure 5: Internal overall view of DC0905

4.5.4. Internal view of DC1229

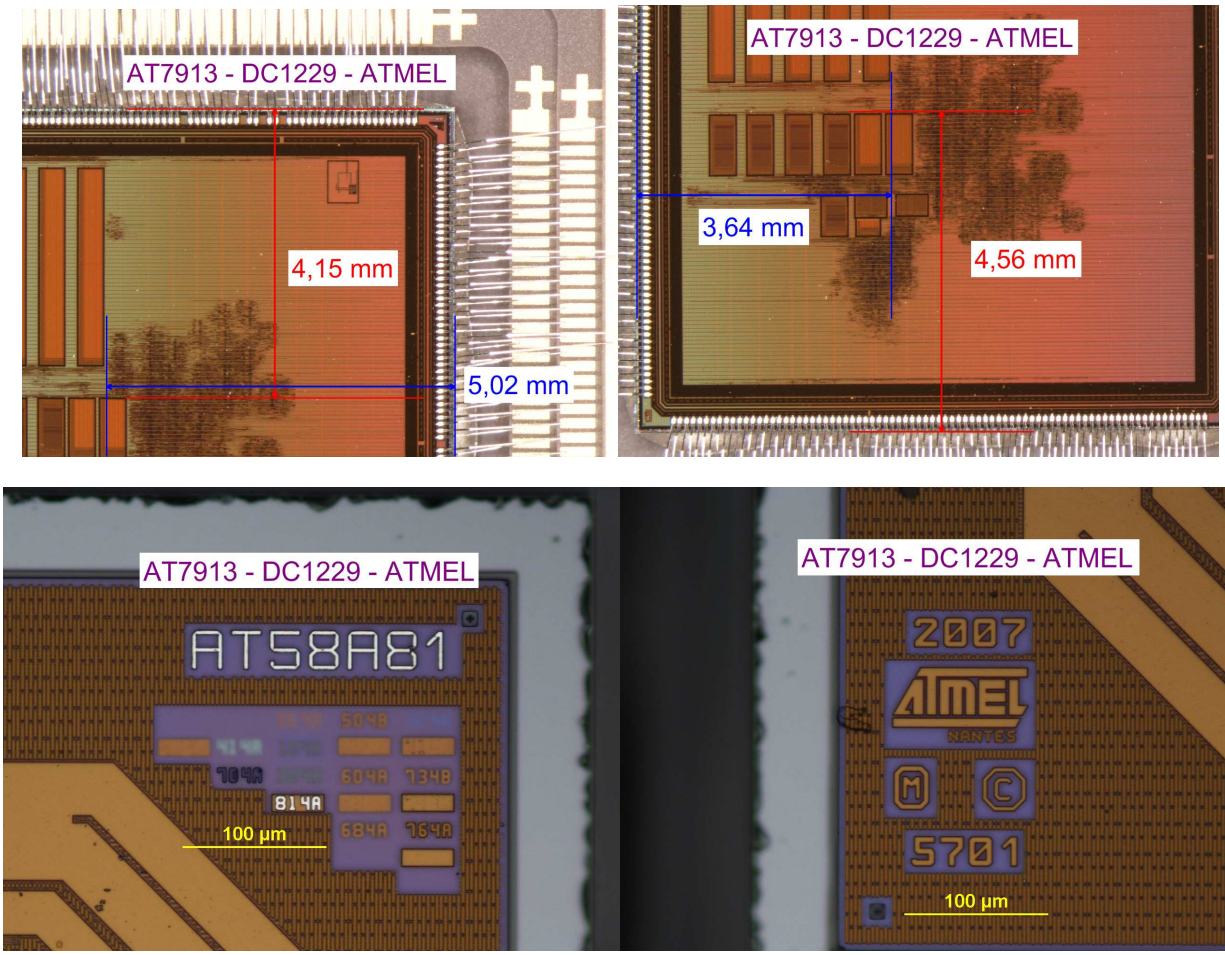


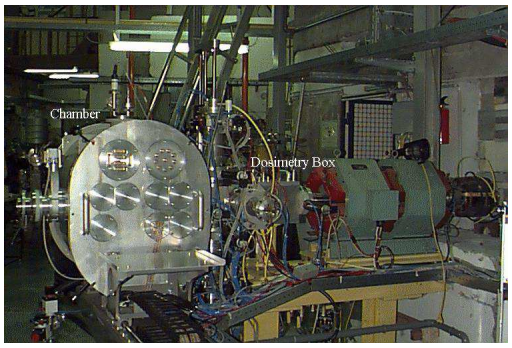
Figure 6: Internal overall view of DC1229

5. Dosimetry and Irradiation Facilities

The test was performed at U.C.L (Université Catholique de Louvain) on 4-5 June 2014 for the first campaign and on 29 September till 1 October 2014 for the second campaign. Two delidded samples were irradiated.

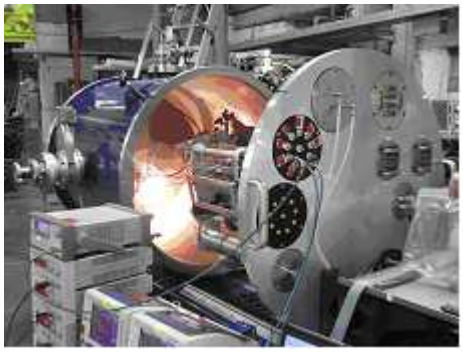
5.1. UCL Heavy Ion Test Facility (Université Catholique de Louvain - Belgium)

The CYClotron of LOuvain la NEuve (CYCLONE) is a multi-particle, variable energy, cyclotron capable of accelerating protons (up to 85 MeV), alpha particles and heavy ions.
For the heavy ions, the covered LET range is between 1.2 MeV.cm².mg^{-1} and 67.7 MeV.cm².mg^{-1}. Heavy ions available are separated in two "Ion Cocktails" named M/Q=5 and M/Q=3.3.



One of the main advantages of the UCL Heavy Ion Test Facility is the fast changing of ion species. Within the same cocktail, it takes only a few minutes to change from one ion to another.

The chamber has the shape of a barrel stretched vertically; its internal dimensions are 71 cm in height, 54 cm in width and 76 cm in depth. One side flange is used to support the board frame (25 X 25 cm) and user connectors.
The chamber is equipped with a vacuum system.



5.2. Dosimetry

To control and monitor the beam parameters, a dosimetry box is placed in front of the chamber.
It contains a faraday cup, 2 Parallel Plate Avalanche Counters (PPAC).
Two additional surface barrier detectors are placed in the test chamber.
The faraday cup is used during beam preparation at high intensity.
A beam uniformity measurement is performed with a collimated surface barrier detector. This detector is placed on a X and Y movement. The final profile is drawn and the ± 10 % width is calculated. The Homogeneity is ± 10 % on a 25 mm diameter.
During the irradiation, the flux is integrated in order to give the delivered total fluence (particule.cm^{-2}) on the device.

5.3. Beam characteristics

The beam flux is variable between a few particles $s^{-1}cm^{-2}$ and $10^4 s^{-1}cm^{-2}$ and is set depending on the device sensitivity. At UCL, Heavy ions available are separated in two "Ion Cocktails", one for the High LET (M/Q=5) and a second one for the High Range (M/Q=3.3). Here bellows are given the characteristics of each cocktail. During the first campaign, the irradiations were performed with the High range cocktail (table 3 in yellow) and during the second campaign, the irradiations were performed with the High LET cocktail (Table°2 in yellow).

Ion	Energy (MeV)	Range (µm(Si))	LET (MeV.cm².mg^{-1})
$^{15}N^{3+}$	60	59	3.3
$^{20}Ne^{4+}$	78	45	6.4
$^{40}Ar^{8+}$	151	40	15.9
$^{84}Kr^{17+}$	305	39	40.4
$^{124}Xe^{25+}$	420	37	67.7

Table 2: UCL cocktail M/Q=5

Ion	Energy (MeV)	Range (µm(Si))	LET (MeV.cm².mg^{-1})
$^{13}C^{4+}$	131	292	1.1
$^{22}Ne^{7+}$	235	216	3
$^{40}Ar^{12+}$	372	117	10.2
$^{58}Ni^{18+}$	567	100	20.4
$^{83}Kr^{25+}$	756	92	32.6

Table 3: UCL cocktail M/Q=3.3

6. Test Procedure and Setup

6.1. Test procedure

6.1.1. Description of the test method

Runs were performed up to a fluence of 1E+6 ions/cm^2 and the flux was adjusted depending on the sensibility of each function but did not exceed a maximum flux of 1E+4 ions.cm^{-2}.s^{-1} for the SEU, SET, SEFI and MBU detection.
The test was terminated when the maximum fluence was reached or when over one hundred errors were detected.

6.1.2. Description of SEE detection methodology

Due to the complexity of the component, each function (peripheral) of the AT7913 was independently tested for the purpose of identifying more easily the function which has generated the errors.

However each test programme for the LEON2FT uses a common framework consisting of the following:

- Configuration of registers is initialised, memory banks are defined, and the use of the cache memories is configured.
- The processor enters an infinite loop.
- The bit “Break on error” of register “DSU control register” forces the processor to a debug mode when the processor would have entered in an error condition (except for the seu32 test bench). The processor freezes when it enters in debug mode. The host software detects that the processor has frozen and it saves all registers before performing a reset of the processor. The SPARC trap type that caused the processor to enter in debug mode is indicated in the DSU trap register (the trap code signals which trap was triggered, see Table 4)

LEON adheres to the general SPARC trap model. The table below shows the implemented trap and their individual priority.

reset	*0x00*	1	Power-on reset
write_error	*0x2B*	2	Write buffer error
instruction_access_exception	*0x01*	3	Error during instruction fetch Edac uncorrectable error during instruction fetch
illegal_instruction	*0x02*	5	UNIMP or other un-implemented instruction
privileged_instruction	*0x03*	4	Execution of privileged instruction in user mode
fp_disabled	*0x04*	6	FP instruction while FPU disabled
cp_disabled	*0x24*		Co-processor instruction while co-processor disabled
watchpoint_detected	*0x0B*	7	Instruction or data watchpoint match
window_overflow	*0x05*	8	SAVE into invalid window
window_underflow	*0x06*		RESTORE into invalid window
register_hardware_error	*0x20*	9	Register file uncorrectable EDAC error
mem_address_not_aligned	*0x07*	10	Memory access to un-aligned address
fp_exception	*0x08*	11	FPU exception
Cp_exception	*0x09*	11	Co-processor exception
data_access_exception	*0x28*	13	Access error during load or store instruction
tag overflow	*0x0A*	14	Tagged arithmetic overflow
divide_exception	*0x2A*	15	Divide by zero
trap_instruction	*0x80 - 0xFF*	16	Software trap instruction (Ticc)

Table 4: Trap allocation and priority

The table below describes the internal registers:

Addresses of Internal Registers	Names of Internal Registers
DSU registers	
0x90080004	Processor State Register
0x9008000C	Trap Base Register
0x9008001C	DSU Trap Register
LEON2 SPARC V8 processor	
0x80000014	Cache control register
0x80000018	Power-Down register
0x80000024	LEON configuration register
AHB Debug UART	
0x800000c4	UART status register
0x800000c8	UART control register
0x800000cc	UART scaler register
FIFO Controller	
0x80050000	FIFO configuration register
0x80050004	FIFO status register
0x80050008	FIFO control register
0x80050020	FIFO tx ch control register
0x80050024	FIFO tx ch status register
0x80050028	FIFO tx ch address register
0x8005002c	FIFO tx ch size register
0x80050030	FIFO tx ch write register
0x80050034	FIFO tx ch read register
0x80050038	FIFO tx ch interrupt register
0x80050040	FIFO rx ch control register
0x80050044	FIFO rx ch status register
0x80050048	FIFO rx ch address register
0x8005004c	FIFO rx ch size register
0x80050050	FIFO rx ch write register
0x80050054	FIFO rx ch read register
0x80050058	FIFO rx ch interrupt register
0x80050060	FIFO data input register
0x80050064	FIFO data output register
0x80050068	FIFO data direction register
UoD SpaceWire link	
0x80060000	SPW Pending Irq Masked Status
0x80060008	SPW Pending Irq Status
0x80060010	SPW Irq Mask
0x80060014	SPW Link Irq Status
0x80060018	SPW Link Irq Status Set
0x8006001c	SPW Link Irq Status Clear
0x80060020	SPW CODEC Configuration
0x80060024	SPW Clock Division
0x80060028	SPW RMAP Destination Key
0x8006002c	SPW Transmit Time-Code
0x80060030	SPW VC Transfer Protocol ID
0x80060034	SPW SW Transmit Time-Code
0x80060040	SPW Status Register

Address of Internals Registers	Names of Internals Registers
0x80060044	SPW CODEC Status Register
0x80060048	SPW Receive Time-Code Status
0x80060050	SPW Transmit Time-Code Mask
0x80060080	SPW First Failing Pkt Register
0x80060100	SPW Rx Config Register [0]
0x80060104	SPW Rx Packet Counter [0]
0x80060108	SPW Rx DMA Page [0]
0x8006010c	SPW Rx DMA Base Address [0]
0x80060110	SPW Rx DMA Block Size [0]
0x80060114	SPW Rx DMA Offset [0]
0x80060118	SPW Rx Status Register [0]
0x8006011c	SPW Rx Current Pkt Status [0]
0x80060120	SPW Rx Irq Status [0]
0x80060124	SPW Rx Irq Status Set [0]
0x80060128	SPW Rx Irq Status Clear [0]
0x80060140	SPW Rx Config Register [1]
0x80060144	SPW Rx Packet Counter [1]
0x80060148	SPW Rx DMA Page [1]
0x8006014c	SPW Rx DMA Base Address [1]
0x80060150	SPW Rx DMA Block Size [1]
0x80060154	SPW Rx DMA Offset [1]
0x80060158	SPW Rx Status Register [1]
0x8006015c	SPW Rx Current Pkt Status [1]
0x80060160	SPW Rx Irq Status [1]
0x80060164	SPW Rx Irq Status Set [1]
0x80060168	SPW Rx Irq Status Clear [1]
0x80060320	SPW Tx SendList Pointer [1]
0x80060324	SPW Tx SendList Size [1]
0x80060328	SPW Tx Status [1]
0x8006032c	SPW Tx Irq Status [1]
0x80060330	SPW Tx Irq Status Set [1]
0x80060334	SPW Tx Irq Status Clear [1]
UoD SpaceWire link	
0x80070000	SPW Pending Irq Masked Status
0x80070008	SPW Pending Irq Status
0x80070010	SPW Irq Mask
0x80070014	SPW Link Irq Status
0x80070018	SPW Link Irq Status Set
0x8007001c	SPW Link Irq Status Clear
0x80070020	SPW CODEC Configuration
0x80070024	SPW Clock Division
0x80070028	SPW RMAP Destination Key
0x8007002c	SPW Transmit Time-Code
0x80070030	SPW VC Transfer Protocol ID
0x80070034	SPW SW Transmit Time-Code
0x80070040	SPW Status Register
0x80070044	SPW CODEC Status Register

Address of Internals Registers	Names of Internals Registers
0x80070048	SPW Receive Time-Code Status
0x80070050	SPW Transmit Time-Code Mask
0x80070080	SPW First Failing Pkt Register
0x80070100	SPW Rx Config Register [0]
0x80070104	SPW Rx Packet Counter [0]
0x80070108	SPW Rx DMA Page [0]
0x8007010c	SPW Rx DMA Base Address [0]
0x80070110	SPW Rx DMA Block Size [0]
0x80070114	SPW Rx DMA Offset [0]
0x80070118	SPW Rx Status Register [0]
0x8007011c	SPW Rx Current Pkt Status [0]
0x80070120	SPW Rx Irq Status [0]
0x80070124	SPW Rx Irq Status Set [0]
0x80070128	SPW Rx Irq Status Clear [0]
0x80070140	SPW Rx Config Register [1]
0x80070144	SPW Rx Packet Counter [1]
0x80070148	SPW Rx DMA Page [1]
0x8007014c	SPW Rx DMA Base Address [1]
0x80070150	SPW Rx DMA Block Size [1]
0x80070154	SPW Rx DMA Offset [1]
0x80070158	SPW Rx Status Register [1]
0x8007015c	SPW Rx Current Pkt Status [1]
0x80070160	SPW Rx Irq Status [1]
0x80070164	SPW Rx Irq Status Set [1]
0x80070168	SPW Rx Irq Status Clear [1]
0x80070320	SPW Tx SendList Pointer [1]
0x80070324	SPW Tx SendList Size [1]
0x80070328	SPW Tx Status [1]
0x8007032c	SPW Tx Irq Status [1]
0x80070330	SPW Tx Irq Status Set [1]
0x80070334	SPW Tx Irq Status Clear [1]
ESA HurriCANe CAN with DMA	
0x80080000	CAN configuration register
0x80080004	CAN status register
0x80080008	CAN control register
0x80080018	CAN sync mask filter register
0x8008001c	CAN sync code filter register
0x80080100	CAN pending irq masked status
0x80080104	CAN pending irq masked
0x80080108	CAN pending irq status
0x8008010c	CAN pending irq register
0x80080110	CAN irq mask register
0x80080114	CAN pending irq clear register
0x80080200	CAN tx channel ctrl register
0x80080204	CAN tx channel addr register
0x80080208	CAN tx channel size register
0x8008020c	CAN tx channel write register
0x80080210	CAN tx channel read register

Address of Internals Registers	Names of Internals Registers
0x80080214	CAN tx channel irq register
0x80080300	CAN rx channel ctrl register
0x80080304	CAN rx channel addr register
0x80080308	CAN rx channel size register
0x8008030c	CAN rx channel write register
0x80080310	CAN rx channel read register
0x80080314	CAN rx channel irq register
0x80080318	CAN rx channel mask register
0x8008031c	CAN rx channel code register
LEON2 Memory Controller	
0x80000000	Memory config register 1
0x80000004	Memory config register 2
0x80000008	Memory config register 3
FT AHB static ram	
0x80010000	Configuration register
GPIO with Pulses	
0x80020000	Pulse input register
0x80020004	Pulse output register
0x80020008	Pulse direction register
0x8002000c	Pulse mask register
0x80020010	Pulse polarity register
0x80020014	Pulse edge register
0x80020018	Pulse pulse register
0x8002001c	Pulse counter register
Modular Timer Unit	
0x80030000	Scaler value register
0x80030004	Scaler reload register
0x80030008	Configuration register
0x8003000c	Latch configuration register
0x80030010	Timer1 value register
0x80030014	Timer1 reload register
0x80030018	Timer1 control register
0x8003001c	Timer1 latch register
0x80030020	Timer2 value register
0x80030024	Timer2 reload register
0x80030028	Timer2 control register
0x8003002c	Timer2 latch register
ADC/DAC Interface	
0x80040000	Configuration Register
0x80040004	Status Register
0x80040010	ADC Data Input Register
0x80040014	DAC Data Output Register
0x80040020	Address Input Register
0x80040024	Address Output Register
0x80040028	Address Direction Register
0x80040030	Data Input Register
0x80040034	Data Output Register
0x80040038	Data Direction Register

Address of Internals Registers	Names of Internals Registers
LEON2 AHB Status & Failing Addr	
0x8000000c	AHB Failing Address register
0x80000010	AHB Status register
LEON2 Write Protection	
0x8000001c	Write protection register 1
0x80000020	Write protection register 2
0x800000d0	Write protect start address 1
0x800000d4	Write protect end address 1
0x800000d8	Write protect start address 2
0x800000dc	Write protect end address 2
LEON2 Timer Unit	
0x80000040	Timer 1 counter register
0x80000044	Timer 1 reload register
0x80000048	Timer 1 control register
0x8000004c	Watchdog timer register
0x80000050	Timer 2 counter register
0x80000054	Timer 2 reload register
0x80000058	Timer 2 control register
0x80000060	Scaler counter register
0x80000064	Scaler reload register
LEON2 UART	
0x80000070	UART data register
0x80000074	UART status register
0x80000078	UART control register
0x8000007c	UART scaler register
LEON2 UART	
0x80000080	UART data register
0x80000084	UART status register
0x80000088	UART control register
0x8000008c	UART scaler register
LEON2 Interrupt Ctrl	
0x80000090	Interrupt mask register
0x80000094	Interrupt pending register
0x80000098	Interrupt force register
LEON2 I/O port	
0x800000a0	I/O data register
0x800000a4	I/O direction register
0x800000a8	I/O interrupt 1 register
0x800000ac	I/O interrupt 2 register
LEON2 Secondary Interrupt Ctrl	
0x800000b0	2nd interrupt mask register
0x800000b4	2nd interrupt pending register
0x800000b8	2nd interrupt status register

Table 5: Internal Registers

6.1.2.1. LEON2 Processor

The Leon2-FT processor has been tested both in static and dynamic mode.

- In static mode the SEU sensitivity of internal registers and cache memories was investigated.
- In dynamic mode, PARANOIA and FFT test routines were used to exercise the FPU, the register file, and the Integer Unit. Each routine used LEON2 trap functions [RD2] as aid to identify particular error states.

6.1.2.1.1. Static Mode

In this mode, The LEON2-FT processor does not "work". The internal registers (213 registers) were read before the irradiation run, then these registers and also the four cache memories (instruction cache tag, instruction cache data, data cache tag, data cache data) were read at the end of the irradiation runs. Host computer software allowed to report and to analyse the error events on the internal registers and the cache memories.

The Static Mode was tested with and without the checking of the EDAC bits for registers. These EDAC bits were checked when a fetched register value was used in an instruction. The "DI" bit of "Register file protection control register", was set to disable the checking function.

A SEU was counted for the whole cache memories when the data reading, at the end of the irradiation, were different from the data before irradiation for the same address. Similarly, a SEU was counted if the value of registers present in the Table 5, had changed.

6.1.2.1.2. Dynamic Mode

The SEU32 test bench developed by Gaisler, was used for this test. The SEU32 test bench has been intended for SEU testing and monitoring of LEON2-FT processor, in order to analyse the behaviour and error rates of typical applications.
It is composed by two parts: a target application running on a LEON2-FT board and a host application running on a test host computer. The target software executed various types of applications and reported error events to the host computer. The host software could control which target application was being run and for how long. It could also collect error statistics and print out an error summary.

The LEON2-FT core contained error counters that incremented each time an error in the cache memories or register files was detected and corrected. These counters were periodically polled by the target run-time system and transmitted to the host system via the UART channel.
Anomalies such as unexpected traps or system hangs were also reported to the host system by the target run-time system, either using the UART channel or by a time-out mechanism.
Failure run was counted when the result of program was wrong. In case of FFT program a sinusoid signal is initialled, next a FFT and inverse FFT is calculated with this sinusoid signal and the resulting signal is compared with initial signal. If these signals are different the FFT program sends a failure to the host system.

Reported errors and anomalies have been classified into two categories, corrected and uncorrected. The corrected errors were formed by summing the reported error counters from the cache and register files. All other events such as checksum errors, traps or hangs are considered to be uncorrected errors since they affect the behaviour of the application.

6.1.2.2. FIFO interface

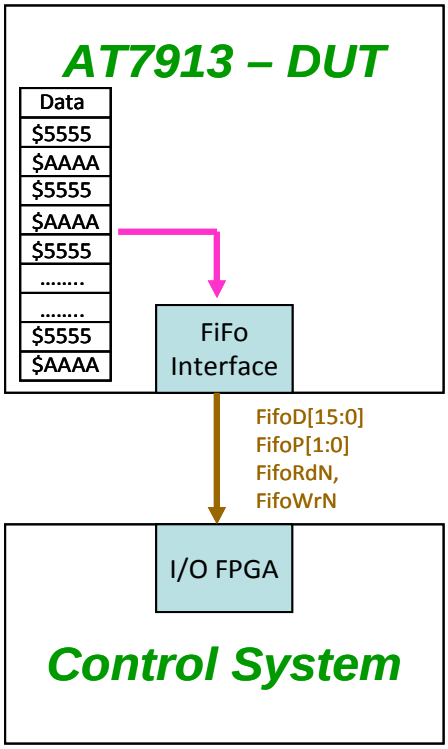


Figure 7: SEU/SEFI on FiFo Interface

Only this interface and the interruption are enabled.

The FIFO interface supports transmission and reception of blocks of data by use of circular buffers located in memory external to the core. Separate transmit and receive buffers are assumed. Reception and transmission of data can be ongoing simultaneously.

The FIFO interface was configured to write on a 16-bit memory, every 7µs on the interface and for each new writing the data bus switching between the data $AAAA and $5555 and the two FIFO parity signals were low level.
The FifoRdN signal was set to inactive level.
The inputs FifoFullN, FifoEmpN and FifoHalfN was set at high logic level, because they are inactive.

An error is detected:

· if FifoWrN signal switches to zero before or after 7µs.
· if during a writing the data bus is not equal to $AAAA or $5555 and the FIFO parity signals are at high level.
· if the FifoRdN signal switches to zero.

A SEFI is detected:

· if FifoWrN signal freezes to high level more than 100ms.
· if the system detects SET on FifoWrN continuously (more than 100ms), in case of modification of the period duration for example.
· if there are more than 50 consecutive errors on data bus or if FifoRdN freezes at low level more than 160µs.

When a SEFI is detected, AT7913 is reset to be reprogrammed. Before the reset, all internal registers are saved on the computer.

The interface software of the test bench allows the user to follow the number of SEU and SEFI, as well as the profile of detected errors, in real time during the run. At the end of each of the run, this information is saved on a computer.

6.1.2.3. 32-bit timer

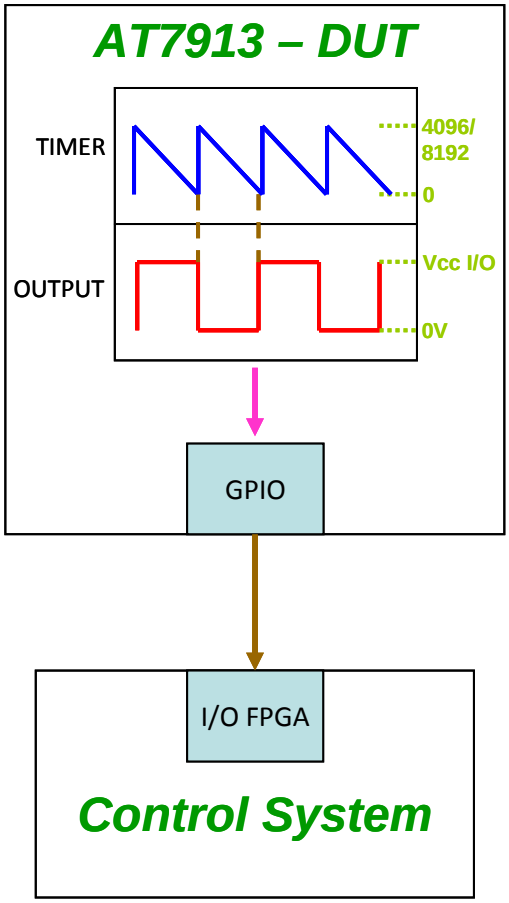


Figure 8: SEU/SEFI on Timer 32-bit

For this test, the 32-bit timers and the interruption were enabled, all other functions were disabled. Three outputs of LeonPIO were used.
In AT7913, there are four different 32-bit timers. Two of these timers were included on the Leon2-FT processor. Only one timer was enabled during the irradiation at the beginning of each run. The user can choose which one to use.

The timer value was decremented on each prescaler tick. The prescaler was clocked by the system clock and decremented on each clock cycle. When a timer underflowed, it was automatically reloaded with the value of the corresponding timer reload register.
The timer was configured to generate an interruption every 4096 clock cycles (200µs) for two timer units or every 8192 clock cycles (400µs) for two timers of the Leon2-FT processor. During this interruption, the output of the PIO was switched to opposite state. These different timer values allow to check easily and quickly, that the selected timer is tested.

The FPGA detected (every 10 ns) any change on the high and the low level of the outputs. If an error occurs on either level, the FPGA stores the event. The test bench allowed to save 500 consecutive wrong time sequences. During this time, the information on the profile of the outputs and the duration of the event are sent to the computer.

If the duration of the event is longer than 100ms, a SEFI is recorded and the AT7913 is reset to be reprogrammed. Before the reset, all internal registers are saved on the computer.

6.1.2.4. 24bits GPIO & 16bits LeonPIO

During this test, all peripherals were disabled. Only, LEON2-FT and all PIO were used and were configured to output. Two different static patterns can be applied to the GPIO (24 bits) and to the LeonPIO (16 bits) before irradiation, the 0x0000000000 pattern or the 0x111111111111 pattern.
The 0x0000000000 pattern allowed to detect a switch of direction (output to input), thanks to the pull-up resistors on the test board and an upset on the output data.
For example in Figure 9, the PIO were set to output with the 0x0000000000 pattern and Vout=0V. If the PIO switch to input then Vout=3.3V. Therefore, with the 0x111111111111 pattern the switch can't be detected because Vout will be equal to 3.3V.

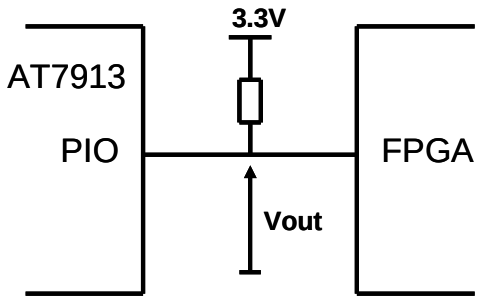


Figure 9: Link between PIO and the system of error detection

During the run, Leon2-FT is in wait state and the FPGA checked (every 10ns) the level of all the 40 bits. If an error occurs on one of the bits then an SEU is counted.

If the error persists after 100ms, a SEFI is counted. In this case, AT7913 is reset to be reprogrammed. Before the reset, all internal registers are saved on the computer.

During the test, the number of detected SEUs and SEFIs are sent continuously to the user. At the end of each run a frame of data composed by time at which the event occurred, the length of the event and the wrong data, is reported and saved on a computer.

6.1.2.5. UART serial link

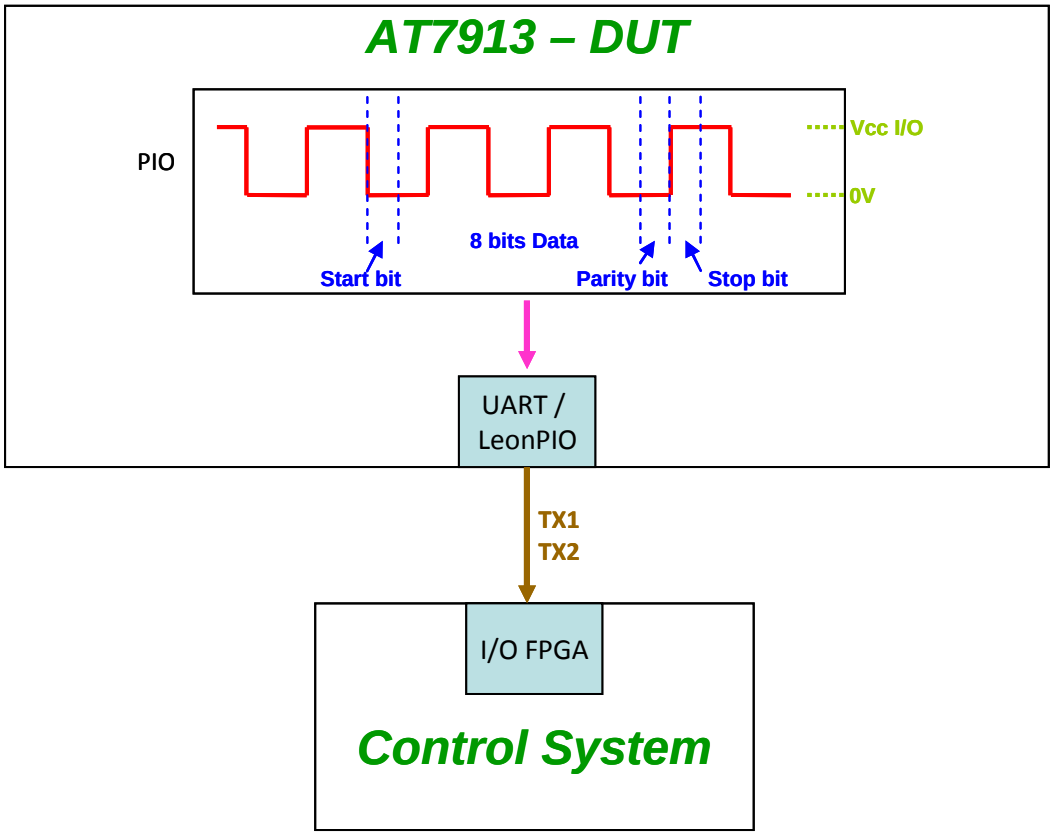


Figure 10: SEU/SEFI on UARTs

For this test, the two UART communication modules were enabled and configured with eight bits of data, one bit stop, one even parity bit and a baud rate of 38400 bauds.

The data $66 was continuously sent by the Leon2-FT to the UART modules to generate a periodic square signal on TX signals, with a duty cycle of 50% and a period of 104µs.
For that, an interrupt was generated by one of the two UART modules when the transmitter holding register moved from full to empty. During this interruption, the data $66 was sent to the transmitter holding register of the UART.

The FPGA detected (every 10 ns) all changes on high and low level of the outputs.
If an error occurs on high or low level, the FPGA stores the event. The test bench allows to save 500 successive wrong time sequences. During this time, the information on the profile of the output and the duration of the event, are sent to the computer.

If the duration of the event is longer than 100ms, a SEFI is recorded. In this case, AT7913 is reset to be reprogrammed. Before the reset, all internal registers are saved on the computer.

6.1.2.6. External memory access

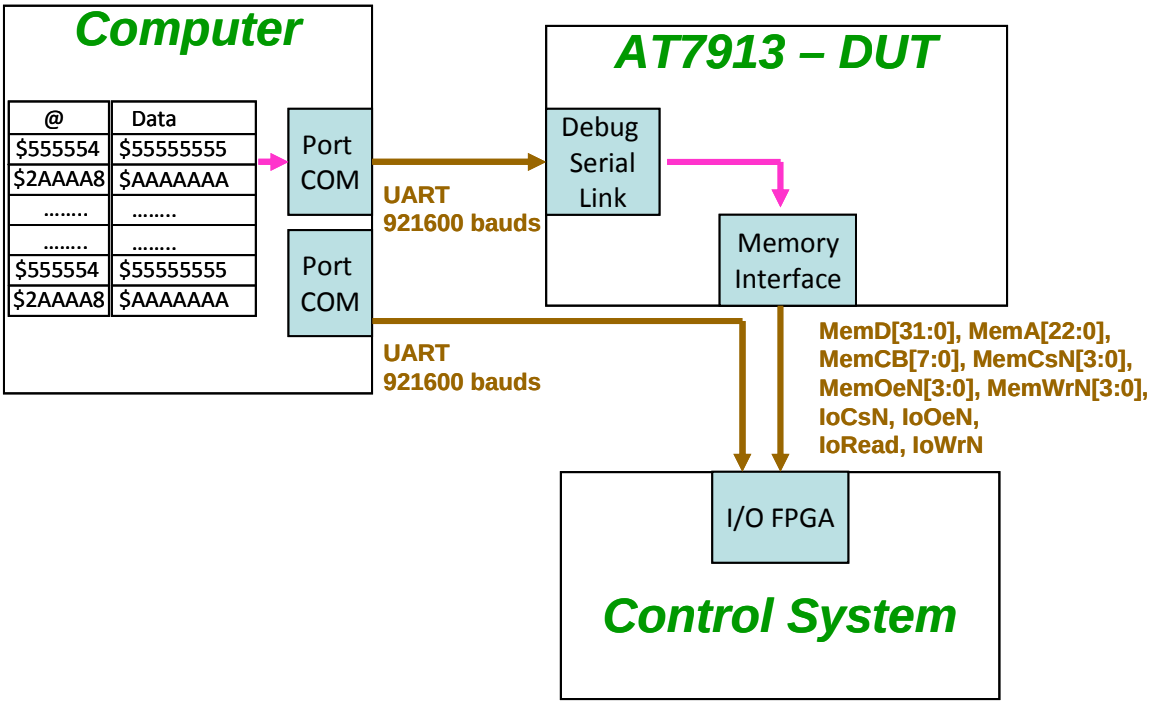


Figure 11: SEU/SEFI on External memory access

Only this interface was enabled and configured to write on a SRAM of $32*2^{21}$ bits and the address bits A0 and A1 were set to low level.
A low level on the MemWrN[3:0] outputs, provided individual write strobes for each byte lane, so the data bus MemD[31:24] was written when MemWrN[0] was active, the data bus MemD[23:16] was written when MemWrN[1] was active, etc.

During this test, the Leon was on stand-by mode. The computer sent the addresses and the data through the Debug Serial Links of AT7913 and then when MemWrN[3:0] was switched to low level, the FPGA checked the address and data buses. The computer sent consecutively the data $AAAAAAAA with the address $2AAAA8 and then the data $55555555 with the address $555554. The cycle can last several hundred milliseconds (it is around 100ms but it depends on the computer load).
The IoOeN, MemBExcN, IoCsN, RomCsN[1 :0], MemOeN[3 :0], IoBrdyN signals were set to inactive level.

When the host software sent data through the Debug Serial Link, a notification was sent (by UART) to the control system.

If MemWrN[3:0] are active before the notification, a SET is counted on MemWrN[3:0].
If MemWrN[3:0] aren't active after the notification, a SET is counted.

An SEU is recorded when the data generated by interface on MemD[31:0], MemA[22:0], MemCB[7:0], MemCsN[3:0], MemWrN[3:0], IoRead, IoWrN are wrong and when MemWrN[3:0] is not equal to $F.

A SEFI is detected:

· if MemWrN signals freeze at low level more than 100µs (the correct write strobe duration is around 20ns).

· if MemWrN signals do not enable after 10 consecutive write requests.

· if MemWrN signals are active more than 60 times after a write request, which mean the part loops (in normal condition, the MemWrN signals are active one times after a write request).

· if there is more than 10 consecutives errors on the data bus.

· if IoOeN, MemBExcN, IoCsN, RomCsN[1:0], MemOeN[3:0] are frozen at low level more than 100ms.

· if IoBrdyN are frozen at high level more than 100ms.

When a SEFI is detected, AT7913 is reset to be reprogrammed. Before the reset, all internal registers are saved on the computer.

The interface software of the test bench allows the user to follow the number of SEUs and SEFIs, as well as the profile of detected errors, in real time during the run. At the end of each run this information is saved on a computer.

6.1.2.7. ADC/DAC interface

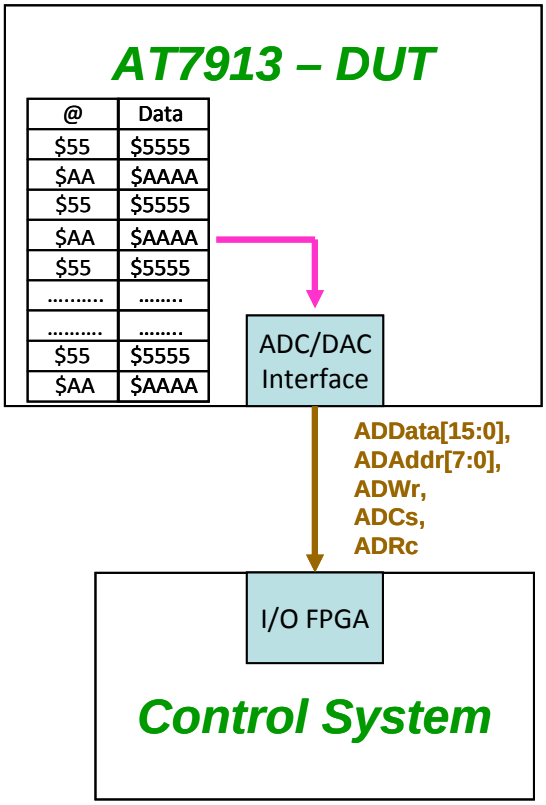


Figure 12: SEU/SEFI on ADC/DAC interface

For this test, writing on a DAC was simulated. For every writing, the 8 bits address bus and the 16 bits data bus were switched between $AAAAAA and $555555 and after an interrupt was generated to start a new write sequence. Therefore, writing on the DAC interface was performed every 6.72µs.

The ADRc and ADCs signals were set to high level.

An error is detected:

- · if ADWr signal switches to zero before or after 6.72µs.
- · If during a writing the address and data bus is not equal to $AAAAAA and $555555.
- · If the ADRc and ADCs signals switches to zero.

A SEFI is detected:

- · if ADWr signal freezes at high level more than 100ms.
- · if the system detects SETs on ADWr continuously (more than 100ms).
- · If there are more than 50 consecutive errors on the data bus.
- · If ADRc or ADCs freeze at low level for more than 160µs.

The interface software of the test bench allows the user to follow the number of SEUs and SEFIs, as well as the profile of detected errors, in real time during the run. At the end of each run this information is saved on a computer.

6.1.2.8. CAN bus interface

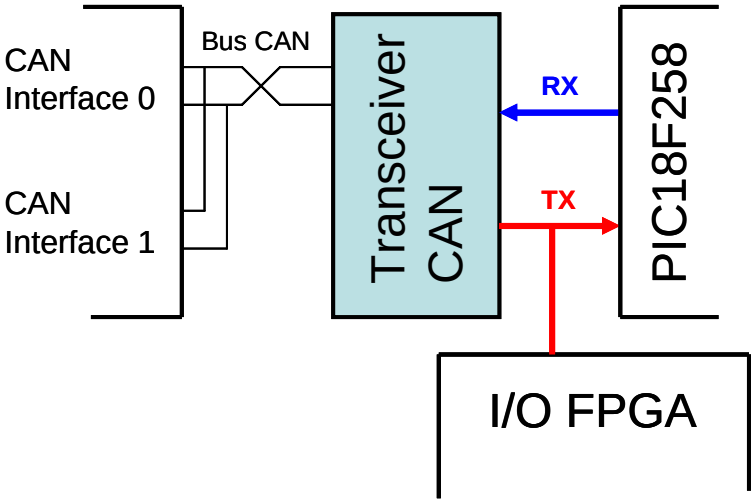


Figure 13: SEU/SEFI on CAN interface

The AT7913 used a CAN controller core and the external interface towards the CAN bus features two redundant pairs of transmission output and reception input.
The Leon2-FT processor ordered the CAN Interface to continuously transmit the same frame. Next, the PIC microcontroller with CAN Module (PIC18F258), was used to have a loopback communication with the CAN Interface, received the frame and sent automatically an acknowledge bit to indicated the right reception of the frame.
The FPGA board continually analysed data from the AT7913 and sent the detected errors to the host software.

The CAN bus is set to send a frame featuring a standard identifier and 64 data bits that is the maximum size of data in a frame, with a speed link of 1 MSPS (Mega Samples Per Seconds). The 0xAAAAAAAAAAAAAAAA pattern was used for 64 data bits.

An SEU is detected by the FPGA boards if there is an error in the frame or if the frame is too long.

If there is no data frame during more than 100 ms, a SEFI is registered.

The interface software of the test bench allows the user to follow the number of SEUs and SEFIs, as well as the profile of detected errors, in real time during the run. At the end of each run this information is saved on a computer.

6.1.2.9. On chip memory

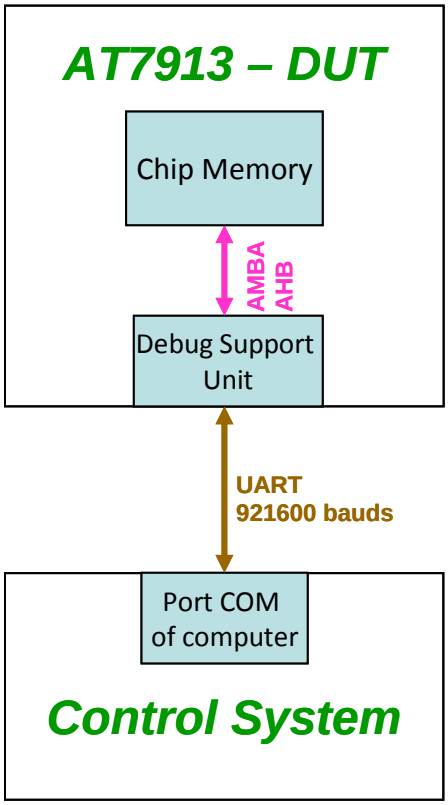


Figure 14: SEU/MBU/SEFI on chip memory

The SpaceWire-RTC device includes a fault tolerant on-chip SRAM with embedded Error Detection and Correction (EDAC) and AMBA AHB slave interface.
When EDAC is enabled write data is passed to an encoder which outputs a 7-bit checksum and the checksum is stored together with the data in memory. Thus it is possible to correct one error or to detect two errors when the data is read. This process is not visible for the user.
One error is corrected and two errors are detected, which is done by using a (32, 7) BCH code. Some of the features available are single error counter, diagnostic reads and writes and auto-scrubbing (automatic correction of single errors during reads).
The on-chip memory comprises a 32-bit wide memory bank of 64 kbytes of data.

The on-chip memory is written at the beginning and during the irradiation, it was continuously read. The cycle to read the whole memory was around two seconds and one hundred milliseconds were needed to read a word of 32 bits with the host software.
The Leon2-FT was on stand-by mode and the peripherals were disabled.
Write cycles were only applied in case of SEU or MBU identification in order to verify the ability of the memory to be written back to its initial state after an upset.
This test method was applied to verify the SEU and MBU sensitivity of the device.

SEUs and MBUs were defined by non destructive single event upset (SEU) and multiple changes of state of latched logics from one to zero or vice-versa (MBU). The logic element could be rewritten or reset. A SEFI was defined by a locked behaviour requiring a complete reset of the system. All addresses were "read and write" tested.

The On-Chip Memory was tested with and without EDAC protection. The user had the possibility to enable or to disable the EDAC protection from front of the host software.

The bit “EDAC Enable” of “Configuration register bit fields” was set to enable the EDAC protection.
The Leon2-FT processor filled all the memory with two patterns $55AA55AA or $AA55AA55 before entering in debug mode. To communicate with this memory we needed to use AHB bus, de facto we were constrained to read and write four bytes at the time. Thus, the pattern $55AA55AA was used to write $55 for even addresses and $AA for odd addresses. To write $55 for odd addresses and $AA for even addresses, the pattern $AA55AA55 was sent by the host software through the Debug Serial Link.

During the test, all addresses were checked and data were compared. When a data was wrong at first reading, a second reading was performed. If the second reading was good, the error was classified as an error of type 1. This error corresponds to an error on the access system of the memory plan. Else if the second reading was wrong the data was rewritten and a third reading was performed. If this reading was good, the error was classified as an error of type 2 which corresponds to an error on the memory plan. However if this reading was wrong, the error was classified as an error of type 3 for a “Stuck bit”. In this case the value “read” during step 3 was copied to avoid it in the next check count.
When an error was identified, the result and address were stored and the test continued to address max.
Table 6 summarises the description of events detected:

	Step 1: Read	**Step 2: Readback**	**Step 3: write**	**Step 4: Read**
No error	Good data ✓	-	-	-
ERR. Type 1	Bad data ✗	Good data ✓	-	-
ERR. Type 2	Bad data ✗	Bad data ✗	Expected data	Good data ✓
ERR. Type 3	Bad data ✗	Bad data ✗	Expected data	Bad data ✗

Table 6: Memory error type

6.1.2.10. Space Wire interface

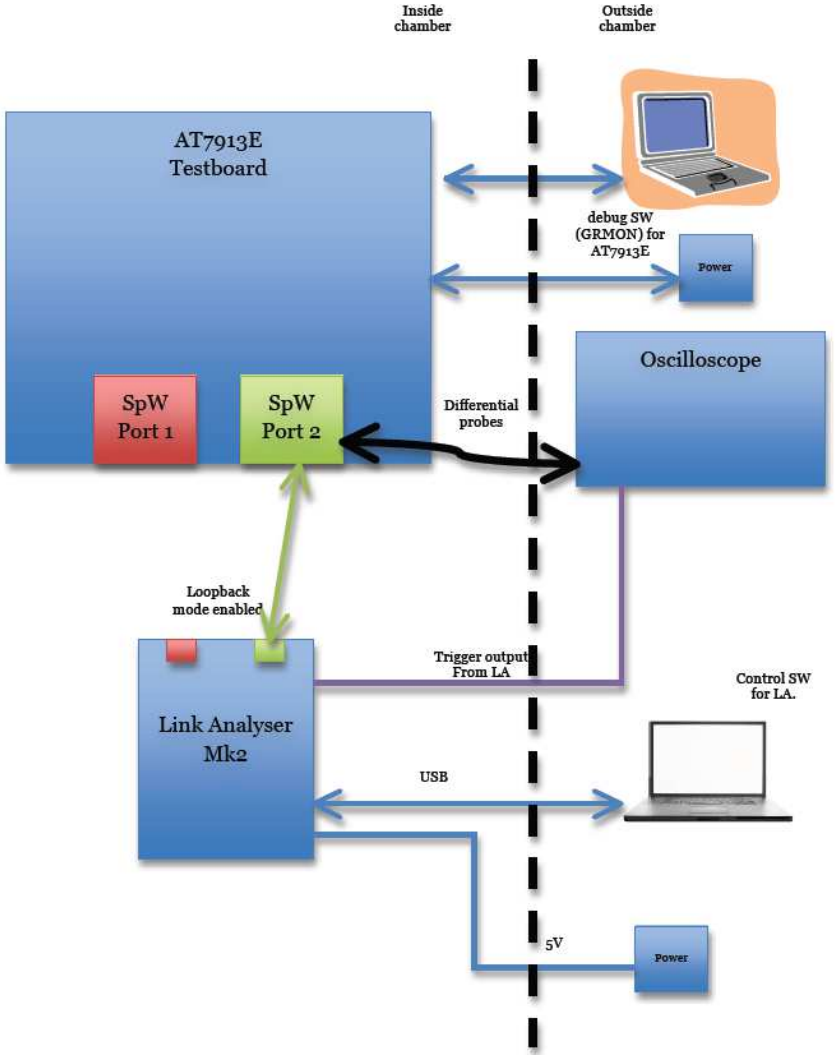


Figure 15: SEU/SET/SEFI on Space Wire Interface

SpaceWire links are point-to-point data links that connect together a SpaceWire node (e.g. instrument, processor, mass-memory unit) to another node or to a router. Information can be transferred over both directions of the link at the same time. Each link is a full-duplex, bi-directional, serial data link which can operate at data-rates of between 2 Mbits/s and 200 Mbits/s. It sends information as a serial bit stream using two signals in each direction (data and strobe). These signals are driven across the link using Low Voltage Differential Signalling (LVDS) which requires two wires for each signal.
To reduce the maximum clock to data skew requirements the clock signal is encoded into a strobe signal in such a way that XORing the data and strobe signal recovers the clock signal.

During the test, a single SPW port was active and linked in loopback mode with the Space Wire Link Analyser Mk2 of Star Dundee. The Space Wire interface was continuously sending a packet with four speed links: 10 Mbits/s, 50 Mbits/s, 100 Mbits/s and 200 Mbits/s. The packet length was one data byte for the first campaign and 64kbytes for the second campaign.

The Space Wire Link Analyser Mk2 captured characters, errors and packets from a Space Wire link. The analyser unit captured information when a pre-defined trigger condition was met with data before and after the trigger condition being recorded by Space Wire Link Analyser Mk2 software and the oscilloscope captured the waveform of data and strobe signals.

The trigger conditions should be set for all error conditions and also be configured to generate a trigger pulse on its trigger_out port connected to the trigger_in port of an oscilloscope. Therefore, when an error described in Table 7 occurs, the signals of the Space Wire link (Data and Strobes) are stored by the oscilloscope.

If any events described in Table 7 were observed, a SEU/SET was counted. If a continuous event was observed, then a SEFI was counted. A subcategory of SEFI could be discriminated when the data sending was interrupted, but the Space Wire link was still working (NULL observed). In this case a "SEFI no data" was counted.

At the end of each run, the test program read the total event counts on the oscilloscope's "Local Scope Counter" and downloaded the recorded current waveforms to store them.

Trigger Sequence Events	Description
EEP Character	An error end of packet character is received.
Character Sequence Error	This event is met when a character sequence error occurs. The error is captured when a time-code or data character is received before the first FCT character at start-up.
Escape Error	This event is met when an escape error is detected. An escape error occurs when an escape character is not followed by a data character or an FCT.
Credit Error	This event is met when a credit error occurs. A credit error occurs when more than the allowed number of FCTs are outstanding or when more data characters are transmitted than the credit allows.
Parity Error	This event is met when a parity error is detected.
Disconnect Error	This event is met when a disconnect error is detected.

Table 7: External Trigger-Out Conditions

6.1.2.11. Summary table of events detected

The next table gives an overview of all events detected for each function of the AT7913:

	SEU	SET Dynamic	SET Static	SEFI	Traps
SEU32 test bench FFT, Paranoia	Cache memories and registers	-	-	-	Detected
Static	Cache memories and registers	-	-	-	Not detected because the processor wasn't used
FIFO Interface	FifoD[15:0] FifoP[1:0]	FifoWrN	FifoRdN FifoFullN FifoEmpN FifoHalfN	All pins	Detected
32-bit Timer	-	3 outputs PIO	-	3 outputs PIO	Detected
PIO/GPIO	-	-	All outputs PIO	All outputs PIO	Detected
UART serial link	-	Two pins Tx	-	Two pins Tx	Detected
External memory access	MemA[22:0] MemD[31:0] MemCB[7:0] MemCsN[3:0] MemWrN[3:0] IoRead IoWrN	-	IoOeN MemBExcN IoCsN RomCsN[1:0] MemOeN[3:0] IoBrdyN	All pins	Not detected because the processor wasn't used
ADC/DAC interface	ADData[15:0] ADAddr[7:0]	ADWr	ADRc ADCs	All pins	Detected
CAN bus interface	CanTx	-	-	CanTx	Detected
On chip memory	Memory Test Error Type: 1, 2 or 3	-	-	-	Not detected because the processor wasn't used
Space Wire interface	SpwDOut SpwSOut	SpwDOut SpwSOut	-	SpwDOut SpwSOut	Detected

Table 8: Synthesis of events detected

6.2. Test bench description

6.2.1. Preparation of test hardware and program

TRAD developed specific test programs for each function of the AT7913. For each function tested three programs have to be coded: one for the AT7913, one for the FPGA test bench and one for the host computer. Moreover, a program for a microcontroller PIC18F258 was developed to communicate with CAN bus interface. A specific test board to make the SPWRTC board compatible with our FPGA test bench, to link with CAN interface of AT7913 and to visualize the Space Wire outputs (Data and Strobe signals) were also designed.

A Star Dundee Link Analyser Mk2 was used to monitor the Space Wire traffic and to generate an external trigger signal when an event occurs. The trigger signals were forwarded to the oscilloscope to save the events.

The test system was driven by a personal computer through a standard IEEE488 communication interface. All signals were delivered and monitored by this equipment and SEE curves were saved in its memory.
At the end of each test run, data transferred to the hard disk for storage.
An overall description of the test system is given in Figure 16.

Before performing the heavy ion test, the whole system (delidded sample, test board and software) was assembled and tested by TRAD in V.A.S.C.O (Vacuum System for Californium Operation). The results are included in the californium test report (TRAD/Calif/AT7913/XXX1/ESA/ELG/1211).

6.3. Test Bench description

The test bench consisted of, a main board (Figure 17) developed by Gaisler, two boards developed by TRAD, a FPGA board with a Xilinx FPGA Spartan3, an oscilloscope DL9240, a SpaceWire link analyser of Star Dundee and a laptop.
One of the test boards developed by TRAD (Figure 18) was used for the CAN bus testing and the other (Figure 19) was used for the Space Wire link testing.
The FPGA board was used to detect the errors and to transmit a portion of the signals of the testing function, to the oscilloscope in order to check that the DUT worked properly.
The Space Wire Link Analyser Mk2 and oscilloscope are used to detect and to store the errors on the Space Wire link.
The laptop was used to save the detected errors, but also to configure and to communicate with the oscilloscope, the Space Wire Link Analyser Mk2, the FPGA board and the the DUT through the Debug Serial Link.

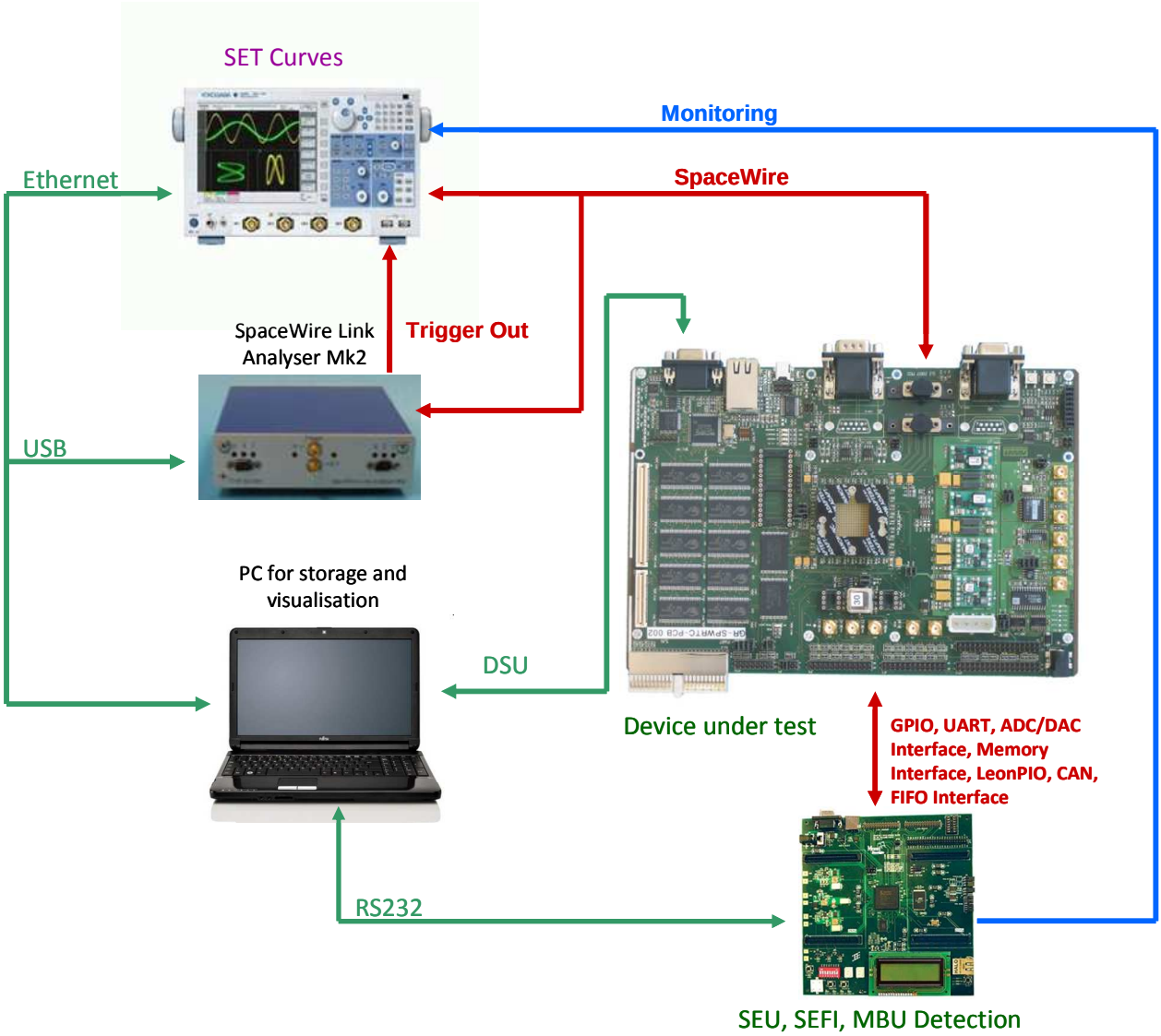


Figure 16: test system description

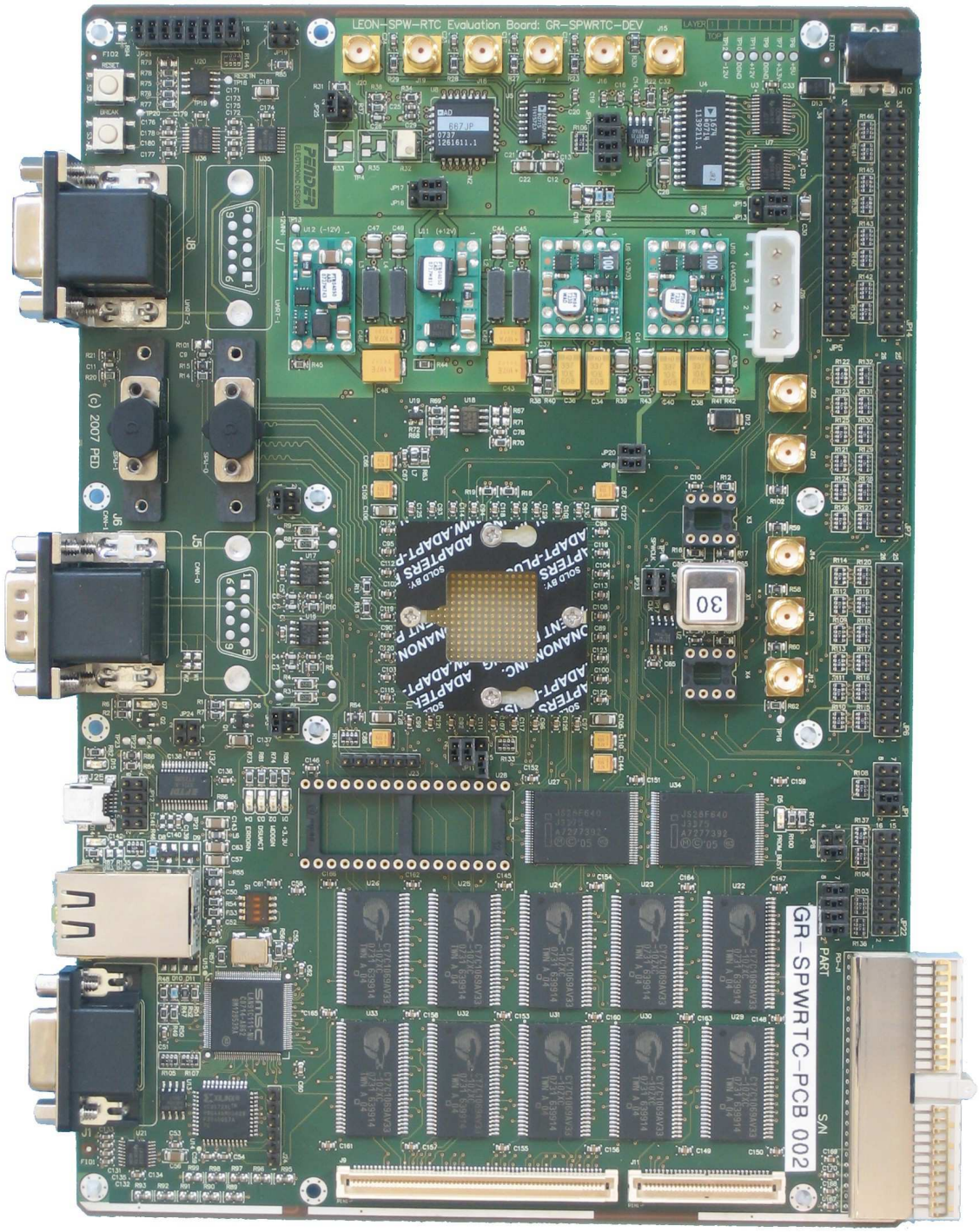


Figure 17: Main Test board developed by Gaisler, top view

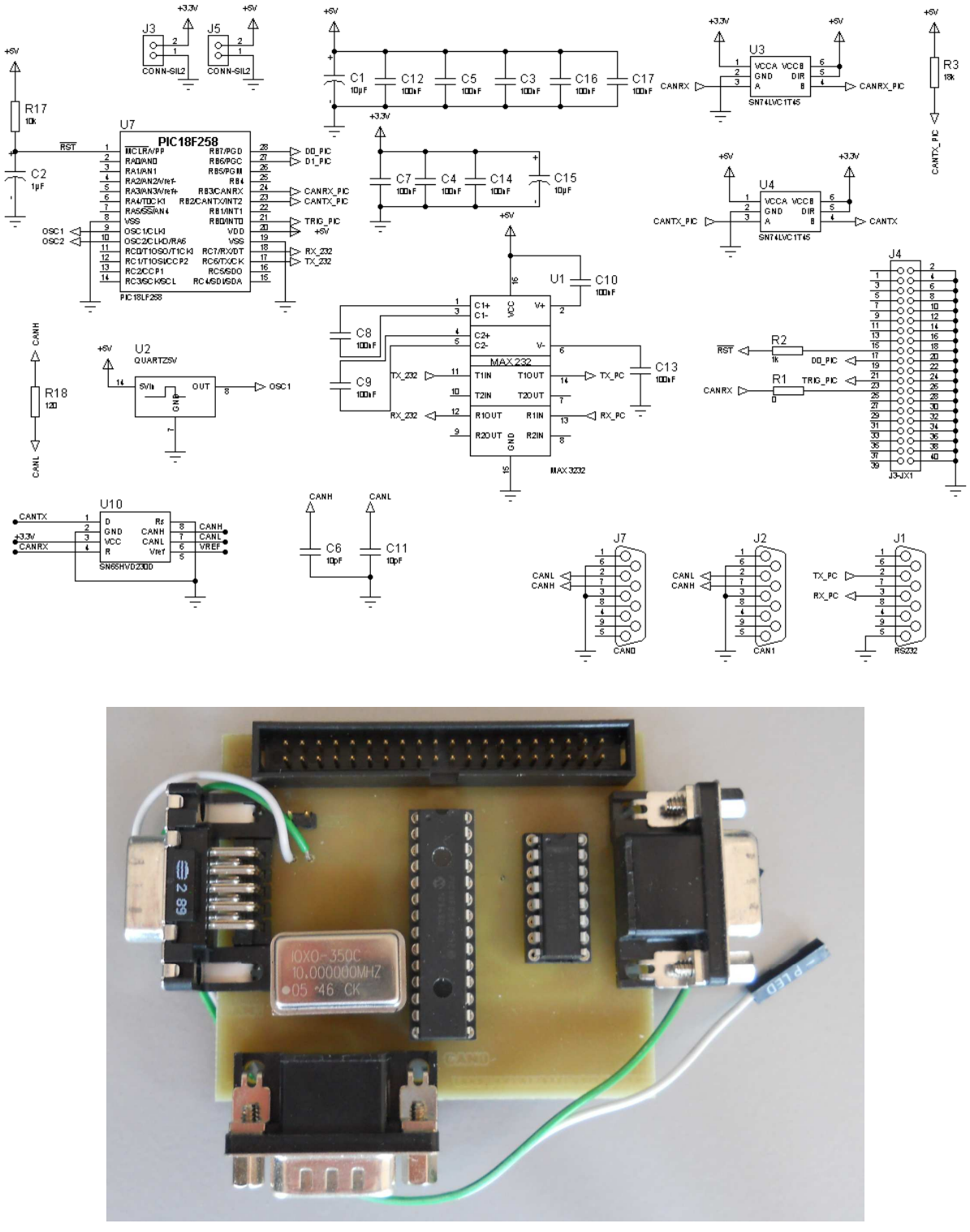
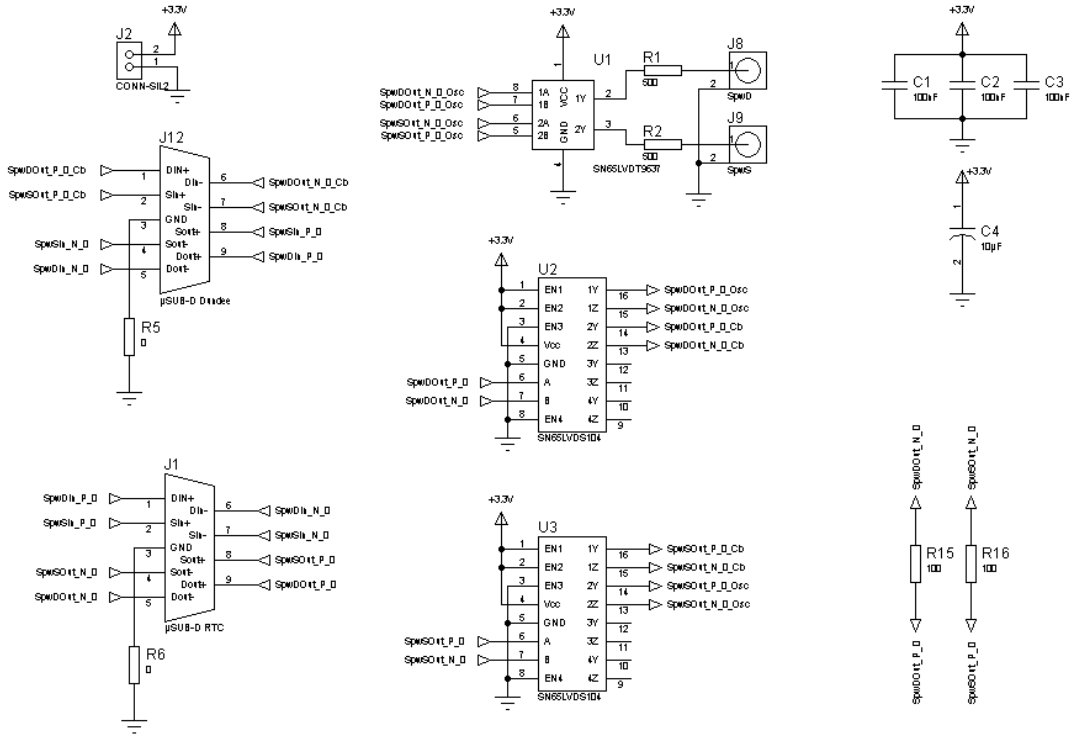


Figure 18: CAN bus Test board developed by TRAD

The board in figure 17 was connected to the CAN bus ports of the main board. This board allowed to receive the data which were sent by the AT7913 and to connect the FPGA to monitor the TX pin of the CAN bus.



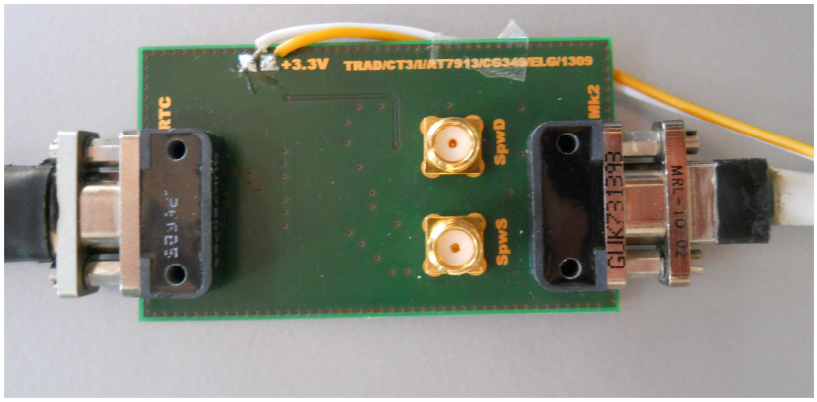


Figure 19: Space Wire Test board developed by TRAD

The board in figure 18 was connected between the main board and the Space Wire Link Analyser Mk2. This board was used to observe the transmitter signals (data and strobes) of the Space Wire link. In this board, a splitter is used to avoid degrading of these signals when the oscilloscope is connected.

6.3.1. Device Setup and Test conditions

A nominal voltage value was applied to the DUT: Vcc I/O=3.3V and Vcc Core=1.8V, a square signal of 50MHz was applied on the SysClk and another of 100MHz was applied on the SpWClk.

6.4. Test equipment identification

The tests were carried out with evaluation test boards developed by Gaisler and TRAD.

COMPUTER	PO-TE-084 PO-TE-059
REF. TEST BOARD	TRAD/CT1/I/AT7913/CG349/ELG/1309 TRAD/CT2/I/AT7913/CG349/ELG/1309 TRAD/CT3/I/AT7913/CG349/ELG/1309 TRAD/CT4/I/AT7913/CG349/ELG/1309 SPW-RTC Development Kit
EQUIPMENT	ME-71; MI-52
TEST PROGRAM	AT7913_TI_XXX1_V10.spf AT7913_TI_XXX1_V20.spf AT7913_TI_XXX1_V30.spf AT7913_TI_XXX1_V40.spf AT7913_TI_XXX1_V50.spf AT7913_TI_XXX1_V60.spf AT7913_TI_XXX1_V70.spf AT7913_TI_XXX1_V80.spf AT7913_TI_XXX1_V90.spf AT7913_TI_XXX1_V10.bit AT7913_TI_XXX1_V20.bit AT7913_TI_XXX1_V31.bit AT7913_TI_XXX1_V51.bit AT7913_TI_XXX1_V60.bit AT7913_TI_XXX1_V70.bit AT7913_TI_XXX1_V91.bit AT7913_TI_XXX1_V10.prom.bc8 AT7913_TI_XXX1_V20.prom.bc8 AT7913_TI_XXX1_V31.prom.bc8 AT7913_TI_XXX1_V50.prom.bc8 AT7913_TI_XXX1_V60.prom.bc8 AT7913_TI_XXX1_V70.prom.bc8 AT7913_TI_XXX1_V81.prom.bc8 AT7913_TI_XXX1_V90.prom.bc8 gr-spwrtc-seu32.prom.bc8

7. RESULTS

7.1. Summary of runs

The choice of the configuration tested and the fluence for each run to optimise test time, were taken with the supervision of Mr C. Poivey from ESA. Hereafter the Runs performed during this campaign are presented. The main table of runs was divided into multiple tables to allow for better visibility of the results.

AT7913													Corrected Errors												
Run	Part	Configuration	Cache Memory	Ion	Energy (MeV)	Range (µm)	LET (MeV.cm²/mg)	Flux (φ) (cm⁻².s⁻¹)	Time (s)	Run Fluence (Φ) (cm⁻²)	Run Dose (krad)	Cumulated Dose (krad)	Instruction Cache Tags Errors	Instruction Cache Datas Errors	Data Cache Tags Errors	Data Cache Datas Errors	Register File Errors	Total Errors	Cross Section (cm²)	Uncorrected Errors	Cross Section (cm²)	Traps	Cross Section (cm²)	Successful runs	Failure runs
High Range M/Q=3.3																									
1	1	Simple-Precision PARANOIA	Enabled	83 Kr 25+	756	92	32.6	6.43E+02	296	1.90E+05	0.099	0.099	20	59	23	21	0	123	6.46E-04	0	<5.25E-06	0	<5.25E-06	5562	0
2	1	Simple-Precision PARANOIA	Enabled	83 Kr 25+	756	92	32.6	5.90E+02	326	1.92E+05	0.100	0.200	20	34	27	13	0	94	4.88E-04	0	<5.20E-06	0	<5.20E-06	6066	0
3	1	Double-Precision PARANOIA	Enabled	83 Kr 25+	756	92	32.6	5.90E+02	296	1.75E+05	0.091	0.291	11	38	39	18	0	106	6.07E-04	0	<5.73E-06	0	<5.73E-06	2593	0
4	1	FFT	Enabled	83 Kr 25+	756	92	32.6	5.43E+02	304	1.65E+05	0.086	0.377	6	62	36	6	0	110	6.66E-04	0	<6.05E-06	1	6.05E-06	16627	1
5	1	FFT	Disabled	83 Kr 25+	756	92	32.6	3.36E+02	735	2.47E+05	0.129	0.506	0	0	0	0	0	0	<4.04E-06	0	<4.04E-06	0	<4.04E-06	15572	0
39	2	Simple-Precision PARANOIA	Enabled	83 Kr 25+	756	92	32.6	5.13E+02	341	1.75E+05	0.091	2.699	11	55	18	21	0	105	6.00E-04	0	<5.71E-06	0	<5.71E-06	6133	0
40	2	FFT	Enabled	83 Kr 25+	756	92	32.6	5.27E+02	335	1.77E+05	0.092	2.791	13	51	37	3	0	104	5.89E-04	0	<5.66E-06	0	<5.66E-06	17891	0
53	1	Simple-Precision PARANOIA	Enabled	58 Ni 18+	567	100	20.4	6.44E+02	345	2.22E+05	0.073	12.915	12	49	35	15	0	111	5.00E-04	0	<4.50E-06	0	<4.50E-06	6180	0
54	1	FFT	Enabled	58 Ni 18+	567	100	20.4	5.47E+02	386	2.11E+05	0.069	12.984	8	49	45	3	0	105	4.97E-04	0	<4.74E-06	0	<4.74E-06	19113	0
70	2	Simple-Precision PARANOIA	Enabled	58 Ni 18+	567	100	20.4	6.69E+02	347	2.32E+05	0.076	8.182	15	40	40	10	0	105	4.53E-04	0	<4.31E-06	0	<4.31E-06	6110	0
71	2	FFT	Enabled	58 Ni 18+	567	100	20.4	6.72E+02	305	2.05E+05	0.067	8.249	9	56	47	1	0	113	5.51E-04	0	<4.88E-06	0	<4.88E-06	16357	0
82	2	Simple-Precision PARANOIA	Enabled	22 Ne 7+	235	216	3	1.44E+03	695	1.00E+06	0.048	10.465	18	52	39	11	0	120	1.20E-04	0	<1.00E-06	0	<1.00E-06	12166	0
83	2	FFT	Enabled	22 Ne 7+	235	216	3	1.50E+03	667	1.00E+06	0.048	10.513	8	61	50	4	0	123	1.23E-04	0	<1.00E-06	0	<1.00E-06	35105	0
94	1	Simple-Precision PARANOIA	Enabled	22 Ne 7+	235	216	3	1.65E+03	307	5.06E+05	0.024	16.362	5	25	12	7	0	49	9.68E-05	0	<1.98E-06	0	<1.98E-06	5545	0
95	1	FFT	Enabled	22 Ne 7+	235	216	3	1.63E+03	615	1.00E+06	0.048	13.032	11	68	53	4	0	136	1.36E-04	0	<1.00E-06	0	<1.00E-06	32208	0
102	1	Simple-Precision PARANOIA	Enabled	40 Ar 12+	372	117	10.2	9.71E+02	409	3.97E+05	0.065	16.809	18	37	35	16	0	106	2.67E-04	0	<2.52E-06	0	<2.52E-06	7853	0
103	1	FFT	Enabled	40 Ar 12+	372	117	10.2	9.81E+02	387	3.80E+05	0.062	16.871	8	46	52	0	0	106	2.79E-04	0	<2.63E-06	0	<2.63E-06	20598	0
112	1	Simple-Precision PARANOIA	Enabled	13 C 4+	131	292	1.1	2.62E+03	382	1.00E+06	0.018	17.893	0	0	0	0	0	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06	6687	0
113	1	FFT	Enabled	13 C 4+	131	292	1.1	3.17E+03	315	1.00E+06	0.018	17.910	0	0	0	1	0	1	1.00E-06	0	<1.00E-06	0	<1.00E-06	17004	0
High Range M/Q=5																									
117	1	Simple-Precision PARANOIA	Enabled	124Xe 26+	420	37	67.7	5.73E+02	324	1.86E+05	0.201	18.164	28	68	24	18	0	138	7.44E-04	0	<5.39E-06	1	5.39E-06	6020	0
118	1	Simple-Precision PARANOIA	Enabled	124Xe 26+	420	37	67.7	3.12E+02	1609	5.01E+05	0.543	18.707	72	189	118	65	0	444	8.85E-04	0	<1.99E-06	1	1.99E-06	27591	0
119	1	FFT	Enabled	124Xe 26+	420	37	67.7	2.90E+02	1729	5.01E+05	0.543	19.250	40	252	180	30	0	502	1.00E-03	0	<2.00E-06	0	<2.00E-06	89215	2
138	2	Simple-Precision PARANOIA	Enabled	124Xe 26+	420	37	67.7	3.00E+02	404	1.21E+05	0.131	10.890	25	40	23	18	0	106	8.75E-04	0	<8.25E-06	0	<8.25E-06	7093	0
139*	2	FFT	Enabled	124Xe 26+	420	37	67.7	2.92E+02	104	3.03E+04	0.033	10.923	3	7	9	2	0	21	6.92E-04	0	<3.30E-05	0	<3.30E-05	5187	0
140	2	FFT	Enabled	124Xe 26+	420	37	67.7	2.79E+02	439	1.23E+05	0.133	11.393	12	52	43	2	0	109	8.90E-04	0	<8.16E-06	0	<8.16E-06	23039	0

Table 9: Paranoia and FFT tests results

*: This run was stopped after a problem of communication on UART 1.

AT7913													SEU								
Run	Part	Configuration	Register file SEU protection	Ion	Energy (MeV)	Range (µm)	LET (MeV.cm²/mg)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	Instruction Cache Tag	Cross Section (cm²/bit)	Instruction Cache Data	Cross Section (cm²/bit)	Data Cache Tag	Cross Section (cm²/bit)	Data Cache Data	Cross Section (cm²/bit)	Registers	Cross Section (cm²/bit)
High Range M/Q=3.3																						
6	1	Static	Enabled	83 Kr 25+	756	92	32.6	1.00E+04	100	1.00E+06	0.522	1.027	464	1.42E-08	734	2.24E-08	836	2.55E-08	695	2.12E-08	1	1.47E-10
7	1	Static	Disabled	83 Kr 25+	756	92	32.6	1.01E+04	99	1.00E+06	0.522	1.549	592	1.81E-08	728	2.22E-08	752	2.29E-08	677	2.07E-08	3	4.40E-10
41	2	Static	Enabled	83 Kr 25+	756	92	32.6	9.71E+03	103	1.00E+06	0.522	3.313	552	1.68E-08	642	1.96E-08	836	2.55E-08	682	2.08E-08	6	8.80E-10
55	1	Static	Enabled	58 Ni 18+	567	100	20.4	9.80E+03	102	1.00E+06	0.326	13.310	528	1.61E-08	557	1.70E-08	760	2.32E-08	545	1.66E-08	0	<1.47E-10
72	2	Static	Enabled	58 Ni 18+	567	100	20.4	1.02E+04	98	1.00E+06	0.326	8.575	344	1.05E-08	525	1.60E-08	668	2.04E-08	583	1.78E-08	1	1.47E-10
84	2	Static	Enabled	22 Ne 7+	235	216	3	9.90E+03	101	1.00E+06	0.048	10.561	96	2.93E-09	128	3.91E-09	212	6.47E-09	139	4.24E-09	0	<1.47E-10
92	1	Static	Enabled	22 Ne 7+	235	216	3	8.85E+03	113	1.00E+06	0.048	16.335	104	3.17E-09	122	3.72E-09	180	5.49E-09	147	4.49E-09	0	<1.47E-10
104	1	Static	Enabled	40 Ar 12+	372	117	10.2	9.80E+03	102	1.00E+06	0.163	17.034	216	6.59E-09	309	9.43E-09	424	1.29E-08	302	9.22E-09	0	<1.47E-10
114	1	Static	Enabled	13 C 4+	131	292	1.1	1.66E+03	602	1.00E+06	0.018	17.034	0	<3.05E-11	2	6.10E-11	0	<3.05E-11	2	6.10E-11	0	<1.47E-10
High Range M/Q=5																						
133	1	Static	Enabled	124Xe 26+	420	37	67.7	4.81E+03	208	1.00E+06	1.083	32.988	832	2.54E-08	1040	3.17E-08	1208	3.69E-08	976	2.98E-08	15	2.20E-09
154	2	Static	Enabled	124Xe 26+	420	37	67.7	4.83E+03	207	1.00E+06	1.083	21.478	1088	3.32E-08	1016	3.10E-08	1016	3.10E-08	986	3.01E-08	14	2.05E-09

Table 10: Static test results

AT7913															
Run	Part	Configuration	Ion	Energy (MeV)	Range (µm)	LET (MeV.cm²/mg)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	SEU	Cross Section (cm²)	SEFI	Cross Section (cm²)
High Range M/Q=3.3															
23	1	PIO - All pins to '0'	83 Kr 25+	756	92	32.6	2.05E+03	488	1.00E+06	0.522	7.300	0	<1.00E-06	0	<1.00E-06
24	1	PIO - All pins to '1'	83 Kr 25+	756	92	32.6	5.08E+03	197	1.00E+06	0.522	7.822	0	<1.00E-06	0	<1.00E-06
49	2	PIO - All pins to '0'	83 Kr 25+	756	92	32.6	4.98E+03	201	1.00E+06	0.522	6.230	0	<1.00E-06	0	<1.00E-06
High Range M/Q=5															
122	1	PIO - All pins to '0'	124Xe 26+	420	37	67.7	3.92E+03	255	1.00E+06	1.083	22.500	0	<1.00E-06	2	2.00E-06
143	2	PIO - All pins to '0'	124Xe 26+	420	37	67.7	4.81E+03	208	1.00E+06	1.083	13.559	0	<1.00E-06	3	3.00E-06

Table 11: PIO interface tests results

AT7913																			
Run	Part	Configuration	Ion	Energy (MeV)	Range (µm)	LET (MeV.cm²/mg)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	SET WrN	Cross Section (cm²)	SET Static Signals	Cross Section (cm²)	SEU	Cross Section (cm²)	SEFI	Cross Section (cm²)
High Range M/Q=3.3																			
19	1	FIFO Interface	83 Kr 25+	756	92	32.6	9.33E+02	650	6.06E+05	0.316	5.916	66	1.09E-04	0	<1.65E-06	0	<1.65E-06	1	1.65E-06
20*	1	FIFO Interface	83 Kr 25+	756	92	32.6	1.04E+03	614	6.38E+05	0.333	6.249	124	1.94E-04	0	<1.57E-06	0	<1.57E-06	1	1.57E-06
48*	2	FIFO Interface	83 Kr 25+	756	92	32.6	1.06E+03	521	5.51E+05	0.287	5.709	96	1.74E-04	0	<1.82E-06	0	<1.82E-06	1	1.82E-06
52	1	FIFO Interface	58 Ni 18+	567	100	20.4	1.92E+03	521	1.00E+06	0.326	12.843	151	1.51E-04	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06
79	2	FIFO Interface	58 Ni 18+	567	100	20.4	1.53E+03	445	6.82E+05	0.222	10.321	106	1.56E-04	0	1.06E+02	0	<1.47E-06	0	<1.47E-06
80	2	FIFO Interface	22 Ne 7+	235	216	3	2.35E+03	426	1.00E+06	0.048	10.369	35	3.50E-05	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06
98	1	FIFO Interface	22 Ne 7+	235	216	3	2.29E+03	225	5.15E+05	0.025	16.507	20	3.89E-05	0	<1.94E-06	0	<1.94E-06	0	<1.94E-06
109	1	FIFO Interface	40 Ar 12+	372	117	10.2	2.29E+03	436	1.00E+06	0.163	17.694	73	7.30E-05	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06
116	1	FIFO Interface	13 C 4+	131	292	1.1	3.19E+03	313	1.00E+06	0.018	17.875	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06
High Range M/Q=5																			
120	1	FIFO Interface	124Xe 26+	420	37	67.7	8.54E+02	1171	1.00E+06	1.083	20.333	305	3.05E-04	0	<1.00E-06	0	<1.00E-06	6	6.00E-06
141	2	FIFO Interface	124Xe 26+	420	37	67.7	7.32E+02	426	3.12E+05	0.338	11.393	103	3.30E-04	0	1.06E+02	0	<3.21E-06	1	3.21E-06

Table 12: FIFO interface tests results

▨: After a SEFI occurred, the DUT was in "undefined state" (it was not working properly), the duration of this state was not possible to estimate.

*: The run was stopped just after a SEFI was detected.

AT7913																				
Run	Part	Configuration	Ion	Energy (MeV)	Range (µm)	LET (MeV.cm²/mg)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	SET WrN	Cross Section (cm²)	SET Static Signals	Cross Section (cm²)	SEU	Cross Section (cm²)	SEFI	Cross Section (cm²)	Number of Iterration
High Range M/Q=3.3																				
12	1	External Memory	83 Kr 25+	756	92	32.6	4.93E+02	1068	5.27E+05	0.275	2.677	0	<1.90E-06	0	<1.90E-06	0	<1.90E-06	0	<1.90E-06	11643
13	1	External Memory	83 Kr 25+	756	92	32.6	1.09E+03	555	6.03E+05	0.315	2.992	0	<1.66E-06	0	<1.66E-06	0	<1.66E-06	0	<1.66E-06	43497
45	2	External Memory	83 Kr 25+	756	92	32.6	1.03E+03	973	1.00E+06	0.522	4.378	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06	1	1.00E-06	16383
58	1	External Memory	58 Ni 18+	567	100	20.4	1.01E+03	986	1.00E+06	0.326	13.972	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06	12156
75	2	External Memory	58 Ni 18+	567	100	20.4	1.18E+03	849	1.00E+06	0.326	9.236	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06	65505
93*	1	External Memory	22 Ne 7+	235	216	3	1.63E+03	37	6.03E+04	0.003	16.338	0	<1.66E-05	0	<1.66E-05	0	<1.66E-05	0	<1.66E-05	7491
High Range M/Q=5																				
132	1	External Memory	124Xe 26+	420	37	67.7	1.06E+03	946	1.00E+06	1.083	31.904	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06	10160
167	2	External Memory	124Xe 26+	420	37	67.7	1.44E+03	696	1.00E+06	1.083	28.407	0	<1.00E-06	1	1.00E-06	0	<1.00E-06	2	2.00E-06	25246

Table 13: External memory access tests results

▨: The run was stopped when the debug serial link was broken.

*: The run was cancelled because no events were detected with the Nickel ion.

AT7913																			
Run	Part	Configuration	Ion	Energy (MeV)	Range (µm)	LET (MeV.cm²/mg)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	SET WrN	Cross Section (cm²)	SET Static Signals	Cross Section (cm²)	SEU	Cross Section (cm²)	SEFI	Cross Section (cm²)
High Range M/Q=3.3																			
21*	1	ADC/DAC Interface	83 Kr 25+	756	92	32.6	9.96E+02	80	7.97E+04	0.042	6.290	9	1.13E-04	0	<1.26E-05	0	<1.26E-05	1	1.26E-05
22*	1	ADC/DAC Interface	83 Kr 25+	756	92	32.6	5.17E+02	1806	9.33E+05	0.487	6.777	163	1.75E-04	0	<1.07E-06	0	<1.07E-06	1	1.07E-06
50*	2	ADC/DAC Interface	83 Kr 25+	756	92	32.6	9.73E+02	96	9.34E+04	0.049	6.279	17	1.82E-04	0	<1.07E-05	0	<1.07E-05	1	1.07E-05
51	2	ADC/DAC Interface	83 Kr 25+	756	92	32.6	1.06E+03	941	1.00E+06	0.522	6.801	217	2.17E-04	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06
61	1	ADC/DAC Interface	58 Ni 18+	567	100	20.4	1.33E+03	753	1.00E+06	0.326	14.951	160	1.60E-04	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06
78	2	ADC/DAC Interface	58 Ni 18+	567	100	20.4	1.53E+03	421	6.42E+05	0.210	10.099	101	1.57E-04	0	<1.56E-06	0	<1.56E-06	0	<1.56E-06
81	2	ADC/DAC Interface	22 Ne 7+	235	216	3	2.49E+03	401	1.00E+06	0.048	10.417	31	3.10E-05	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06
99	1	ADC/DAC Interface	22 Ne 7+	235	216	3	2.35E+03	227	5.33E+05	0.026	16.533	22	4.13E-05	0	<1.88E-06	0	<1.88E-06	0	<1.88E-06
110	1	ADC/DAC Interface	40 Ar 12+	372	117	10.2	2.46E+03	407	1.00E+06	0.163	17.858	87	8.70E-05	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06
111	1	ADC/DAC Interface	13 C 4+	131	292	1.1	3.19E+03	313	1.00E+06	0.018	17.875	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06	0	<1.00E-06
High Range M/Q=5																			
125	1	ADC/DAC Interface	124Xe 26+	420	37	67.7	4.36E+02	1152	5.02E+05	0.544	25.210	151	3.01E-04	1	1.99E-06	0	<1.99E-06	3	5.97E-06
146	2	ADC/DAC Interface	124Xe 26+	420	37	67.7	4.85E+02	1035	5.02E+05	0.544	16.269	123	2.45E-04	0	<1.99E-06	0	<1.99E-06	0	<1.99E-06

Table 14: ADC/DAC interface tests results

*: The runs were stopped just after a SEFI was detected.

AT7913																			
Run	Part	Configuration	Ion	Energy (MeV)	Range (µm)	LET (MeV.cm²/mg)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	SET UART 1	Cross Section (cm²)	SEFI UART 1	Cross Section (cm²)	SET UART 2	Cross Section (cm²)	SEFI UART 2	Cross Section (cm²)
High Range M/Q=3.3																			
14	1	UART1&2	83 Kr 25+	756	92	32.6	6.90E+02	1449	1.00E+06	0.522	3.513	0	<0.01E-06	0	<0.01E-06	0	<0.01E-06	0	<0.01E-06
46	2	UART1&2	83 Kr 25+	756	92	32.6	1.39E+03	719	1.00E+06	0.522	4.900	1	1.00E-06	0	<0.01E-06	0	<0.01E-06	1	1.00E-06
59	1	UART1&2	58 Ni 18+	567	100	20.4	1.98E+03	504	1.00E+06	0.326	14.298	0	<0.01E-06	0	<0.01E-06	0	<0.01E-06	0	<0.01E-06
76	2	UART1&2	58 Ni 18+	567	100	20.4	2.04E+03	489	1.00E+06	0.326	9.563	1	1.00E-06	0	<0.01E-06	0	<0.01E-06	1	1.00E-06
87	2	UART1&2	22 Ne 7+	235	216	3	2.00E+03	501	1.00E+06	0.048	10.662	0	<0.01E-06	0	<0.01E-06	0	<0.01E-06	0	<0.01E-06
96	1	UART1&2	22 Ne 7+	235	216	3	1.98E+03	506	1.00E+06	0.048	16.458	0	<0.01E-06	0	<0.01E-06	0	<0.01E-06	0	<0.01E-06
107	1	UART1&2	40 Ar 12+	372	117	10.2	1.96E+03	511	1.00E+06	0.163	17.368	0	<0.01E-06	0	<0.01E-06	0	<0.01E-06	0	<0.01E-06
High Range M/Q=5																			
123	1	UART1	124Xe 26+	420	37	67.7	1.44E+03	694	1.00E+06	1.083	23.583	0	<1.00E-06	4	4.00E-06	-	-	-	-
124	1	UART2	124Xe 26+	420	37	67.7	1.21E+03	827	1.00E+06	1.083	24.666	-	-	-	-	0	<1.00E-06	0	<1.00E-06
144	2	UART1	124Xe 26+	420	37	67.7	1.26E+03	794	1.00E+06	1.083	14.643	0	<1.00E-06	2	2.00E-06	-	-	-	-
145	2	UART2	124Xe 26+	420	37	67.7	1.24E+03	804	1.00E+06	1.083	15.726	-	-	-	-	1	1.00E-06	1	1.00E-06

Table 15: UART serial link test results

AT7913															
Run	Part	Configuration	Ion	Energy (MeV)	Range (µm)	LET (MeV.cm²/mg)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	SET	Cross Section (cm²)	SEFI	Cross Section (cm²)
High Range M/Q=3.3															
15	1	Timer Int 1	83 Kr 25+	756	92	32.6	4.76E+02	2103	1.00E+06	0.522	4.035	96	9.60E-05	0	<1.00E-06
16	1	Timer Int 2	83 Kr 25+	756	92	32.6	9.98E+02	1002	1.00E+06	0.522	4.556	88	8.80E-05	0	<1.00E-06
17	1	Timer Leon 2	83 Kr 25+	756	92	32.6	6.49E+02	1541	1.00E+06	0.522	5.078	84	8.40E-05	0	<1.00E-06
18	1	Timer Leon 1	83 Kr 25+	756	92	32.6	1.55E+03	647	1.00E+06	0.522	5.600	83	8.30E-05	1	1.00E-06
47	2	Timer Int 1	83 Kr 25+	756	92	32.6	1.55E+03	647	1.00E+06	0.522	5.421	94	9.40E-05	0	<1.00E-06
60	1	Timer Int 1	58 Ni 18+	567	100	20.4	1.48E+03	674	1.00E+06	0.326	14.624	81	8.10E-05	0	<1.00E-06
77	2	Timer Int 1	58 Ni 18+	567	100	20.4	1.54E+03	650	1.00E+06	0.326	9.889	96	9.60E-05	0	<1.00E-06
88	2	Timer Int 1	22 Ne 7+	235	216	3	2.13E+03	469	1.00E+06	0.048	10.710	19	1.90E-05	0	<1.00E-06
97	1	Timer Int 1	22 Ne 7+	235	216	3	1.94E+03	263	5.10E+05	0.024	16.482	11	2.16E-05	0	<1.96E-06
108	1	Timer Int 1	40 Ar 12+	372	117	10.2	1.79E+03	560	1.00E+06	0.163	17.531	38	3.80E-05	0	<1.00E-06
115	1	Timer Int 1	13 C 4+	131	292	1.1	2.84E+03	352	1.00E+06	0.018	17.946	0	<1.00E-06	0	<1.00E-06
High Range M/Q=5															
121	1	Timer Int 1	124Xe 26+	420	37	67.7	1.20E+03	835	1.00E+06	1.083	21.417	109	1.09E-04	6	6.00E-06
142	2	Timer Int 1	124Xe 26+	420	37	67.7	1.17E+03	854	1.00E+06	1.083	12.476	144	1.44E-04	2	2.00E-06

Table 16: 32-bit timers tests results

AT7913															
Run	Part	Configuration	Ion	Energy (MeV)	Range (µm)	LET (MeV.cm²/mg)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	SEU	Cross Section (cm²)	SEFI	Cross Section (cm²)
High Range M/Q=3.3															
25	1	CAN Bus	83 Kr 25+	756	92	32.6	5.03E+03	199	1.00E+06	0.522	8.343	0	<1.00E-06	0	<1.00E-06
38	2	CAN Bus	83 Kr 25+	756	92	32.6	5.24E+03	191	1.00E+06	0.522	2.608	0	<1.00E-06	0	<1.00E-06
High Range M/Q=5															
126	1	CAN Bus	124Xe 26+	420	37	67.7	9.82E+02	1018	1.00E+06	1.083	26.293	2	2.00E-06	3	3.00E-06
147	2	CAN Bus	124Xe 26+	420	37	67.7	1.05E+03	949	1.00E+06	1.083	17.352	3	3.00E-06	0	<1.00E-06

Table 17: CAN bus test results

AT7913																			
Run	Part	Configuration	EDAC	Ion	Energy (MeV)	Range (µm)	LET (MeV.cm²/mg)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	SEU	Cross Section (cm²/bit)	MBU	Cross Section (cm²/word)	SEFI	Cross Section (cm²)	Type Errors	Number of all reading of memory
High Range M/Q=3.3																				
8	1	On-chip Memory	Enabled	83 Kr 25+	756	92	32.6	3.65E+03	274	1.00E+06	0.522	2.071	21	4.01E-11	28	1.71E-09	0	<1.00E-06	2	225
9	1	On-chip Memory	Enabled	83 Kr 25+	756	92	32.6	4.91E+02	1216	5.97E+05	0.311	2.382	2	6.39E-12	4	4.09E-10	0	<1.68E-06	2	838
10	1	On-chip Memory	Disabled	83 Kr 25+	756	92	32.6	2.57E+02	82	2.10E+04	0.011	2.393	217	1.97E-08	0	<2.90E-09	0	<4.75E-05	2	72
11	1	On-chip Memory	Disabled	83 Kr 25+	756	92	32.6	4.79E+01	367	1.76E+04	0.009	2.402	206	2.24E-08	0	<3.47E-09	0	<5.69E-05	2	262
42	2	On-chip Memory	Enabled	83 Kr 25+	756	92	32.6	5.47E+02	1829	1.00E+06	0.522	3.835	3	5.72E-12	9	5.49E-10	0	<1.00E-06	2	1206
43	2	On-chip Memory	Disabled	83 Kr 25+	756	92	32.6	1.99E+02	94	1.87E+04	0.010	3.844	228	2.32E-08	0	<3.26E-09	0	<5.34E-05	2	135
44	2	On-chip Memory	Disabled	83 Kr 25+	756	92	32.6	5.31E+01	441	2.34E+04	0.012	3.857	211	1.72E-08	0	<2.61E-09	0	<4.27E-05	2	292
56	1	On-chip Memory	Enabled	58 Ni 18+	567	100	20.4	6.78E+02	1474	1.00E+06	0.326	13.637	3	5.72E-12	2	1.22E-10	0	<1.00E-06	2	971
57	1	On-chip Memory	Disabled	58 Ni 18+	567	100	20.4	1.90E+02	136	2.59E+04	0.008	13.645	208	1.53E-08	0	<2.36E-09	0	<3.86E-05	2	127
73	2	On-chip Memory	Enabled	58 Ni 18+	567	100	20.4	6.18E+02	1619	1.00E+06	0.326	8.902	1	1.91E-12	2	1.22E-10	0	<1.00E-06	2	1087
74	2	On-chip Memory	Disabled	58 Ni 18+	567	100	20.4	1.57E+02	166	2.61E+04	0.009	8.910	209	1.53E-08	0	<2.34E-09	0	<3.83E-05	2	122
85	2	On-chip Memory	Enabled	22 Ne 7+	235	216	3	6.07E+02	1647	1.00E+06	0.048	10.609	0	<1.91E-12	0	<6.10E-11	0	<1.00E-06	2	1140
86	2	On-chip Memory	Disabled	22 Ne 7+	235	216	3	2.04E+02	507	1.03E+05	0.005	10.614	201	3.71E-09	0	<5.91E-10	0	<9.68E-06	2	350
90	1	On-chip Memory	Enabled	22 Ne 7+	235	216	3	6.55E+02	789	5.17E+05	0.025	16.281	0	<3.69E-12	0	<1.18E-10	0	<1.93E-06	2	534
91	1	On-chip Memory	Disabled	22 Ne 7+	235	216	3	2.87E+02	393	1.13E+05	0.005	16.287	214	3.61E-09	0	<5.40E-10	0	<8.85E-06	2	274
105	1	On-chip Memory	Enabled	40 Ar 12+	372	117	10.2	7.30E+02	1370	1.00E+06	0.163	17.197	0	<1.91E-12	0	<6.10E-11	0	<1.00E-06	2	916
106	1	On-chip Memory	Disabled	40 Ar 12+	372	117	10.2	3.08E+02	156	4.80E+04	0.008	17.205	211	8.39E-09	0	<1.27E-09	0	<2.08E-05	2	142
114	1	On-chip Memory	Disabled	13 C 4+	131	292	1.1	1.66E+03	602	1.00E+06	0.018	17.928	10	1.91E-11	0	<6.10E-11	0	<1.00E-06	2	409
High Range M/Q=5																				
134	1	On-chip Memory	Enabled	124Xe 26+	420	37	67.7	2.64E+02	3795	1.00E+06	1.083	34.071	3	5.72E-12	39	2.38E-09	0	<1.00E-06	One SEU: type 1 All others: type 2	2128
135*	1	On-chip Memory	Disabled	124Xe 26+	420	37	67.7	4.22E+02	716	3.02E+05	0.327	34.398	5643	3.56E-08	10	2.02E-09	0	<3.31E-06	2	379
155	2	On-chip Memory	Enabled	124Xe 26+	420	37	67.7	2.95E+02	3392	1.00E+06	1.083	22.561	2	3.81E-12	51	3.11E-09	0	<1.00E-06	2	2222
156	2	On-chip Memory	Disabled	124Xe 26+	420	37	67.7	3.68E+02	694	2.56E+05	0.277	22.838	4724	3.53E-08	11	2.63E-09	0	<3.91E-06	2	438
165	2	On-chip Memory	Enabled	84 Kr 17+	305	39	40.4	3.03E+02	3298	1.00E+06	0.646	26.677	1	1.91E-12	16	9.77E-10	0	<1.00E-06	2	2165
166	2	On-chip Memory	Disabled	84 Kr 17+	305	39	40.4	1.04E+03	964	1.00E+06	0.646	27.324	15115	2.88E-08	39	2.38E-09	0	<1.00E-06	2	594
200	1	On-chip Memory	Enabled	84 Kr 17+	305	39	40.4	3.25E+02	3075	1.00E+06	0.646	42.507	2	3.81E-12	18	1.10E-09	0	<1.00E-06	2	2020
201	1	On-chip Memory	Disabled	84 Kr 17+	305	39	40.4	7.26E+02	1377	1.00E+06	0.646	43.153	14813	2.83E-08	26	1.59E-09	0	<1.00E-06	2	851

Table 18: On-Chip Memory test results

*: During the first two hundred seconds the flux was to 200 ions.s^{-1}.cm^{-2} and no MBU was detected. Next the flux was up to 500 ions.s^{-1}.cm^{-2}.

AT7913													Error Type								
Run	Part	Configuration	Frequency (MHz)	Ion	Energy (MeV)	Range (µm)	LET (MeV.cm²/mg)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	DISCONNECT	PARITY	EOP-ESCAPE	SEU/SET Total	Cross Section (cm²)	SEFI	Cross Section (cm²)	SEFI No Data Sending	Cross Section (cm²)
High Range M/Q=3.3																					
26	1	Space Wire 0	10	83 Kr 25+	756	92	32.6	4.95E+03	202	1.00E+06	0.522	8.865	0	-	-	0	<1.00E-06	-	-	-	-
27	1	Space Wire 0	50	83 Kr 25+	756	92	32.6	5.00E+03	200	1.00E+06	0.522	9.387	2	-	-	2	2.00E-06	-	-	-	-
28	1	Space Wire 0	100	83 Kr 25+	756	92	32.6	4.90E+03	204	1.00E+06	0.522	9.908	1	-	-	1	1.00E-06	-	-	-	-
29	1	Space Wire 0	200	83 Kr 25+	756	92	32.6	4.90E+03	204	1.00E+06	0.522	10.430	0	-	-	0	<1.00E-06	-	-	-	-
30	1	Space Wire 1	200	83 Kr 25+	756	92	32.6	4.98E+03	201	1.00E+06	0.522	10.951	0	1	-	1	<1.00E-06	-	-	-	-
31	1	Space Wire 1	100	83 Kr 25+	756	92	32.6	4.93E+03	203	1.00E+06	0.522	11.473	2	-	-	2	2.00E-06	-	-	-	-
32	1	Space Wire 1	50	83 Kr 25+	756	92	32.6	5.10E+03	196	1.00E+06	0.522	11.995	0	-	-	0	<1.00E-06	-	-	-	-
33	1	Space Wire 1	10	83 Kr 25+	756	92	32.6	5.05E+03	198	1.00E+06	0.522	12.516	1	-	-	1	1.00E-06	-	-	-	-
34	2	Space Wire 1	10	83 Kr 25+	756	92	32.6	5.08E+03	197	1.00E+06	0.522	0.522	1	-	-	1	1.00E-06	-	-	-	-
35	2	Space Wire 1	50	83 Kr 25+	756	92	32.6	5.32E+03	188	1.00E+06	0.522	1.043	1	-	-	1	1.00E-06	-	-	-	-
36	2	Space Wire 1	100	83 Kr 25+	756	92	32.6	5.32E+03	188	1.00E+06	0.522	1.565	0	-	-	0	<1.00E-06	-	-	-	-
37	2	Space Wire 1	200	83 Kr 25+	756	92	32.6	5.29E+03	189	1.00E+06	0.522	2.086	1	-	-	1	1.00E-06	-	-	-	-
62	1	Space Wire 0	10	58 Ni 18+	567	100	20.4	4.95E+03	202	1.00E+06	0.326	15.277	3	-	-	3	3.00E-06	-	-	-	-
63	1	Space Wire 0	50	58 Ni 18+	567	100	20.4	4.90E+03	204	1.00E+06	0.326	15.604	0	-	-	0	<1.00E-06	-	-	-	-
64	1	Space Wire 0	100	58 Ni 18+	567	100	20.4	5.10E+03	196	1.00E+06	0.326	15.930	0	-	-	0	<1.00E-06	-	-	-	-
65	1	Space Wire 0	200	58 Ni 18+	567	100	20.4	4.98E+03	201	1.00E+06	0.326	16.256	0	-	-	0	<1.00E-06	-	-	-	-
66	2	Space Wire 0	10	58 Ni 18+	567	100	20.4	5.03E+03	199	1.00E+06	0.326	7.127	1	-	-	1	1.00E-06	-	-	-	-
67	2	Space Wire 0	50	58 Ni 18+	567	100	20.4	5.10E+03	196	1.00E+06	0.326	7.453	0	-	-	0	<1.00E-06	-	-	-	-
68	2	Space Wire 0	100	58 Ni 18+	567	100	20.4	5.05E+03	198	1.00E+06	0.326	7.780	0	-	-	0	<1.00E-06	-	-	-	-
69	2	Space Wire 0	200	58 Ni 18+	567	100	20.4	5.05E+03	198	1.00E+06	0.326	8.106	0	-	-	0	<1.00E-06	-	-	-	-
89	2	Space Wire 0	10	22 Ne 7+	235	216	3	4.95E+03	202	1.00E+06	0.048	10.758	0	-	-	0	<1.00E-06	-	-	-	-
100	1	Space Wire 0	10	22 Ne 7+	235	216	3	5.00E+03	200	1.00E+06	0.048	16.581	0	-	-	0	<1.00E-06	-	-	-	-
101	1	Space Wire 0	10	40 Ar 12+	372	117	10.2	5.29E+03	189	1.00E+06	0.163	16.744	0	-	-	0	<1.00E-06	-	-	-	-

Table 19: Space Wire interface test results in M/Q=3.3

AT7913													Error Type								
Run	Part	Configuration	Frequency (MHz)	Ion	Energy (MeV)	Range (µm)	LET (MeV.cm²/mg)	Flux (φ) ($cm^{-2}.s^{-1}$)	Time (s)	Run Fluence (Φ) (cm^{-2})	Run Dose (krad)	Cumulated Dose (krad)	DISCONNECT	PARITY	ESCAPE-EOP	SEU/SET Total	Cross Section (cm²)	SEFI	Cross Section (cm²)	SEFI No Data Sending	Cross Section (cm²)
High Range M/Q=5																					
127	1	Space Wire 0	10	124Xe 26+	420	37	67.7	1.30E+03	767	1.00E+06	1.083	27.376	7	0	0	7	7.00E-06	0	<1.00E-06	1	1.00E-06
128*	1	Space Wire 0	50	124Xe 26+	420	37	67.7	1.95E+03	513	1.00E+06	1.083	28.460	2	1	0	3	3.00E-06	0	<1.00E-06	0	<1.00E-06
129*	1	Space Wire 0	100	124Xe 26+	420	37	67.7	2.48E+03	403	1.00E+06	1.083	29.543	3	0	0	3	3.00E-06	0	<1.00E-06	1	1.00E-06
130	1	Space Wire 0	200	124Xe 26+	420	37	67.7	2.81E+03	64	1.80E+05	0.195	29.738	1	0	0	1	5.55E-06	1	5.55E-06	0	<5.55E-06
131*	1	Space Wire 0	200	124Xe 26+	420	37	67.7	2.45E+03	408	1.00E+06	1.083	30.821	3	0	0	3	3.00E-06	0	<1.00E-06	1	1.00E-06
136	1	Space Wire 0	10	84 Kr 17+	305	39	40.4	3.46E+03	289	1.00E+06	0.646	35.044	1	0	0	1	1.00E-06	0	<1.00E-06	0	<1.00E-06
137	1	Space Wire 0	50	84 Kr 17+	305	39	40.4	4.10E+03	100	4.16E+05	0.269	35.313	0	0	0	0	<2.40E-06	0	<2.40E-06	0	<2.40E-06
148	2	Space Wire 0	10	124Xe 26+	420	37	67.7	2.10E+03	218	4.58E+05	0.496	18.240	3	0	0	3	6.55E-06	0	<2.18E-06	1	2.18E-06
149	2	Space Wire 0	10	124Xe 26+	420	37	67.7	2.17E+03	166	3.61E+05	0.391	18.990	0	0	0	0	<2.77E-06	0	<2.77E-06	1	2.77E-06
150	2	Space Wire 0	50	124Xe 26+	420	37	67.7	1.97E+03	351	6.93E+05	0.751	19.574	0	1	1	2	2.89E-06	0	<1.44E-06	1	1.44E-06
151	2	Space Wire 0	100	124Xe 26+	420	37	67.7	1.48E+03	364	5.39E+05	0.584	20.004	3	2	0	5	9.28E-06	0	<1.86E-06	1	1.86E-06
152	2	Space Wire 0	200	124Xe 26+	420	37	67.7	1.29E+03	307	3.97E+05	0.430	20.395	1	0	0	1	2.52E-06	0	<2.52E-06	1	2.52E-06
153	2	Space Wire 0	200	124Xe 26+	420	37	67.7	1.32E+03	274	3.61E+05	0.391	21.478	1	1	1	3	8.32E-06	0	<2.77E-06	1	2.77E-06
157	2	Space Wire 0	10	84 Kr 17+	305	39	40.4	2.14E+03	467	1.00E+06	0.646	23.484	2	0	0	2	2.00E-06	0	<1.00E-06	0	<1.00E-06
158	2	Space Wire 0	50	84 Kr 17+	305	39	40.4	2.96E+03	174	5.15E+05	0.333	23.817	2	0	0	2	3.88E-06	0	<1.94E-06	1	1.94E-06
159	2	Space Wire 0	50	84 Kr 17+	305	39	40.4	2.50E+03	400	1.00E+06	0.646	24.464	2	0	0	2	2.00E-06	0	<1.00E-06	0	<1.00E-06
160	2	Space Wire 0	100	84 Kr 17+	305	39	40.4	2.51E+03	369	9.28E+05	0.600	25.063	1	0	0	1	1.08E-06	0	<1.08E-06	1	1.08E-06
161	2	Space Wire 0	200	84 Kr 17+	305	39	40.4	2.60E+03	83	2.16E+05	0.140	25.203	0	0	0	0	<4.63E-06	0	<4.63E-06	1	4.63E-06
162	2	Space Wire 0	200	84 Kr 17+	305	39	40.4	2.06E+03	371	7.65E+05	0.495	25.698	1	0	0	1	1.31E-06	0	<1.31E-06	0	<1.31E-06
163	2	Space Wire 0	200	84 Kr 17+	305	39	40.4	2.02E+03	153	3.09E+05	0.200	25.897	2	0	0	2	6.48E-06	0	<3.24E-06	0	<3.24E-06
164	2	Space Wire 0	100	84 Kr 17+	305	39	40.4	2.03E+03	102	2.07E+05	0.134	26.031	0	0	0	0	<4.84E-06	0	<4.84E-06	1	4.84E-06
168	2	Space Wire 0	10	124Xe 26+	420	37	67.7	1.31E+03	141	1.85E+05	0.200	28.607	1	0	0	1	5.41E-06	0	<5.41E-06	1	5.41E-06
169	2	Space Wire 0	10	124Xe 26+	420	37	67.7	1.06E+03	383	4.06E+05	0.439	29.046	1	0	0	1	2.47E-06	0	<2.47E-06	1	2.47E-06
170	2	Space Wire 0	10	124Xe 26+	420	37	67.7	1.07E+03	146	1.56E+05	0.169	29.215	2	0	0	2	1.28E-05	0	<6.42E-06	1	6.42E-06
171	2	Space Wire 0	10	124Xe 26+	420	37	67.7	1.06E+03	526	5.55E+05	0.601	29.816	0	0	0	0	<1.80E-06	0	<1.80E-06	0	<1.80E-06
172	2	Space Wire 0	50	124Xe 26+	420	37	67.7	1.30E+03	588	7.66E+05	0.830	30.646	1	0	0	1	1.31E-06	0	<1.31E-06	0	<1.31E-06
173	2	Space Wire 0	50	124Xe 26+	420	37	67.7	1.68E+03	182	3.06E+05	0.331	30.977	1	1	0	2	6.55E-06	0	<3.27E-06	0	<3.27E-06
174	2	Space Wire 0	100	124Xe 26+	420	37	67.7	1.62E+03	39	6.33E+04	0.069	31.045	2	0	0	2	3.16E-05	0	<1.58E-05	1	1.58E-05
175	2	Space Wire 0	100	124Xe 26+	420	37	67.7	1.65E+03	287	4.73E+05	0.512	31.557	2	0	1	3	6.35E-06	0	<2.12E-06	1	2.12E-06
176	2	Space Wire 0	100	124Xe 26+	420	37	67.7	1.63E+03	253	4.12E+05	0.446	32.003	1	0	0	1	2.43E-06	0	<2.43E-06	1	2.43E-06
177	2	Space Wire 0	100	124Xe 26+	420	37	67.7	1.62E+03	69	1.12E+05	0.121	32.124	0	0	1	1	8.94E-06	0	<8.94E-06	1	8.94E-06
178	2	Space Wire 0	100	124Xe 26+	420	37	67.7	1.64E+03	94	1.54E+05	0.167	32.291	2	0	0	2	1.30E-05	0	<6.49E-06	0	<6.49E-06
179	2	Space Wire 0	200	124Xe 26+	420	37	67.7	1.66E+03	49	8.12E+04	0.088	32.379	0	0	0	0	<1.23E-05	0	<1.23E-05	1	1.23E-05
180	2	Space Wire 0	200	124Xe 26+	420	37	67.7	1.66E+03	67	1.11E+05	0.121	32.500	0	0	0	0	<8.98E-06	0	<8.98E-06	1	8.98E-06
181	2	Space Wire 0	200	124Xe 26+	420	37	67.7	1.67E+03	88	1.47E+05	0.159	32.659	1	0	0	1	6.81E-06	0	<6.81E-06	1	6.81E-06
182	2	Space Wire 0	200	124Xe 26+	420	37	67.7	1.30E+03	424	5.51E+05	0.597	33.256	2	0	0	2	3.63E-06	0	<1.81E-06	1	1.81E-06
183	2	Space Wire 0	200	124Xe 26+	420	37	67.7	1.31E+03	232	3.05E+05	0.330	33.586	0	3	0	3	9.85E-06	0	<3.28E-06	0	<3.28E-06
184	1	Space Wire 0	50	124Xe 26+	420	37	67.7	1.34E+03	746	1.00E+06	1.083	36.397	3	0	0	3	3.00E-06	0	<1.00E-06	0	<1.00E-06
185	1	Space Wire 0	100	124Xe 26+	420	37	67.7	1.37E+03	154	2.11E+05	0.228	36.625	1	0	0	1	4.74E-06	0	<4.74E-06	1	4.74E-06
186	1	Space Wire 0	100	124Xe 26+	420	37	67.7	1.32E+03	759	1.00E+06	1.086	37.711	3	0	0	3	2.99E-06	0	<9.98E-07	0	<9.98E-07
187	1	Space Wire 0	200	124Xe 26+	420	37	67.7	1.34E+03	192	2.58E+05	0.279	37.990	1	0	0	1	3.88E-06	0	<3.88E-06	1	3.88E-06
188	1	Space Wire 0	200	124Xe 26+	420	37	67.7	1.40E+03	79	1.10E+05	0.120	38.110	0	0	0	0	<9.06E-06	0	<9.06E-06	1	9.06E-06
189	1	Space Wire 0	200	124Xe 26+	420	37	67.7	1.30E+03	161	2.09E+05	0.226	38.336	0	0	0	0	<4.79E-06	0	<4.79E-06	1	4.79E-06
190	1	Space Wire 0	200	124Xe 26+	420	37	67.7	1.25E+03	166	2.07E+05	0.224	38.560	0	0	0	0	<4.83E-06	0	<4.83E-06	1	4.83E-06
191	1	Space Wire 0	200	124Xe 26+	420	37	67.7	1.37E+03	262	3.60E+05	0.390	38.950	1	0	0	1	2.78E-06	0	<2.78E-06	1	2.78E-06
192	1	Space Wire 0	200	124Xe 26+	420	37	67.7	1.38E+03	68	9.35E+04	0.101	39.052	0	0	0	0	<1.07E-05	0	<1.07E-05	0	<1.07E-05
193	1	Space Wire 0	200	84 Kr 17+	305	39	40.4	1.50E+03	666	1.00E+06	0.646	39.698	0	0	0	0	<1.00E-06	0	<1.00E-06	1	1.00E-06
194	1	Space Wire 0	100	84 Kr 17+	305	39	40.4	2.00E+03	501	1.00E+06	0.646	40.345	0	1	0	1	1.00E-06	0	<1.00E-06	0	<1.00E-06
195	1	Space Wire 0	50	84 Kr 17+	305	39	40.4	2.22E+03	59	1.31E+05	0.085	40.429	0	1	0	1	7.65E-06	0	<7.65E-06	1	7.65E-06
196	1	Space Wire 0	50	84 Kr 17+	305	39	40.4	2.01E+03	369	7.40E+05	0.478	40.907	1	0	0	1	1.35E-06	0	<1.35E-06	1	1.35E-06
197	1	Space Wire 0	50	84 Kr 17+	305	39	40.4	2.05E+03	197	4.05E+05	0.262	41.169	1	0	0	1	2.47E-06	0	<2.47E-06	0	<2.47E-06
198	1	Space Wire 0	10	84 Kr 17+	305	39	40.4	2.40E+03	29	6.96E+04	0.045	41.214	0	0	0	0	<1.44E-05	0	<1.44E-05	1	1.44E-05
199	1	Space Wire 0	10	84 Kr 17+	305	39	40.4	2.04E+03	490	1.00E+06	0.646	41.860	1	1	0	2	2.00E-06	0	<1.00E-06	0	<1.00E-06

Table 20: Space Wire interface test results in M/Q=5

: The run was stopped because the system continuously detected “PARITY ERROR”.

: The run was stopped because there was a problem with Mk2 Link Analyser.

: The part sent a frame consisted of data byte.

*: Don’t take these runs for the cross-section because it’s not certain that the part sent the data at the end of run.

The test results are described hereunder.

7.2. AT7913 test results

7.2.1. Simple-Precision PARANOIA SEE tests results

The details of all irradiation runs for this test are shown in Table 9.

During the experiment, it was noted that the DUT showed the same sensibility with the simple and double precision, so it was decided to focus our experimentation on the simple precision paranoia program.

SEUs were observed during the irradiation down to the Neon Heavy Ion (LET = 3 MeV.cm²/mg).

Traps were observed on part 1 during the irradiation to the Xenon Heavy Ion (LET = 67.7 MeV.cm²/mg).

All errors were corrected and all runs were successful.

7.2.1.1. Simple-Precision PARANOIA - Corrected Error Cross sections

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²)	
	N° 1	N° 2
67.7	8.85E-04	8.75E-04
32.6	6.46E-04	6.00E-04
20.4	5.00E-04	4.53E-04
10.2	2.67E-04	-
3	9.68E-05	1.20E-04
1.1	<1.00E-06	-

Table 21: Simple-Precision PARANOIA - SEU Corrected Error cross section results

The following figure presents the cross section of corrected errors by the AT7913 on the instruction cache memory (data and tag), the data cache memory (data and tag) and the total number of registers.
Points represented by an arrow pointing down indicate that no events were observed at the corresponding LET.
The evaluated cross section is then lower than 1E-6 cm^2, value corresponding to one event at maximum fluence.

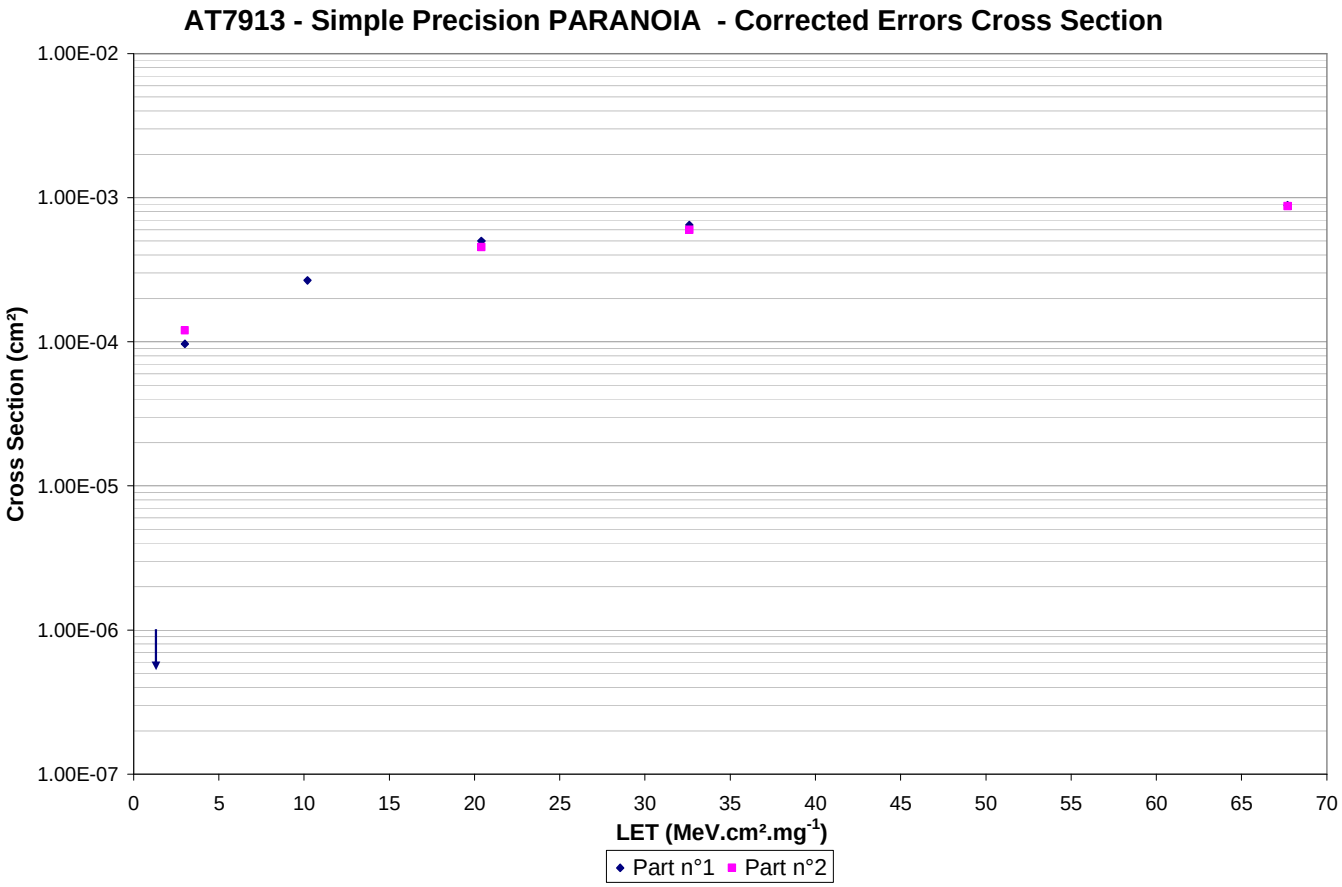


Figure 20: Simple-Precision PARANOIA - SEU Corrected Errors cross section curve for AT7913

7.2.2. FFT SEE tests results

SEUs were observed during the irradiation down to the Neon Heavy Ion (LET = 3 MeV.cm²/mg).

One failure was detected due to a trap during run number 4 with cache memories enabled. Two failures of program iteration runs were during run number 119 but no trap and no uncorrected error were detected that could have produced these failures. It is possible that these were due to SEU in memory map where the sinusoid signals were stored.

No uncorrected error was detected for this test with or without cache memories.

The run number 139 was aborted because the UART communication was stopped. The normal operation was recovered with a reset after the SEFI.

7.2.2.1. FFT - Corrected Errors Cross sections

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²)	
	N° 1	N° 2
67.7	1.00E-03	8.90E-04
32.6	6.66E-04	5.89E-04
20.4	4.97E-04	5.51E-04
10.2	2.79E-04	-
3	1.36E-04	1.23E-04
1.1	<1.00E-06	-

Table 22: FFT - SEU Corrected Errors cross section results

The following figure presents the cross section of corrected errors by the AT7913 on the instruction cache memory, the data cache memory and the registers.
Points represented by an arrow pointing down indicate that no events were observed at the corresponding LET.
The evaluated cross section is then lower than 1E-6 cm^2, value corresponding to one event at maximum fluence.

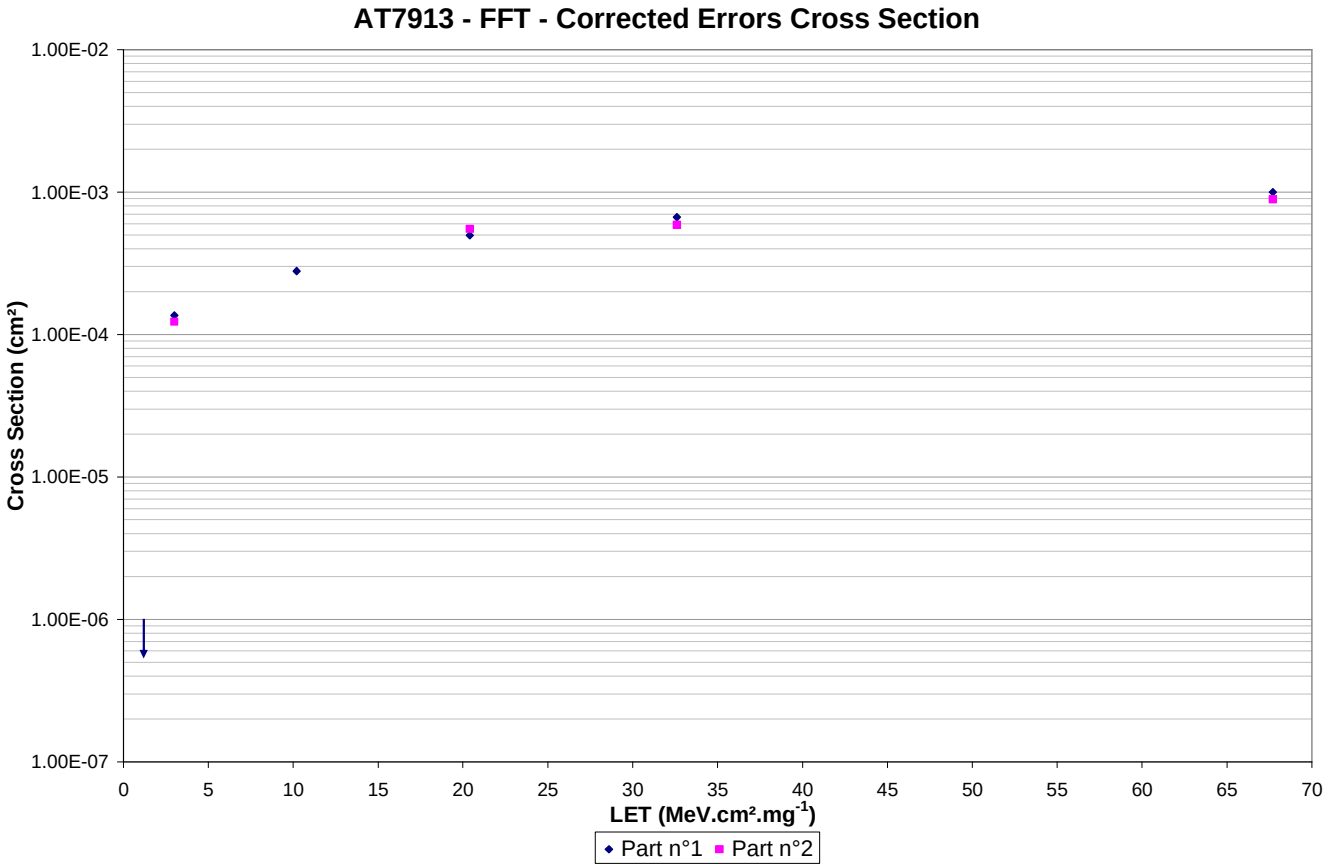


Figure 21: FFT - SEU Corrected Errors cross section curve for AT7913

7.2.3. Static Mode SEE tests results

The details of all runs for this test are shown in Table 10.

This test was performed without SEU protection for the registers, except for the run 7. Each word of the main register file is protected using a 7-bit EDAC checksum. Checking of the EDAC bits is done every time a fetched register value is used in an instruction. Like in our case any instructions were used the SEU protection was not effective. Therefore the SEU protection activation does not have any impact on the SEU registers sensibility.

The cross section was estimated for the registers and cache memories (instruction cache tag, instruction cache data, data cache tag, and data cache data). SEU cross sections of all cache memories are similar.

SEUs for the cache tag memories, were observed during the irradiation down to the Neon Heavy Ion (LET= 3 MeV.cm²/mg).
SEUs for the cache data memories, were observed during the irradiation down to the Carbon Ion (LET= 1.1 MeV.cm²/mg).
SEUs for the registers, were observed during the irradiation down to the Nickel Ion (LET= 20.4 MeV.cm²/mg).

The register cross sections were calculated per bit with 213 registers of 32 bits.
The cross sections for the cache memories were calculated per bit with the memory of 4096 bytes.

7.2.3.1. Static Mode - Instruction Cache - SEU Cross sections

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²/bit)	
	N° 1	N° 2
67.7	2.20E-9	2.05E-9
32.6	4.40E-10	8.80E-10
20.4	<1.47E-10	1.47E-10
10.2	<1.47E-10	-
3	<1.47E-10	<1.47E-10
1.1	<1.47E-10	-

Table 23: Static Mode - Registers - SEU cross section results

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²/bit)	
	N° 1	N° 2
67.7	2.54E-08	3.32E-08
32.6	1.42E-08	1.68E-08
20.4	1.61E-08	1.05E-08
10.2	6.59E-09	-
3	3.17E-09	2.93E-09
1.1	<3.05E-11	-

Table 24: Static Mode - Instruction Cache Tag - SEU cross section results

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²/bit)	
	N° 1	N° 2
67.7	3.17E-08	3.10E-08
32.6	2.24E-08	2.22E-08
20.4	1.70E-08	1.60E-08
10.2	9.43E-09	-
3	3.72E-09	3.91E-09
1.1	6.10E-11	-

Table 25: Static Mode - Instruction Cache Data - SEU cross section results

The events at Carbon Ion have been identified during the run of the on-chip memory (run n°114),
To directly access to the on-chip memory, the DSU interface was used and so, the Leon2-FT was in stand by mode. At the beginning of the test the register and the cache memories were systematically initialised and at the end of the run, they were systematically checked and logged.

The following figure presents the cross section of uncorrected errors by the AT7913 on the instruction cache tag memory and the instruction cache data memory.
Points represented by an arrow pointing down indicate that no events were observed at the corresponding LET.
The evaluated cross section is then lower than 3.05E-11 cm^2, value corresponding to one event at maximum fluence.

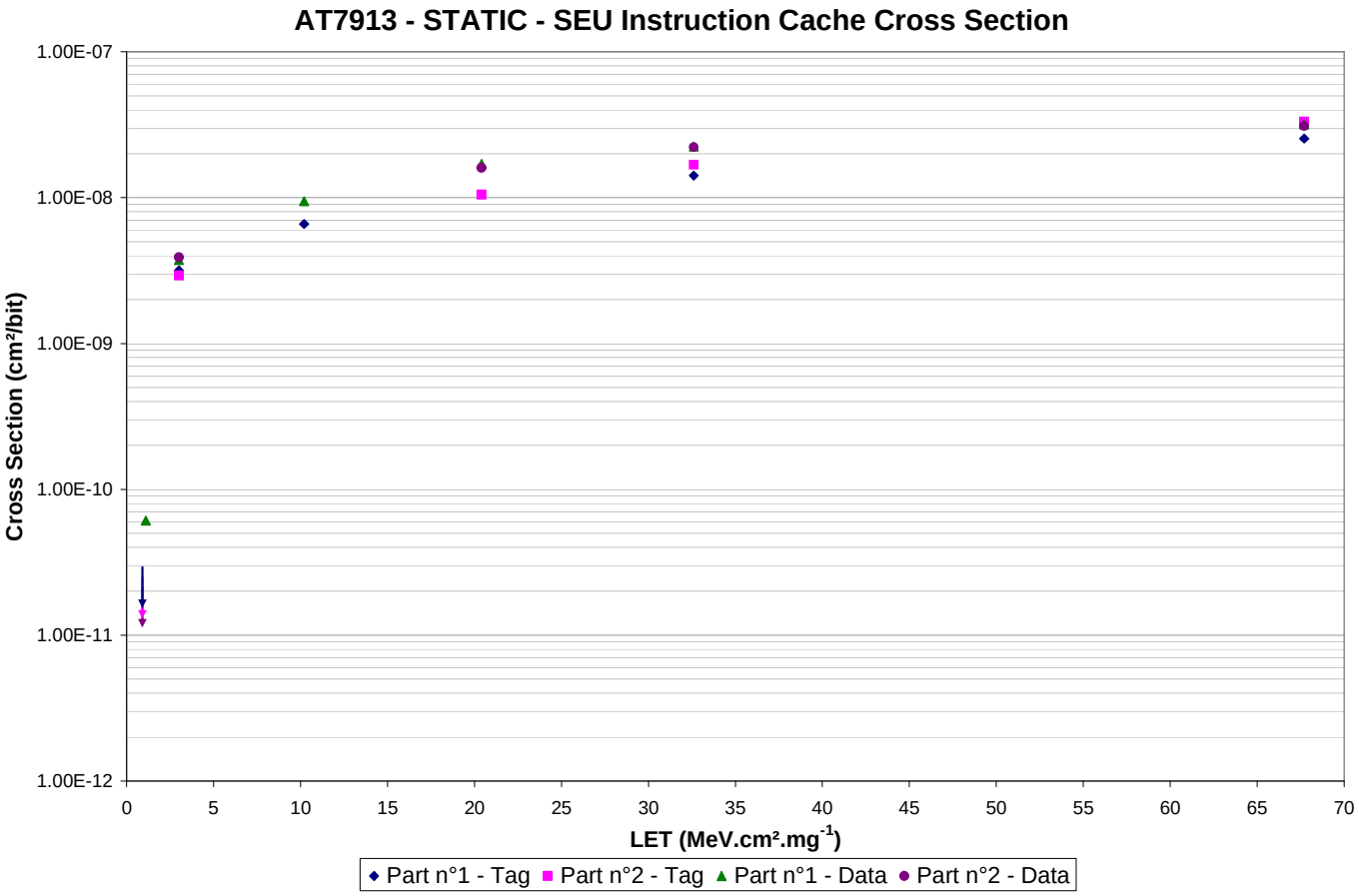


Figure 22: Static Mode - Instruction Cache - SEU cross section curve for AT7913

7.2.3.2. Static Mode - Data Cache - SEU Cross sections

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²/bit)	
	N° 1	N° 2
67.7	3.69E-08	3.10E-08
32.6	2.55E-08	2.55E-08
20.4	2.32E-08	2.04E-08
10.2	1.29E-08	-
3	5.49E-09	6.47E-09
1.1	<3.05E-11	-

Table 26: Static Mode - Data Cache Tag - SEU cross section results

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²/bit)	
	N° 1	N° 2
67.7	2.98E-08	3.01E-08
32.6	2.12E-08	2.08E-08
20.4	1.66E-08	1.78E-08
10.2	9.22E-09	-
3	4.49E-09	4.24E-09
1.1	6.10E-11	-

Table 27: Static Mode - Data Cache Data - SEU cross section results

The following figure presents the cross section of uncorrected errors by the AT7913 on the instruction cache tag memory and the instruction cache data memory.
Points represented by an arrow pointing down indicate that no events were observed at the corresponding LET.
The evaluated cross section is then lower than 3.05E-11 cm^2, value corresponding to one event at maximum fluence.

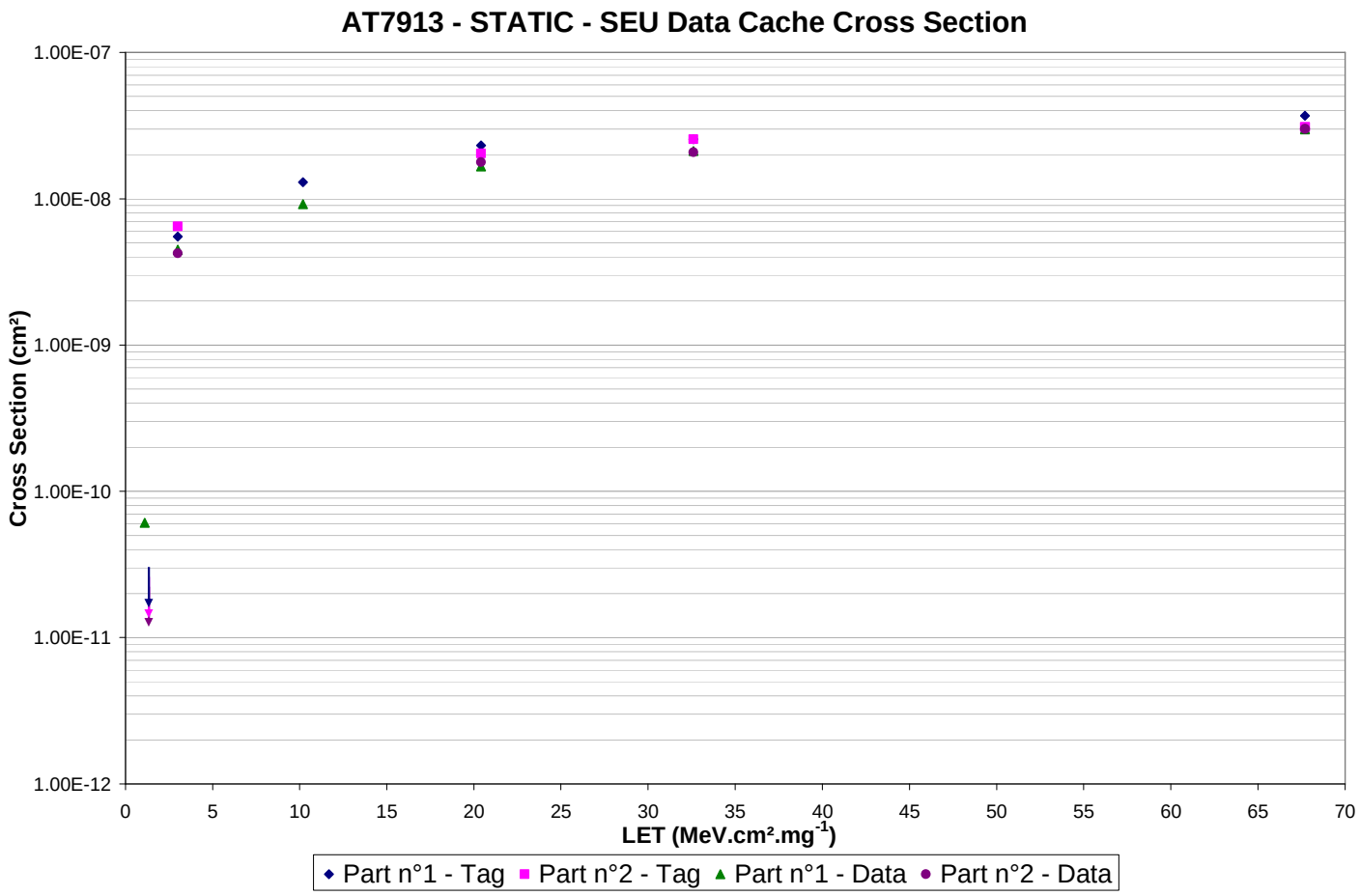


Figure 23: Static Mode - Data Cache - SEU cross section curve for AT7913

7.2.4. FIFO Interface SEE tests results

The details of all runs for this test are showed in Table 12.

No events were detected on the data bus and the FifoRdN signal, during this test under Krypton irradiation with a total fluence equal to 1E+6 ions/cm^2 (LET = 32.4 MeV.cm²/mg and range = 92µm).

In contrast, events were observed on the FifoWrN signal. Most events were due to a time lag of the writing request, certainly because of the processor. But all writing requests were transferred and there never was any change on the pulse width of FifoWrN.

Due to a failure of the test bench during the first campaign, the SEFI detection was performed by a manual system based on the monitoring of signals FifoWrN and FIFO_DATA_0.
When the signals froze on the scope, the run was stopped.
The problem has been detected during run n°19, therefore this run wasn't directly stopped.

The part was configured to move into debug mode when the processor entered an error condition. Every time a SEFI was detected for the first campaign, the bit "Error mode" of "DSU trap register" was set, because a trap caused the processor to enter error mode. Therefore, the SEFIs were due to a trap, the code SPARC trap types (of tbr register) are the following:

- Run n°19: Trap 0x02 "illegal instruction" was detected.
- Run n°20: Trap 0x03 "privileged instruction" was detected.
- Run n°48: Trap 0x2B "write buffer error" was detected.

For the second campaign the test bench was modified to generate a reset after a SEFI, thus the runs weren't aborted after SEFI and that there has been more than one SEFI which was detected. The normal operation was recovered with a reset after the SEFI.

For the run number 120 six SEFIs were detected but according to the registers, only three were due to traps and concerning the others no traps occurred and no FIFO configuration registers were changed. For the run number 141 the SEFI was due to a trap. The code SPARC trap types (of tbr register) are the following:

- Run n°120: Traps 0x02 "illegal instruction", 0x09 "Co-processor exception", 0x0B "watchpoint detected" were detected.
- Run n°141: Trap 0X07 "Memory access to un-aligned address" was detected.

SETs on FifoWrN signal, were observed during the irradiation down to the Neon Ion (LET = 3 MeV.cm²/mg).

7.2.4.1. FIFO Interface SET Cross sections

LET Eff (MeV.cm².mg^{-1})	SET Cross Section (cm²)	
	N° 1	N° 2
67.7	3.05E-04	3.30E-04
32.6	1.94E-04	1.74E-04
20.4	1.51E-04	1.56E-04
10.2	7.30E-05	-
3	7.30E-05	7.30E-05
1.1	<1.00E-06	-

Table 28: FIFO Interface SET on FifoWrN cross section results

LET Eff (MeV.cm².mg^{-1})	SEFI Cross Section (cm²)	
	N° 1	N° 2
67.7	6.00E-06	3.21E-06
32.6	1.57E-06	1.82E-06
20.4	<1.00E-06	<1.47E-06
10.2	<1.00E-06	-
3	<1.94E-06	<1.00E-06
1.1	<1.00E-06	-

Table 29: FIFO Interface SEFI cross section results

The following figures present the cross section of SET on FifoWrN signal of FIFO Interface for the AT7913.
Points represented by an arrow pointing down indicate that no events were observed at the corresponding LET.
The evaluated cross section is then lower than 1E-6 cm^2, value corresponding to one event at maximum fluence.

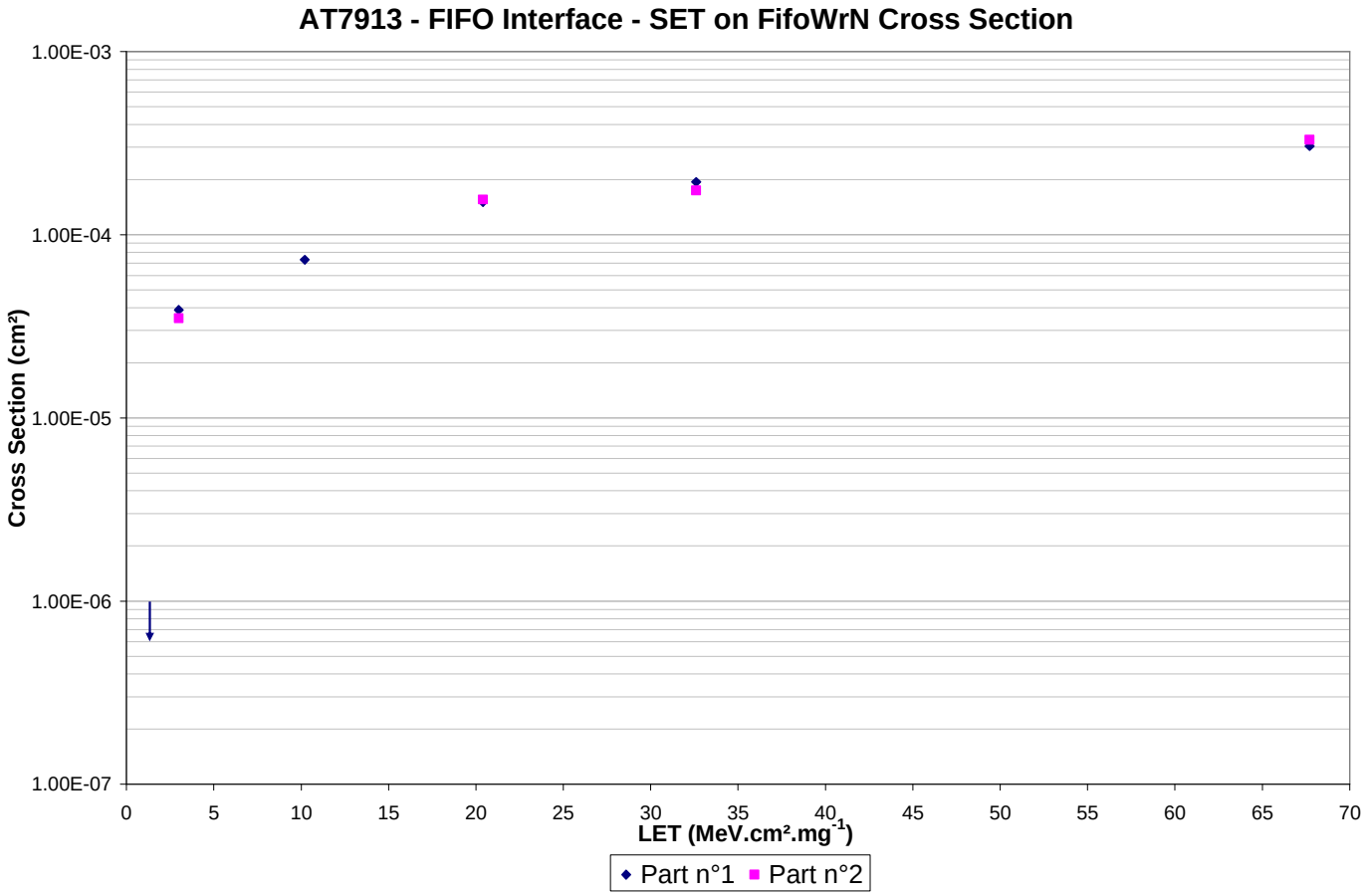


Figure 24: FIFO Interface SET cross section curve for AT7913

7.2.4.2. Worst Cases SET Observed

The event bellow shows that the duration between two pulse activations of WrN pin, was 8.04µs instead of 7µs. This is the maximum gap between two activations of WrN. It occurs on Part N°1 during run n°20 event n°105 (Kr, 32.4 MeV.cm²/mg)

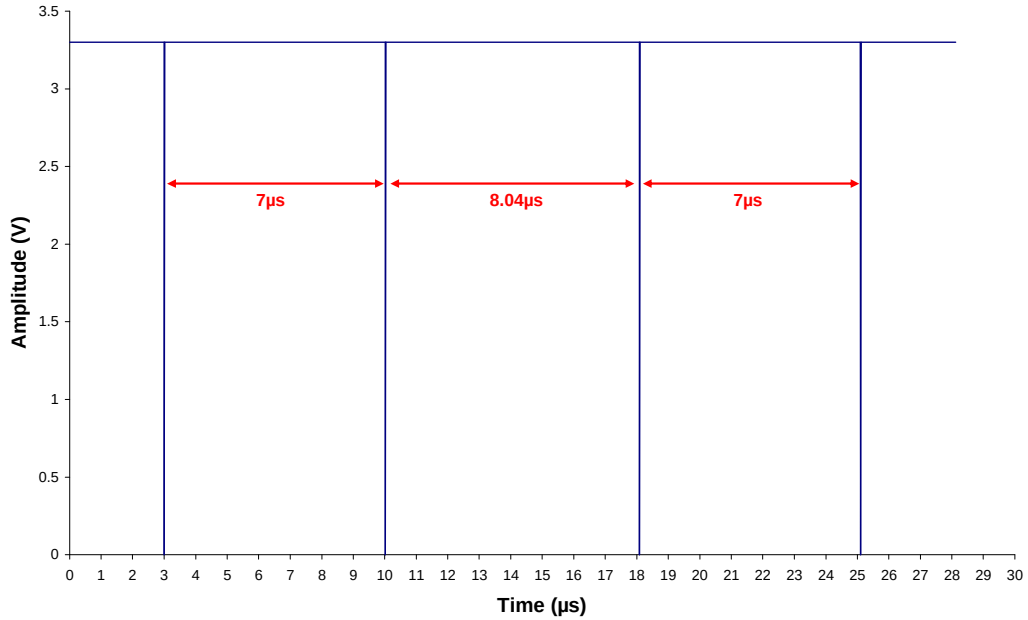


Figure 25: SET curve on WrN pin, Heavy Ion $^{83}Kr^{25+}$ (LET of 32.4MeV.mg/cm²), Part 1, Run n°20, Event n°105

7.2.5. 32-bit timer SEE tests results

The details of all runs for this test are showed in Table 16.

At the beginning of the test, the sensitivity was investigated in order to determine if the four different timers show the same sensitivity. As results show the same sensitivity for the four timers, the cross section has been estimated only for internal timer 1.

The majority of the events observed, were a duty cycle change, certainly due to the processor. In case in which an error on a single width is observed, we could assume that it is a problem on the timer, however we have systematically observed two consecutive wrong widths whose duration is at least as long as the signal period (81.92 µs for internal timer 1).
For example, in figure 27, when we add the two wrong widths 41.72 µs and 40.19 µs, we have 81.91µs that correspond to the signal period.
In figure 28, there are three consecutive wrong widths (it's the only case), when we add these widths, we have 122.87 µs that correspond to three half periods. We conclude that the problem comes from the processor because if it wasn't the case the duration wouldn't be proportional to the half period.
In figure 29, this event is a problem during the clearing request of the flag interrupt. Therefore, the processor has executed twice the interrupt program and the outputs have toggled every time.
As the events have been identical on all outputs, we can conclude that the events detected, are not due to a problem on PIO but due to the processor itself.

SEFIs have been detected during runs n°18, n°121, n°142 due to a stuck output signal for more than 100 ms. For the run n°121, two SEFIs were due to trap 0x02 "illegal instruction" and one SEFI due to changing of value of "I/O direction register". For the run n°142 the SEFIs were due to trap 0x03 "privileged instruction" and at toggling of bit 0 "Enable the timer" of "Timer control registers". For the others, no traps occurred and no timer configuration registers were changed, according to the registers. The normal operation was recovered with a reset after the SEFI.

SETs for internal timer 1, were observed during the irradiation up to the Neon Ion (LET = 3 MeV.cm²/mg).

7.2.5.1. 32-bit timer SET Cross sections

LET Eff (MeV.cm².mg^{-1})	SET Cross Section (cm²)	
	N° 1	N° 2
67.7	1.09E-04	1.44E-04
32.6	9.60E-05	9.40E-05
20.4	8.10E-05	9.60E-05
10.2	3.80E-05	-
3	2.16E-05	1.90E-05
1.1	<1.00E-06	-

Table 30: 32-bit timer SET cross section results

The following figure presents the cross section of SET by the AT7913 on internal timer 1.
Points represented by an arrow pointing down indicate that no events were observed at the corresponding LET.
The evaluated cross section is then lower than 1E-6 cm², value corresponding to one event at maximum fluence.

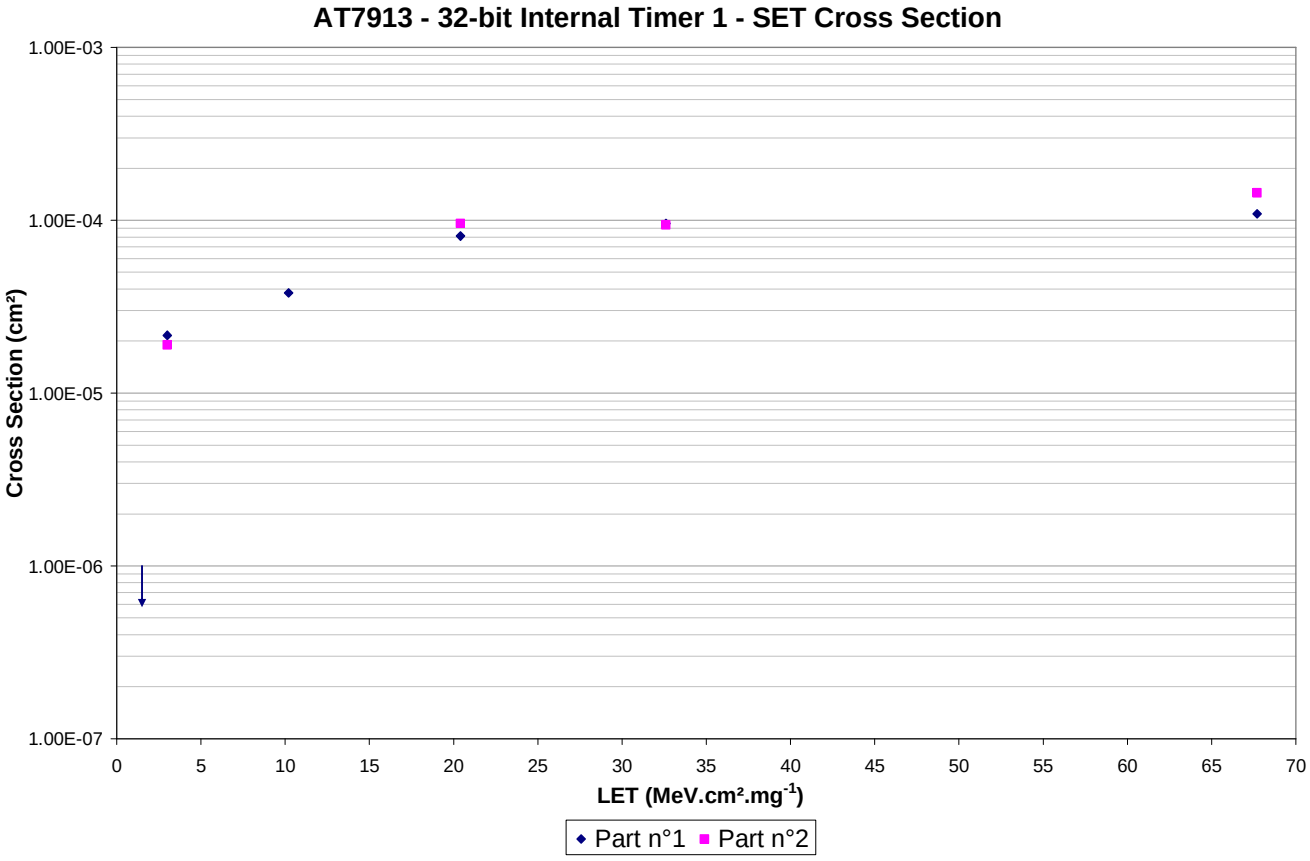


Figure 26: 32-bit timer SET cross section curve for AT7913

7.2.5.2. Worst Cases SET Observed

The worst SET case occurs on Part N°2 during run n°142 event n°117 (Xe, 67.7 MeV.cm²/mg).

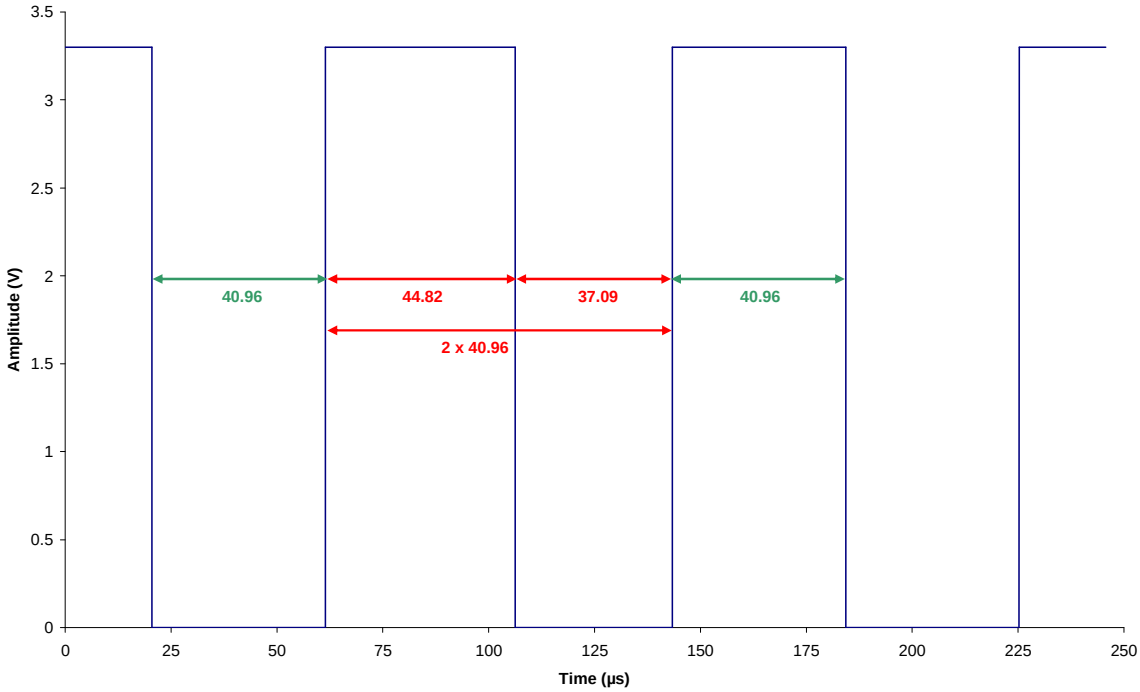


Figure 27: SET curve Heavy Ion $^{124}Xe^{26+}$ (LET of 67.7MeV.mg/cm²), Part 2, Run n°142, Event n°117

The worst SET case occurs on Part N°1 during run n°16 event n°44 (Kr, 32.4 MeV.cm²/mg).

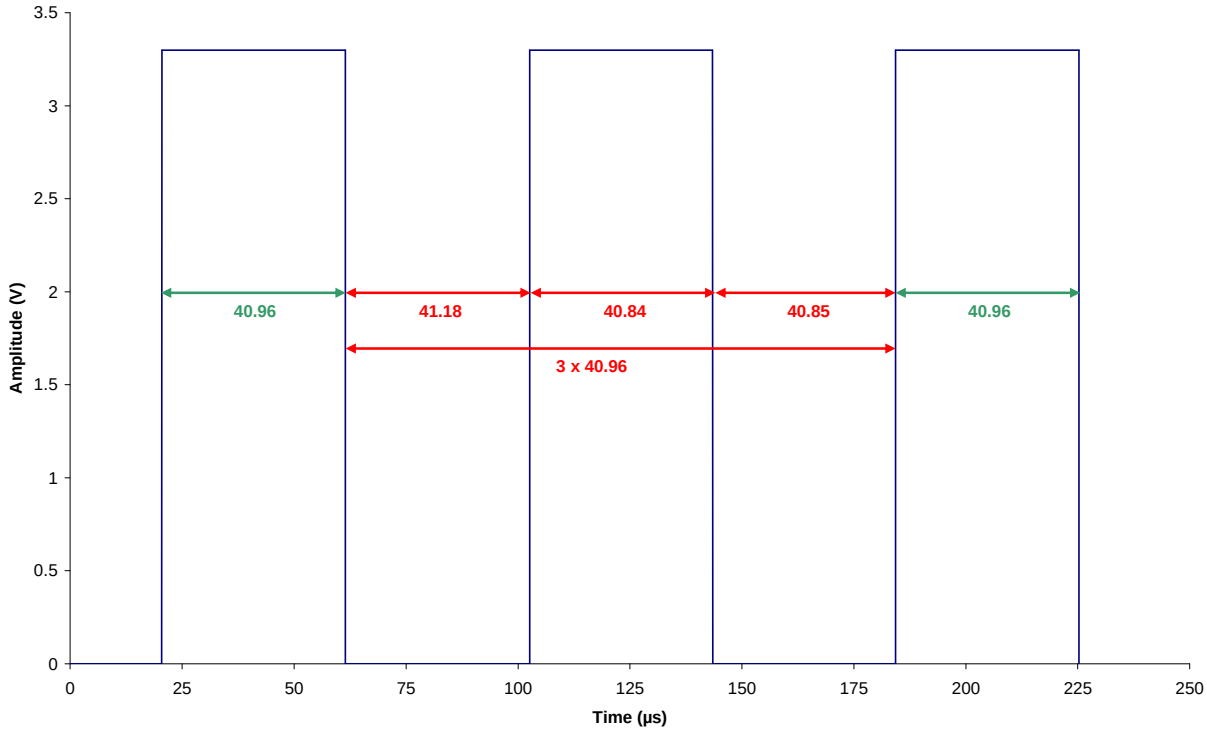


Figure 28: SET curve Heavy Ion $^{83}Kr^{25+}$ (LET of 32.4MeV.mg/cm²), Part 1, Run n°16, Event n°44

The worst SET case occurs on Part N°1 during run n°15 event n°2 (Kr, 32.4 MeV.cm²/mg).

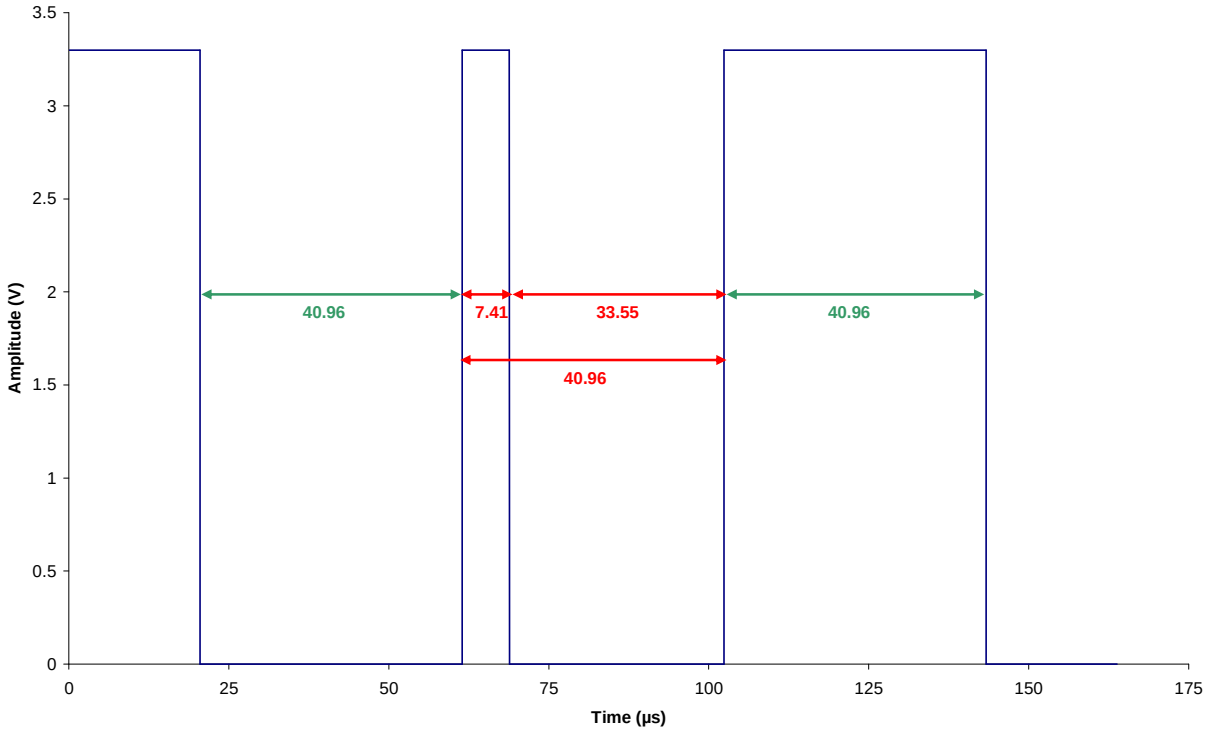


Figure 29: SET curve Heavy Ion $^{83}Kr^{25+}$ (LET of 32.4MeV.mg/cm²), Part 1, Run n°15, Event n°2

7.2.6. 24bits GPIO & 16bits LeonPIO SEE tests results

The details of all runs for this test are shown in Table 11.

SEFIs were detected mainly due to changing of direction of Leon PIO. A toggle of bits 13, 12 and 5 of "I/O direction register" were observed on the run n°122 and run n°143. But for one SEFI of run n°143, according to the registers, no traps and no PIO configuration registers were changed.
The normal operation was recovered with a reset after the SEFI.

No SEU was detected with the two patterns, up to the maximum tested LET of 67.7MeVcm^2/mg (Xenon) and a fluence of 1E+6 ions/cm^2

7.2.6.1. 24bits GPIO & 16bits LeonPIO SEFI Cross sections

LET Eff (MeV.cm².mg^{-1})	SEFI Cross Section (cm²)	
	N° 1	N° 2
67.7	2.00E-06	3.00E-06
32.6	<1.00E-06	<1.00E-06

Table 31: 24bits GPIO & 16bits LeonPIO SEFI cross section results

7.2.7. UART serial link SEE tests results

The details of all runs for this test are showed in Table 15.

SETs for UART 1, were observed during the irradiation down to the Nickel Ion (LET = 20.4 MeV.cm²/mg).
SET for UART 2, was observed during the irradiation only with the Xenon Ion (LET = 67.7 MeV.cm²/mg).

SEFIs for UART 1, were observed during the irradiation only with the Xenon Ion (LET= 67.7 MeV.cm²/mg).
SEFIs for UART 2, were observed during the irradiation down to the Nickel Ion (LET = 20.4 MeV.cm²/mg).

During the first campaign, SETs and SEFIs have been detected in the same time on UART1 and UART2 for DUT n°2. When SET occurred on UART 1, a SEFI occurred at the same time on UART 2. It's possible that an event impacted the interrupt management of two UARTs and if the processor misses an interrupt no data will be sent through UART port, in our case through UART 2.
For the second campaign, the two UARTs were tested independently.
For the UART 1, only two SEFIs were detected due to traps. The code SPARC trap types (of tbr register) are the following:

- Run n°123: one Traps 0x2B "write buffer error", two traps 0x0B "watchpoint detected" were detected and one SEFI with no information
- Run n°144: Trap 0x02 "illegal instruction", 0X0A "Tagged arithmetic overflow" were detected.

For UART2 one SET and one SEFI were detected at the maximum tested LET (Xenon LET=67.7MeVcm^2/mg) and a fluence of 1E+6 ions/cm^2. This SEFI was due to toggling of PIO direction because the value of register "I/O direction register" was changed.

These results are interesting, because, if we compare results observed with 32-bit timer test and UART serial link test, we can see that very few events were detected in UART test. For UART test the switching

of the outputs has not been directly managed by an interrupt. During UART interrupt, the processor sent a writing request on the UART ports and then the UART modules send the data on TX signals. For the 32-bit timers, it is quite different, for every interrupt, the processor sent directly the data on the PIO outputs. It means that, in the case of the 32-bit timers, the processor performs more action than in the case of the UART. Therefore, if there was a problem with the processor (e.g. time-lag with interrupt detected), the PIO outputs would be directly impacted. This observation supports the hypothesis that the errors were due to the processor and not to the function tested.

7.2.8. External memory access SEE tests results

The details of all runs for this test are showed in Table 13.

No SEU were detected, during this test up to Xenon irradiation with a total fluence equal to 1E+6 ions/cm^2 (LET=67.7 MeV.cm²/mg and range=37µm). Therefore, no event was detected on the data and address bus of external memory access.

One SET on IoOeN pin for external memory access, was observed during the irradiation with the Xenon Ion (LET=67.7 MeV.cm²/mg and range = 37µm).

SEFIs for external memory access, were observed during the irradiation down to the Krypton Ion (LET= 32.6 MeV.cm²/mg). The normal operation was recovered with a reset after the SEFI.

This SEFI that occurred during the first campaign (run 45), because the EDAC check bits bus broke to low level ($0) instead of that being equal to $C. Actually, the “WB” and “RE” bits of “MCFG3” register were toggled. The switching of the first bit led to bypass the EDAC diagnostic write and the switching of the second one led to disable the EDAC checking of the RAM area.
During the second campaign (run 167), a SEFI was detected because the checksum was wrong ten times in succession and another SEFI was detected because RomCsN[2] and RomCsN[0] pins were frozen to active level.

7.2.9. ADC/DAC interface

The details of all runs for this test are shown in Table 14.

No events were detected on the data and the address bus, as on the static signals, during this test up to Krypton irradiation with a total fluence equal to 1E+6 ions/cm^2 (LET=32.4 MeV.cm²/mg and range=37µm).

SETs were detected on ADRc static signals, during this test under Xenon irradiation with a total fluence equal to 1E+6 ions/cm^2 (LET=67.7 MeV.cm²/mg and range=37µm). The ADRc pin was activated during one clock cycle.

SETs on ADWr signal, were observed during the irradiation down to the Neon Ion (LET = 3 MeV.cm²/mg).

The majority of the events observed, were a time lag of writing request on ADWr signal, certainly due to processor. All writing requests were transferred except one in run n°125 and there never was any change on the pulse width of ADWr signal.

Due to a failure that occurred on the test bench during the first campaign, the SEFI detection was performed by a manual system based on the monitoring of ADWr and ADData_0 signals.
When the signals froze on the scope, the run was stopped.

The part was configured to switch into debug mode when the processor entered an error condition. Every time a SEFI was detected, the bit "Error mode" of "DSU trap register" was set (no information for the run n°21 due to a technical error), because a trap caused the processor to enter into error mode. Therefore, the break of the part was due to a trap, the code SPARC trap type (of tbr register) for the run n°22 is 0x02 "illegal instruction".

For the second campaign the test bench was modified to generate a reset after a SEFI, thus the runs weren't aborted after SEFI and that there has been more than one SEFI which was detected. The normal operation was recovered with a reset after the SEFI.

For the run number 123 three SEFIs were detected but according to the registers, only two were due to traps and for the others SEFIs no traps occurred and no ADC/DAC configuration registers were changed.
The code SPARC trap types (of tbr register) are the following:

- Trap 0x02 "illegal instruction" was detected.
- Trap 0X1B "Asynchronous interrupt 11" was detected.

7.2.9.1. ADC/DAC Interface SET Cross sections

LET Eff (MeV.cm².mg^{-1})	SET Cross Section (cm²)	
	N° 1	N° 2
67.7	3.01E-04	2.45E-04
32.6	1.75E-04	2.17E-04
20.4	1.60E-04	1.57E-04
10.2	8.70E-05	-
3	4.13E-05	3.10E-05
1.1	<1.00E-06	-

Table 32: ADC/DAC Interface SET on ADWr signal cross section results

It can be observed that the events detected are identical between the FIFO interface and the ADC/DAC interface with the same cross section. However, it can be supposed that they do not have the same design, because they absolutely do not have the same function. For the test of these interfaces, the only commonality is the processor, which supports the hypothesis that the events were not due to a problem on the interface itself.

The following figures present the cross section of SET by the AT7913 on ADWr signal of ADC/DAC Interface.
Points represented by an arrow pointing down indicate that no events were observed at the corresponding LET.
The evaluated cross section is then lower than 1E-6 cm^2, value corresponding to one event at maximum fluence.

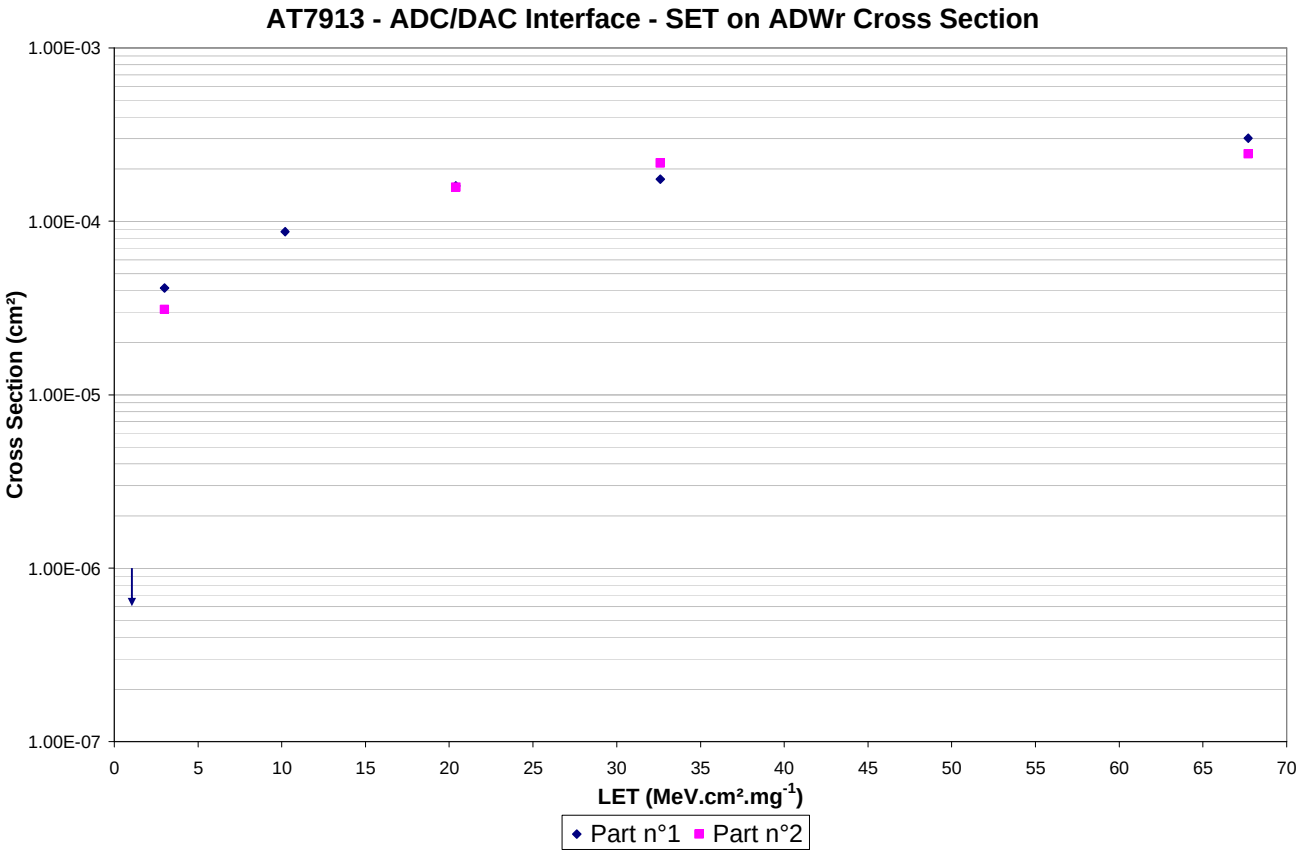


Figure 30: ADC/DAC Interface SET on ADWr cross section curve for AT7913

7.2.9.2. Worst Cases SET Observed

The maximum gap between two activations of WrN pin occurs on Part N°1 during run n°2 event n°140 (Kr, 32.4 MeV.cm²/mg).

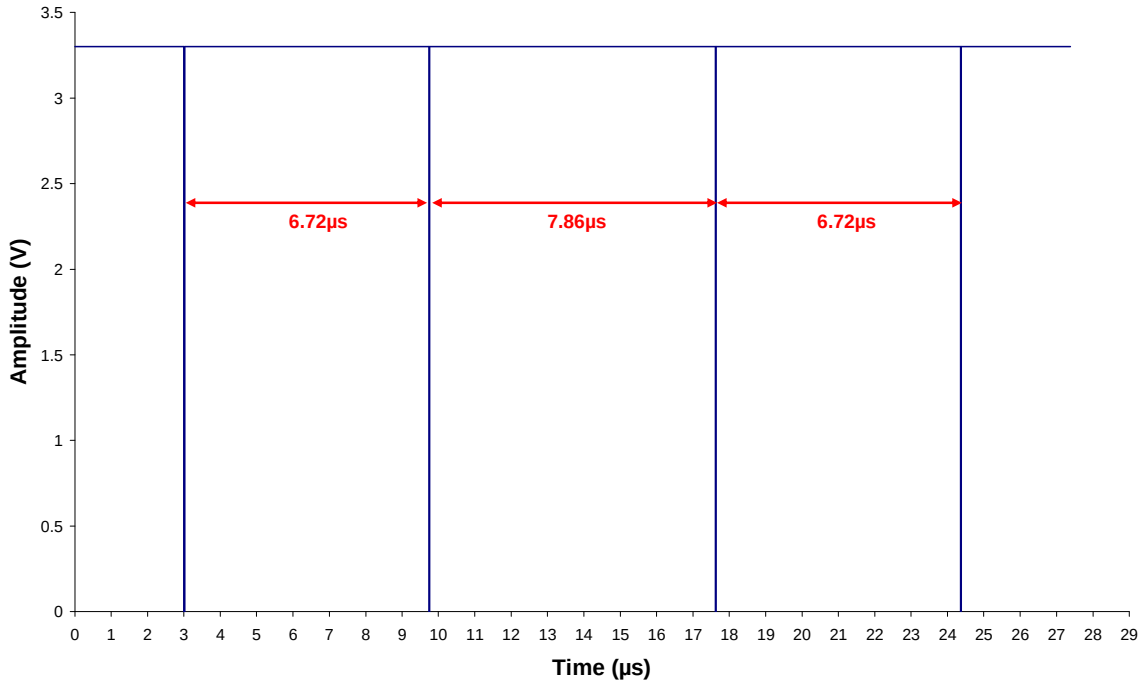


Figure 31: SET curve on ADWr pin, Heavy Ion $^{83}Kr^{25+}$ (LET of 32.4MeV.mg/cm²), Part 1, Run n°2, Event n°140

7.2.10. On-chip Memory SEE tests results

The details of all runs for this test are showed in Table 18.

The on-chip memory has been tested with EDAC protection in run n°8 with a high flux and in run n° 9 with a low flux. We observed fewer events with a low flux than with the high flux, because the EDAC had more time to correct the errors in the on-chip memory. Then, we have used the low flux for the runs with EDAC protection, but the flux was still too high.

A MBU was counted when there was more than one bit that has toggled on a 32-bit word. We could observe on some of the MBU events that only one bit has toggled by byte. For example, between the correct data $AA55AA55 and the wrong data detected $EA55AE55, there is only one bit that toggled on two bytes. For the other MBU events, we have frequently observed two bits that toggled on one byte.

During the second campaign, the runs without EDAC protection were performed with a fluence higher than during the first campaign, which allowed us to observe MBUs because the probability of two bits in error in 32-bit word was increased. A reading “Test Check Bits” field of “Configuration register bit fields” register during the second reading of data error, was added and thus several case its were observed, during the runs in high LET:

- When a SEU of type 2 was detected with EDAC protection, the data reading in the Test Check Bits field (red square in Figure 32) of configuration register was wrong. This data corresponding to checkbits stored with the data in memory (red ring in Figure 32). It is possible that SEU detected on the data was due to an erroneous correction during the decoding (red line in Figure 32). As these checkbits and the new recalculation of checkbits were different, the part corrected the data while the data was correct. Therefore, the data was read corresponding to corrected data with wrong checkbits.

- When a SEU of type 1 was detected with EDAC protection, the Test Check Bits field (red square in Figure 32) of the configuration register was right. Thus, SEU was due to a transient error that appeared on the data bus at the time of reading.

- When a MBU was detected with or without EDAC protection, the checkbits was right except once in run n°200.

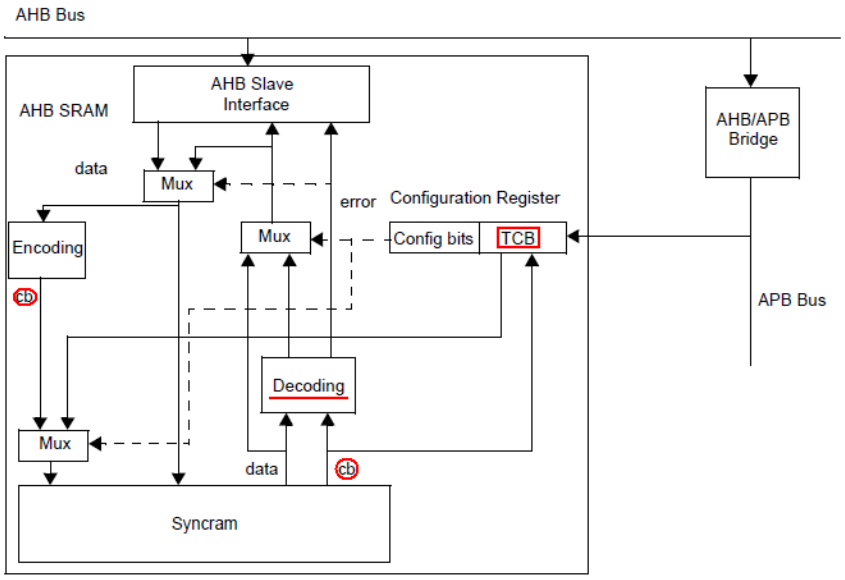


Figure 32: The FT AHB RAM block diagraml

SEUs for the on-chip memory with EDAC protection, were observed during the irradiation down to the NIckel Heavy Ion (LET = 20.4 MeV.cm²/mg). These SEUs probably are due to SEUs in checkbits stored in memory.
SEUs for the on-chip memory without EDAC protection, were observed during the irradiation down to the Carbon Ion (LET = 1.1 MeV.cm²/mg).

On the next table, the SEU cross sections were calculated per bit with the memory of 64 Kbytes and the MBU cross sections were calculated per word of 32 bits with the memory of 16 Kwords.

7.2.10.1. On-chip Memory with EDAC MBU Cross sections

LET Eff (MeV.cm².mg^{-1})	MBU Cross Section (cm²/word)	
	N° 1	N° 2
67.7	2.38E-09	3.11E-09
40.4	1.10E-09	9.77E-10
32.6	4.09E-10	5.49E-10
20.4	1.22E-10	1.22E-10
10.2	<6.10E-11	-
3	<1.18E-10	<6.10E-11

Table 33: On-chip Memory with EDAC MBU cross section results

7.2.10.2. On-chip Memory without EDAC MBU Cross sections

LET Eff (MeV.cm².mg^{-1})	MBU Cross Section (cm²/word)	
	N° 1	N° 2
67.7	2.02E-09	2.63E-09
40.4	1.59E-09	2.38E-09
32.6	<2.90E-09	<2.61E-09
20.4	<2.36E-09	<2.34E-09
10.2	<1.27E-09	-
3	<5.40E-10	<5.91E-10
1.1	<6.10E-11	-

Table 34: On-chip Memory without EDAC MBU cross section results

7.2.10.3. On-chip Memory with EDAC SEU Cross sections

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²/bit)	
	N° 1	N° 2
67.7	5.72E-12	3.81E-12
40.4	3.81E-12	1.91E-12
32.6	6.39E-12	5.72E-12
20.4	5.72E-12	1.91E-12
10.2	<1.91E-12	-
3	<3.69E-12	<1.91E-12

Table 35: On-chip Memory with EDAC SEU cross section results

7.2.10.4. On-chip Memory without EDAC SEU Cross sections

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²/bit)	
	N° 1	N° 2
67.7	3.56E-08	3.53E-08
40.4	2.83E-08	2.88E-08
32.6	2.24E-08	2.32E-08
20.4	1.53E-08	1.53E-08
10.2	8.39E-09	-
3	3.61E-09	3.71E-09
1.1	1.91E-11	-

Table 36: On-chip Memory without EDAC SEU cross section results

The following figures present the cross section of SEU by the AT7913 for the on- chip memory without EDAC.

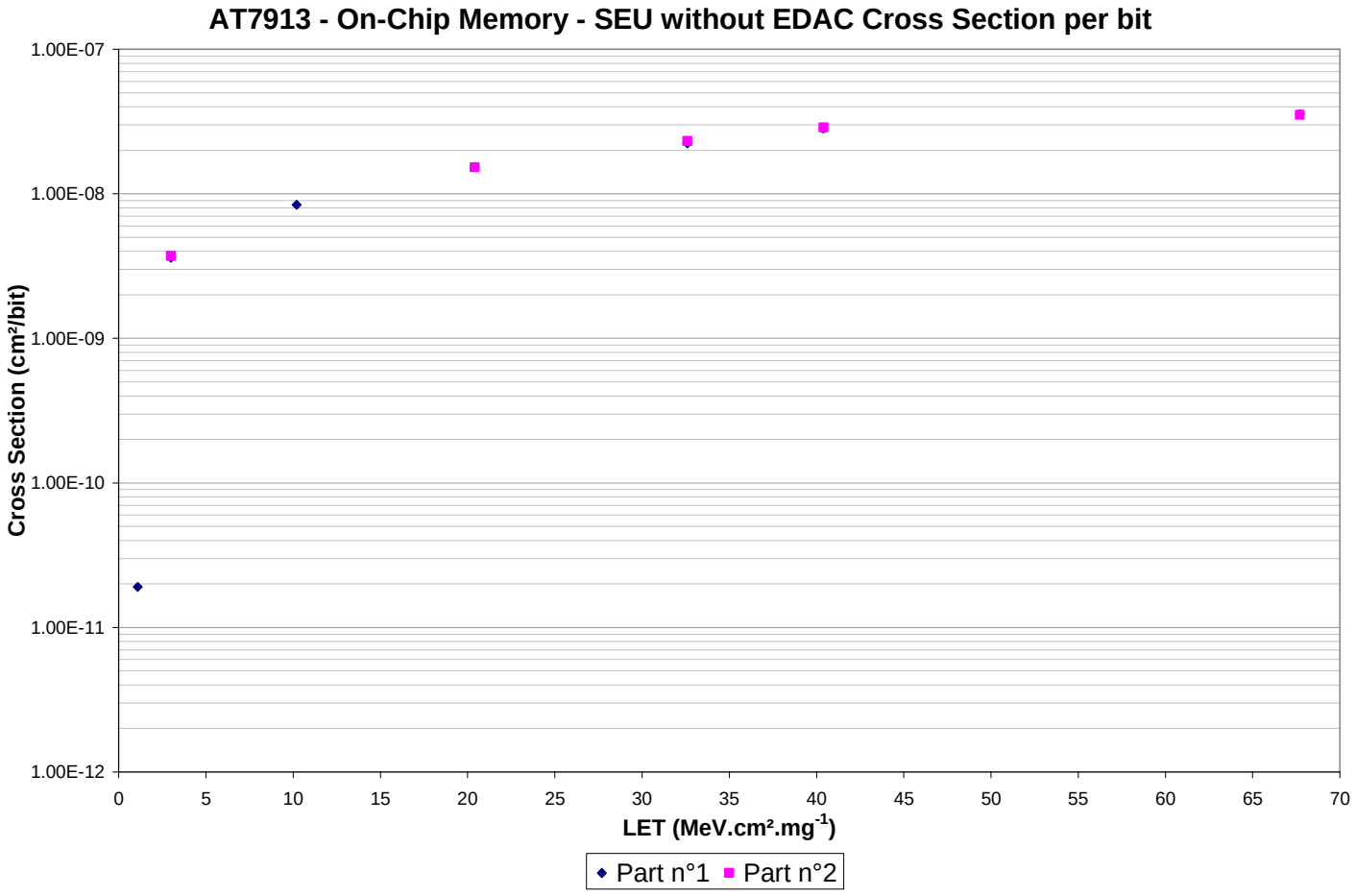


Figure 33: On-chip Memory without EDAC SEU cross section curve for AT7913

.

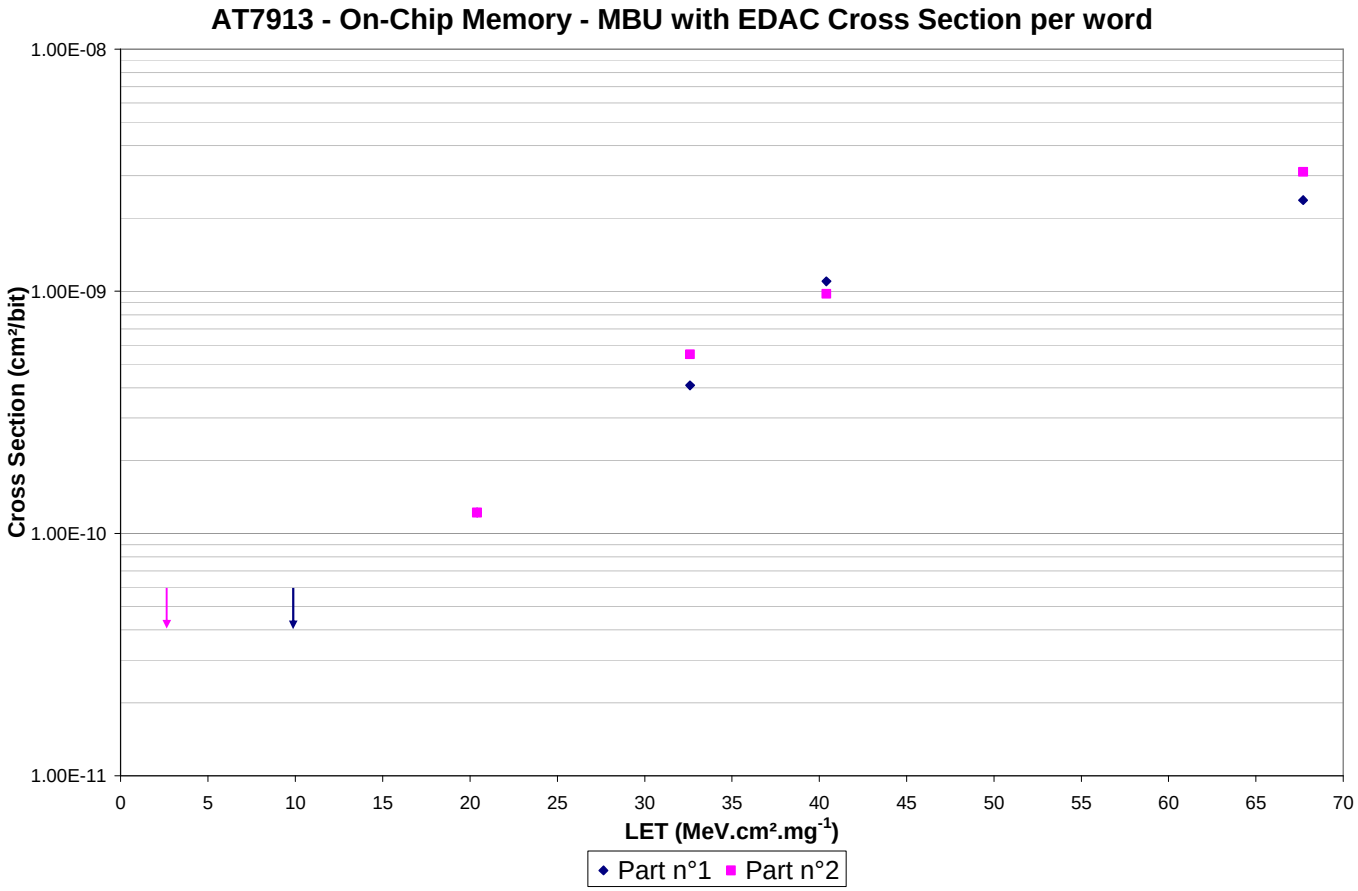


Figure 34: On-chip Memory with EDAC MBU cross section curve for AT7913

7.2.11. CAN bus interface SEE test results

The details of all runs for this test are shown in Table 17.

During the Xenon runs of SEUs were detected. The origins of these SEUs are following:

- An error on the data and therefore on the CRC.
- An error on CRC and no error on data.
- Sending of a new frame was delayed of one time cycle.
- Sending of the Acknowledge Delimiter bit was delayed of several time cycles.

The SEFIs were due to traps according to register. The code SPARC trap types (of tbr register) are the following:

- Trap 0x01 “Error during instruction fetch” was detected.
- Trap 0X2B “write buffer error” was detected.

SEUs were detected, only at the highest tested LET (Xenon, LET=67.7 MeV.cm²/mg and range = 37µm) with a total fluence equal to 1E+6 ions/cm^2.
SEFIs were detected, only at the highest tested LET (Xenon, LET=67.7 MeV.cm²/mg and range = 37µm) with a total fluence equal to 1E+6 ions/cm^2.

7.2.11.1. CAN bus SEU Cross sections

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²)	
	N° 1	N° 2
67.7	2.00E-06	3.00E-06
32.6	<1.00E-06	<1.00E-06

Table 37: CAN bus SEU cross section results

7.2.11.2. CAN bus SEFI Cross sections

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²)	
	N° 1	N° 2
67.7	3.00E-06	<1.00E-06
32.6	<1.00E-06	<1.00E-06

Table 38: CAN bus SEFI cross section results

7.2.11.3. Worst Cases SEU Observed

SEU occurs on Part N°2 during run n°147 event n°3 (Xe, 67.7 MeV.cm²/mg). In this frame two errors were detected, one cycle delay at the beginning and seven cycle delays during the acknowledgement bit, as illustrated in the following figure.

Expected CAN Frame:

0	00011001011	0	0	0	1000	10101010 10101010 10101010 10101010 10101010 10101010 10101010 10101010	000110111000011	1	0	1	1111111
Start of Frame	Identifier	Remote transmission request	Identifier extension bit	Reserved bit	Data length code	Data field	CRC	CRC delimiter	ACK slot	ACK delimiter	End of Frame

Error CAN Frame:

00	00011001011	0	0	0	1000	10101010 10101010 10101010 10101010 10101010 10101010 10101010 10101010	000110111000011	1	0000 0000	1	1111111
Start of Frame	Identifier	Remote transmission request	Identifier extension bit	Reserved bit	Data length code	Data field	CRC	CRC delimiter	ACK slot	ACK delimiter	End of Frame

Frame delayed of one time cycle — 7 dominant bits in excess

Figure 35: SEU worst cases, Heavy Ion $^{124}Xe^{26+}$ (LET of 67.7MeV.mg/cm²), Part 2, Run n°147, Event n°3

SEU occurs on Part N°1 during run n°126 event n°1 (Xe, 67.7 MeV.cm²/mg). In this frame two errors were detected, six cycle delays during the acknowledgement bit and a CRC field disruption (Figure 36).

Expected CAN Frame:

0	00011001011	0	0	0	1000	10101010 10101010 10101010 10101010 10101010 10101010 10101010 10101010	000110111000011	1	0	1	111111
Start of Frame	Identifier	Remote transmission request	Identifier extension bit	Reserved bit	Data length code	Data field	CRC	CRC delimiter	ACK slot	ACK delimiter	End of Frame

Error CAN Frame:

0	00011001011	0	0	0	1000	10101010 10101010 10101010 10101010 10101010 10101010 10101010 10101010	000011101101100 01	1	0000 000	1	111111
Start of Frame	Identifier	Remote transmission request	Identifier extension bit	Reserved bit	Data length code	Data field	CRC	CRC delimiter	ACK slot	ACK delimiter	End of Frame

Error CRC — 6 dominant bits in excess

Figure 36: SEU worst cases, Heavy Ion $^{124}Xe^{26+}$ (LET of 67.7MeV.mg/cm²), Part 1, Run n°126, Event n°1

7.2.12. Space Wire interface SEE tests results

The details of all runs for this test are showed in Table 19 and Table 20.

During the first campaign, the part continuously sent one data byte, therefore the Space Wire interface mainly sent a NULL character when the DUT prepared to send a new byte, the Space Wire link was still active. For the second campaign, the part was programmed to continuously send 65535 data bytes (that is a software limit), thus in this case the interface mainly sent of data.

With the second program, it was observed after a certain amount of time the part didn't send the data but the NULL character. After the run n°131, when the part didn't send the data, the runs were stopped and another run was performed in order to have a fluence of 1E+6 ions/cm^2. The cross-section has been calculated in addition several runs.
During the first campaign the Space Wire link mainly sent the "NULL" character and it was more difficult to observe this event. The run n°153 was performed in order to check that this event occurred when one data byte is sent.

Very few events were detected for every run and mainly a disconnect link event. After a disconnect link event, the Space Wire interface automatically managed the restart of the link.

SEFI was detected, during the irradiation up to the Xenon Ion (LET = 67.7 MeV.cm²/mg).

SEUs were observed during the irradiation down to the Nickel Ion (LET = 20.4 MeV.cm²/mg), with the frequency of 10MHz.

7.2.12.1. Space Wire interface SEU Cross sections

LET Eff (MeV.cm².mg^{-1})	SEU Cross Section (cm²)							
	10MHz		50MHz		100MHz		200MHz	
	N° 1	N° 2	N° 1	N° 2	N° 1	N° 2	N° 1	N° 2
67.7	7.00E-06	2.25E-06	3.00E-06	2.83E-06	3.30E-06	7.99E-06	1.62E-06	4.40E-06
40.4	1.45E-06	2.00E-06	2.35E-06	2.64E-06	1.00E-06	8.82E-07	<1.00E-06	2.33E-06
32.6	1.00E-06	1.00E-06	2.00E-06	1.00E-06	2.00E-06	<1.00E-06	<1.00E-06	1.00E-06
20.4	3.00E-06	1.00E-06	<1.00E-06	<1.00E-06	<1.00E-06	<1.00E-06	<1.00E-06	<1.00E-06
10.2	<1.00E-06	-	-	-	-	-	-	-
3	<1.00E-06	<1.00E-06	-	-	-	-	-	-

Table 39: Space Wire interface SEU cross section results

7.2.12.2. Worst Cases SEU Observed

When the Space Wire communication is enabled, a NULL character is automatically sent if no other character is sent by the AT7913. NULL is formed by ESCAPE followed by flow control token (FCT). NULL is transmitted, whenever a link is not sending data or control tokens, to keep the link active and to support link disconnect detection. On the curves presented in Figure 37 and Figure 38, NULL is formed by ESCAPE followed by End Of Packet (EOP) characters instead of FCT. The receiver (in our case the DUT) detects the escape error and then initiates a disconnection of the link as dictated by the ErrorReset state in the link state machine.

After the disconnection was initiated the link was standby during several microseconds and then the communication was automatically restored (Figure 41 and Figure 42). Character synchronisation was performed when a link is re-started following a link disconnection. One end of synchronisation the link starts to send Nulls, a specific sequence of 8 data bits. Next, a new data packet was sent.

In Figure 39 and Figure 40, there an error on the Data signal before a disconnect error. The signal stays to ‘0’ logical instead of being ‘1’ logical. Therefore, as there isn’t problem on the Strobe signal before a disconnect error, the clock should be delay of half period and a parity error is detected.

In the other case, one clock cycle delay on strobe signal has been observed, which caused a half-period clock shift and parity errors were detected (Figure 43).

All figures presented hereunder correspond to imported bit-stream of Star Dundee Link Analyser Mk2 software.

The SEU cases shown hereunder occur on Part N°2 with the Space Wire port 0 at 200MHz and one byte sending, during run n°153 (Xe, 67.7 MeV.cm²/mg).

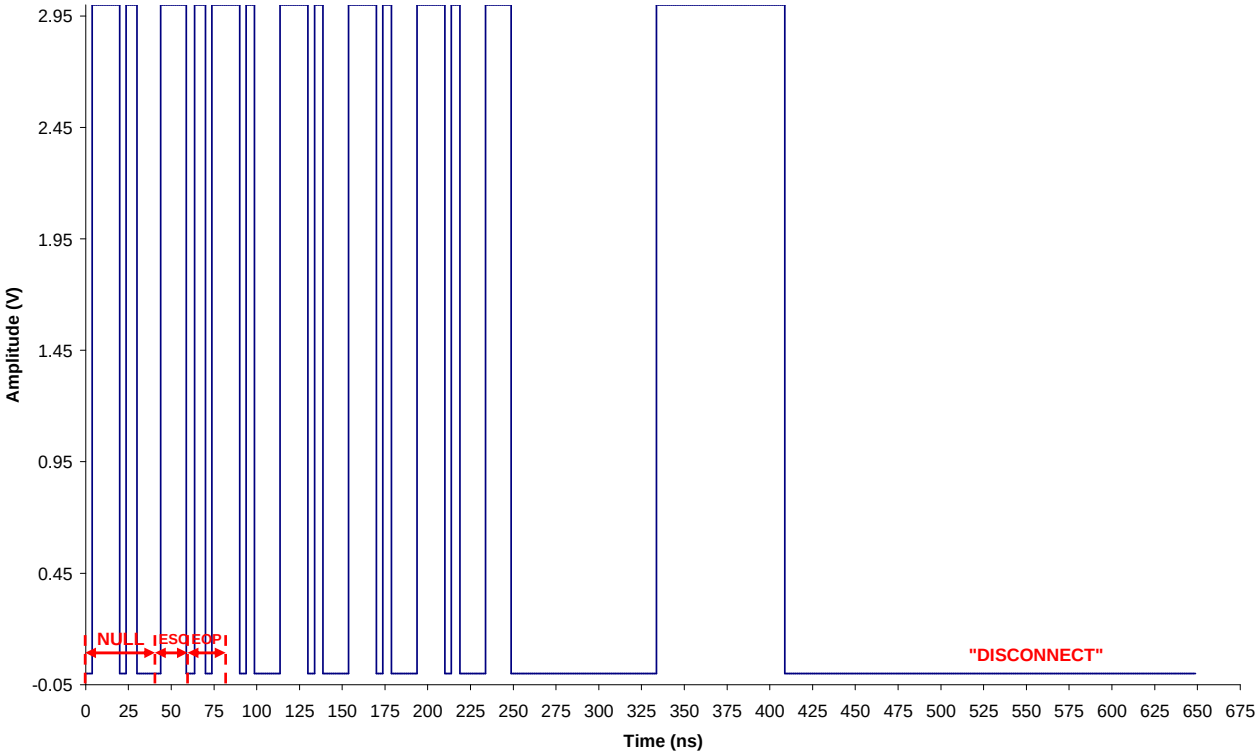


Figure 37: SEU curve Heavy Ion $^{124}Xe^{26+}$ (LET of 67.7MeV.mg/cm²), Part 2, Space Wire port 0, Data signal, Run n°153, ESCAPE-EOP.

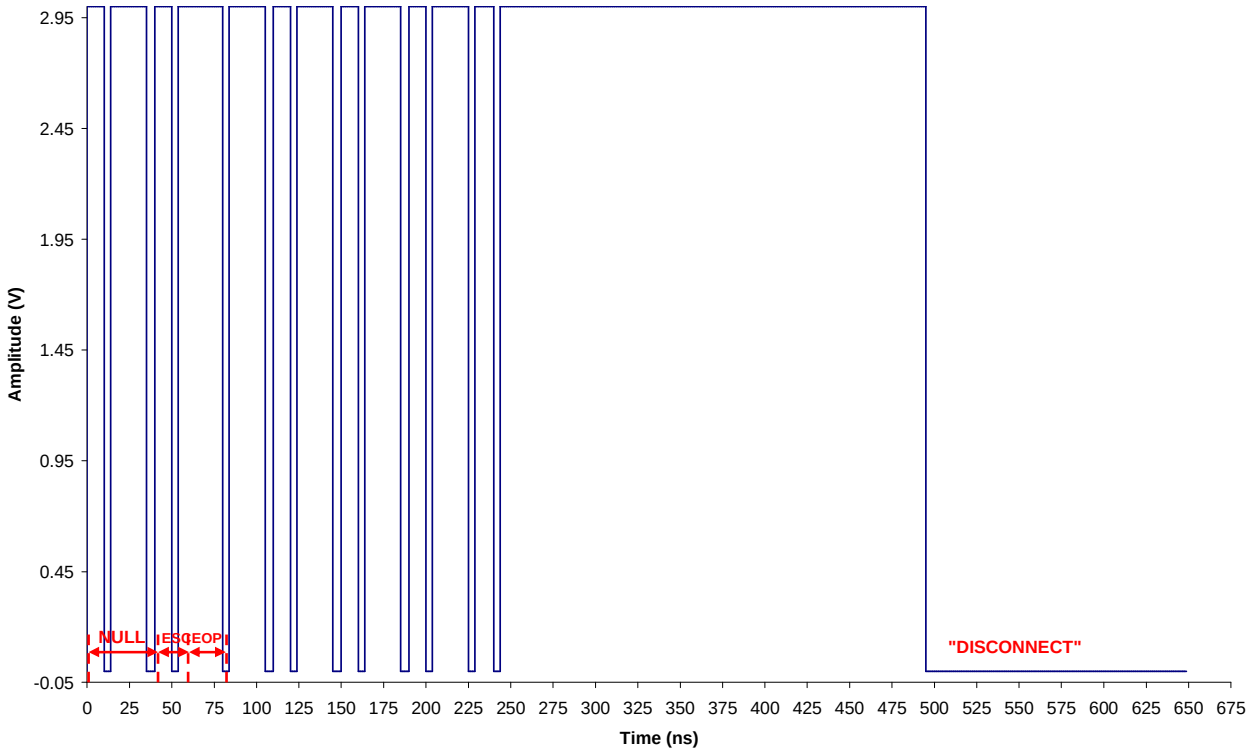


Figure 38: SEU curve Heavy Ion $^{124}Xe^{26+}$ (LET of 67.7MeV.mg/cm²), Part 2, Space Wire port 0, Strobe signal, Run n°153, ESCAPE-EOP.

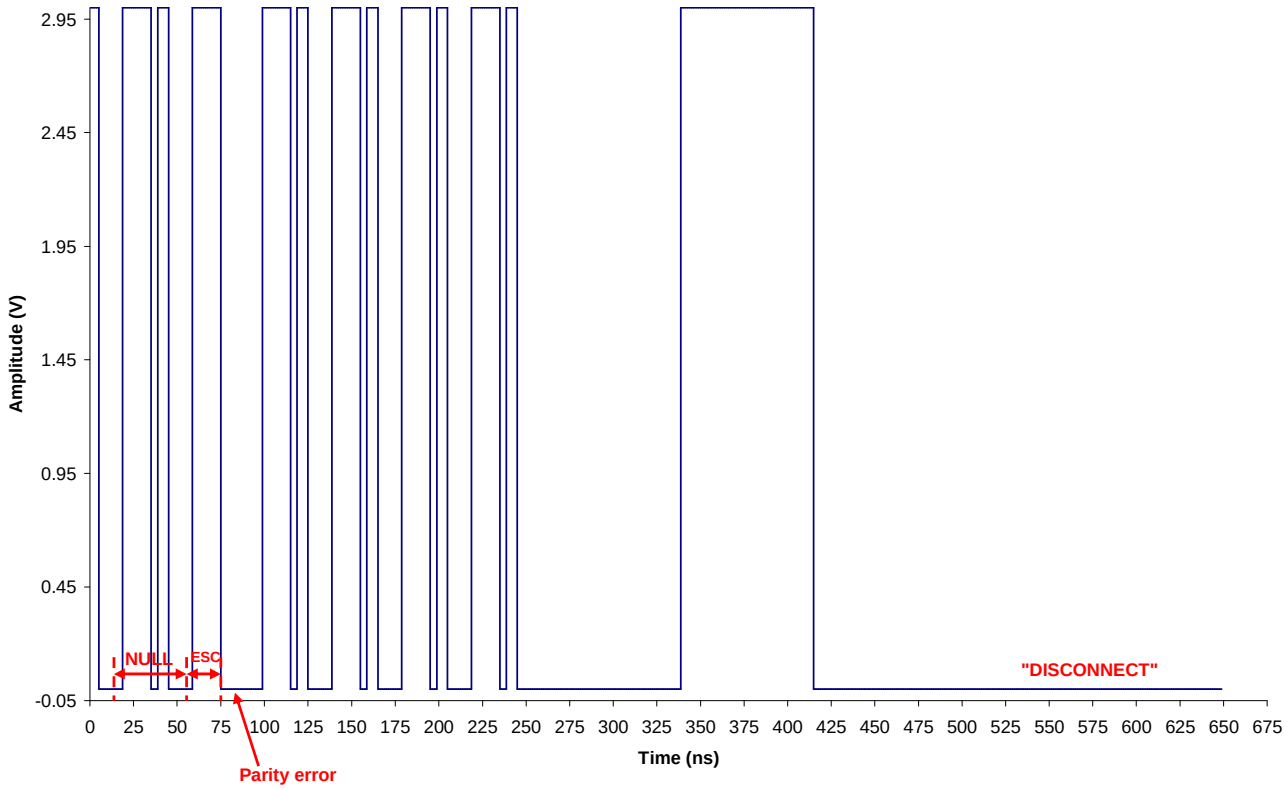


Figure 39: SEU curve Heavy Ion $^{124}Xe^{26+}$ (LET of 67.7MeV.mg/cm²), Part 2, Space Wire port 0, Data signal, Run n°153, Parity Error.

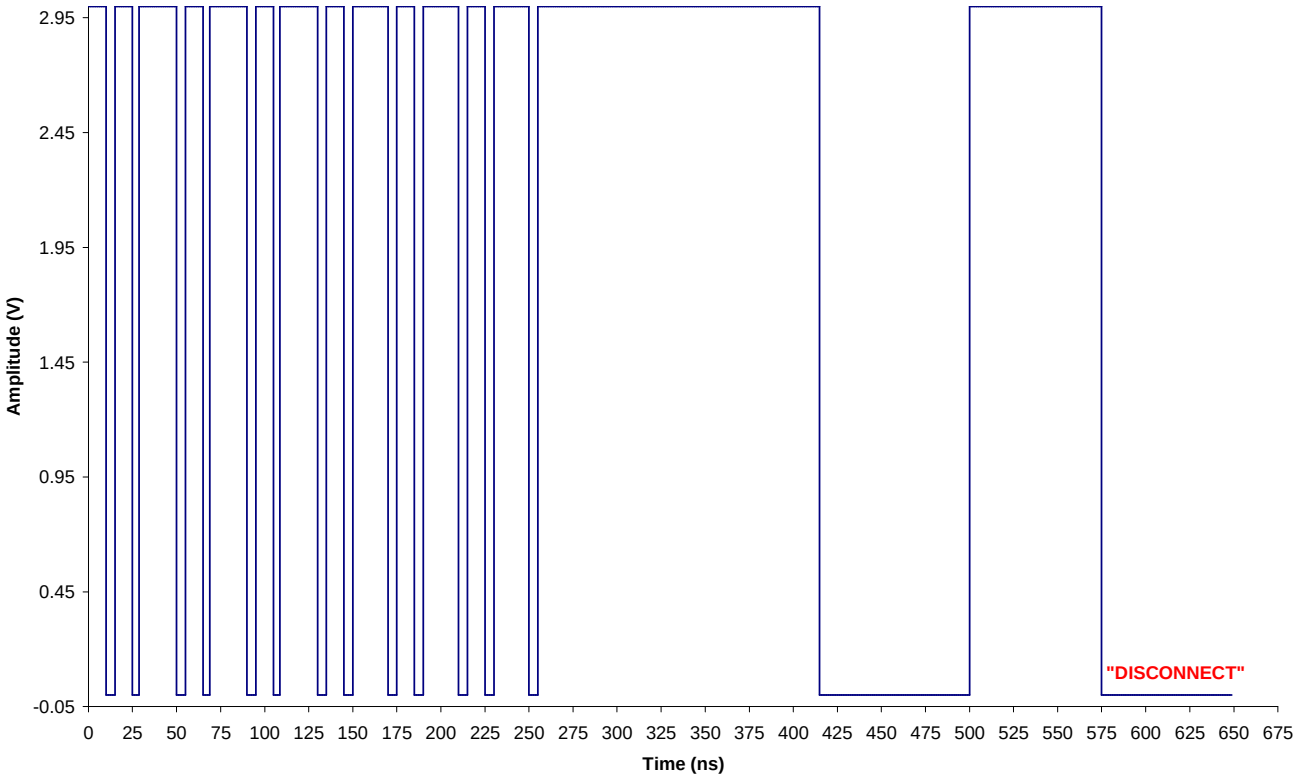


Figure 40: SEU curve Heavy Ion $^{124}Xe^{26+}$ (LET of 67.7MeV.mg/cm²), Part 2, Space Wire port 0, Strobe signal, Run n°153, Event n°2, Parity Error.

The SEU cases shown hereunder occur on Part N°1 with the Space Wire port 0 at 10MHz and 64Kbytes sending, during run n°127 (Xe, 67.7 MeV.cm²/mg).

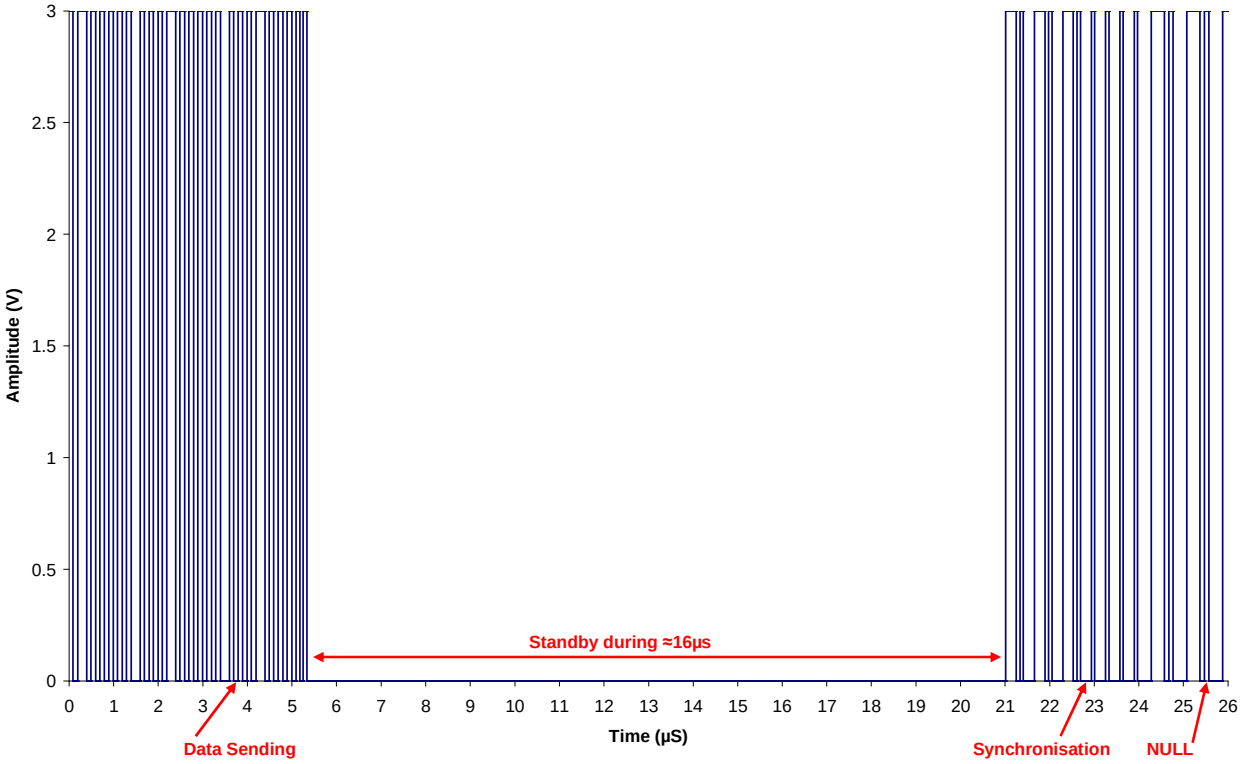


Figure 41: SEU curve Heavy Ion $^{124}Xe^{26+}$ (LET of 67.7MeV.mg/cm²), Part 1, Space Wire port 0, Data signal, Run n°127, Event n°2, Disconnect Error.

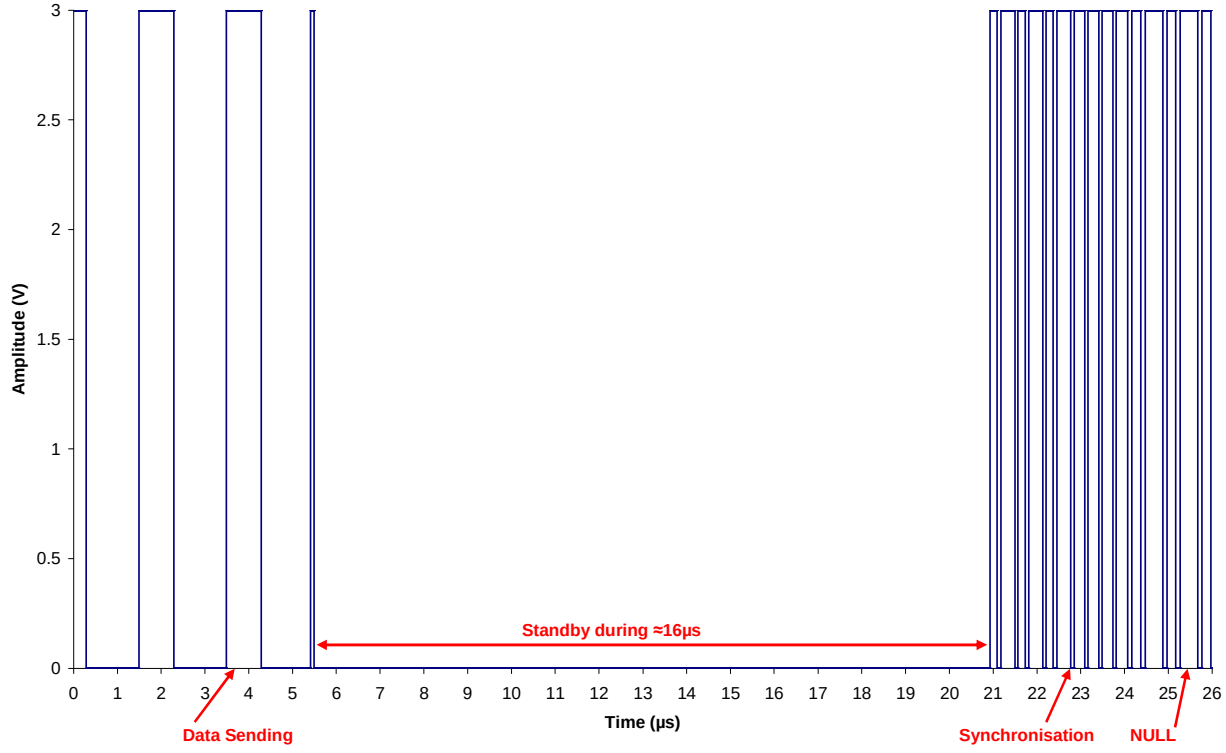


Figure 42: SEU curve Heavy Ion $^{124}Xe^{26+}$ (LET of 67.7MeV.mg/cm²), Part 1, Space Wire port 0, Strobe signal, Run n°127, Event n°2, Disconnect Error.

The SEU cases shown hereunder occur on Part N°2 with the Space Wire port 0 at 50MHz and 64Kbytes sending, during run n°150 (Xe, 67.7 MeV.cm²/mg).

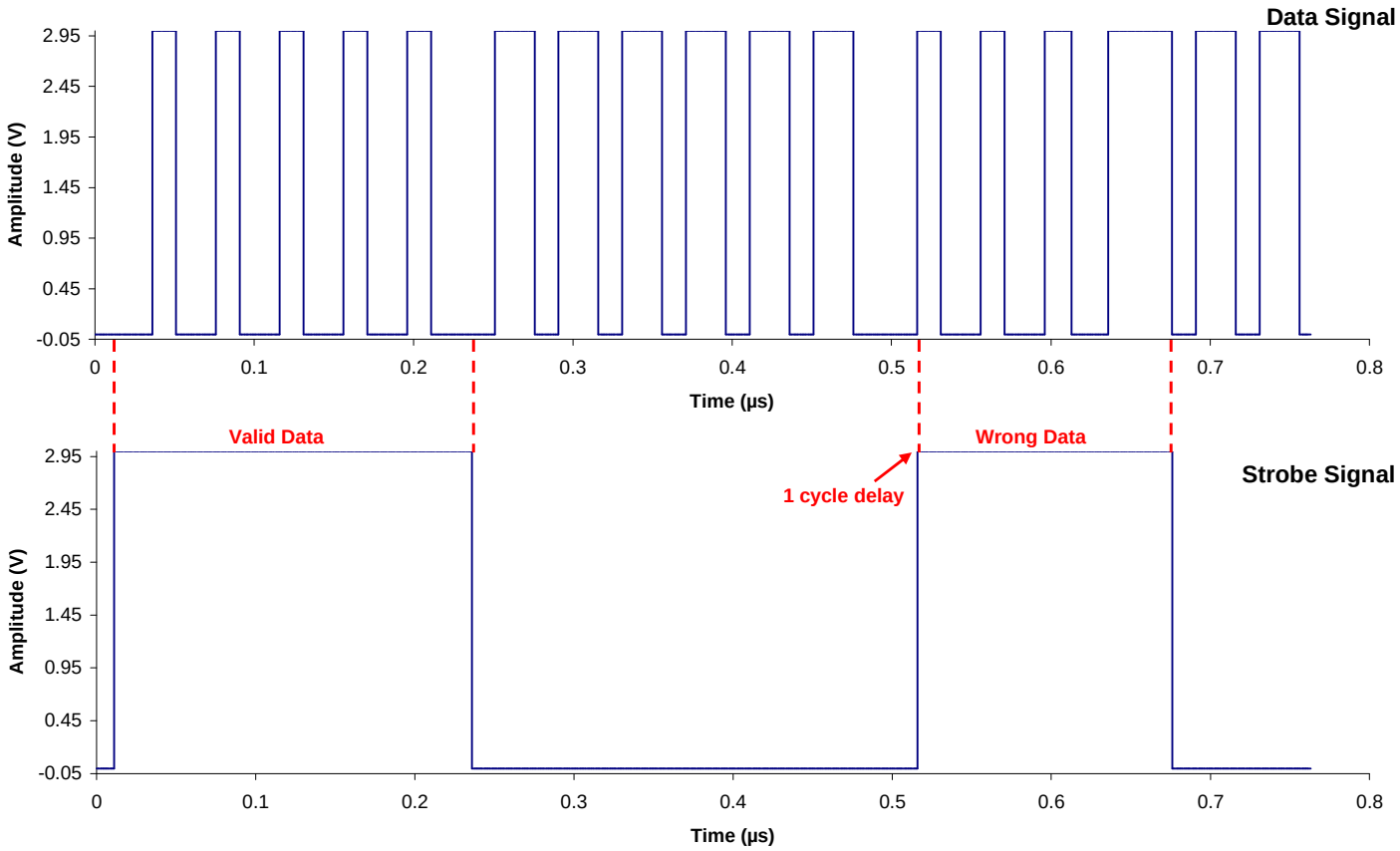


Figure 43: SEU curve Heavy Ion $^{124}Xe^{26+}$ (LET of 67.7MeV.mg/cm²), Part 2, Space Wire port 0, Strobe and Data signals, Run n°150, Event n°1, Parity Error.

8. Conclusion

The AT7913E SpaceWire RTC is a complex system with multiple functions, like FIFO Interface, GPIO and Leon PIO, LEON2-FT Processor, External memory controller, ADC/DAC interface, Space wire interface, CAN interface, on chip memory, 32-bit Timer and UART serial link.

Heavy ion tests were performed on each function of the AT7913. The aim of the test was to evaluate the sensitivity of the device versus SEU, SET, SEFI and MBU.

During the paranoia test, SEUs were observed with a minimum LET of 3 MeV.cm²/mg. Traps were detected for this test, with an LET of 67.7 MeV.cm²/mg.

During the FFT test, SEUs were observed with a minimum LET of 3 MeV.cm²/mg. One trap was detected for this test, with a minimum LET of 32.6 MeV.cm²/mg and failure runs occurred with a minimum LET of 32.6 MeV.cm²/mg.

During the cache tag memories in-static test, SEUs were observed with a minimum LET of 3 MeV.cm²/mg.
During the cache data memories in-static test, SEUs were observed with a minimum LET of 1.1 MeV.cm²/mg.
During the registers in-static test, SEUs were observed with a minimum LET of 20.4 MeV.cm²/mg.

During the FIFO interface test, SETs on the FifoWrN signal were observed with a minimum LET of 3 MeV.cm²/mg, as well as SEFIs with a minimum LET of 32.6 MeV.cm²/mg. No events were detected on the data bus and the RdN signal for this test.

During the 32-bit timers test, SETs on the WrN signal, were observed with a minimum LET of 3 MeV.cm²/mg, as well as SEFIs with a minimum LET of 32.6 MeV.cm²/mg.

During the PIO and GPIO tests, SEFIs were observed with a minimum LET of 67.7 MeV.cm²/mg. No SEU was observed detected for this test with an LET of 67.7 MeV.cm²/mg.

During the UART test, SETs on the WrN signal were observed with a minimum LET of 20.4 MeV.cm²/mg, as well as SEFIs with a minimum LET of 20.4 MeV.cm²/mg.

During the external memory access test, SEFI was observed with a minimum LET of 32.6 MeV.cm²/mg. As well as SET on static signals were detected for this test with an LET of 67.7 MeV.cm²/mg. No SEU were detected for this test. And no event was observed on data and address bus.

During the ADC/DAC interface test, SETs were observed on the ADWr signal with a minimum LET of 3 MeV.cm²/mg, as well as SEFIs with a minimum LET of 32.6 MeV.cm²/mg and SET on static signals a minimum LET of 67.7 MeV.cm²/mg No events were detected on the data and the address bus, for this test.

During the On-chip Memory test, SEUs were observed with a minimum LET of 20.4 MeV.cm²/mg with EDAC protection and a minimum LET of 1.1 MeV.cm²/mg without EDAC protection. MBUs were also observed but certainly due to the high level of the flux.

SEFIs and SEUs were detected for the CAN bus test, with an LET of 67.7 MeV.cm²/mg.

During the Space Wire test, SEUs were observed with a minimum LET of 20.4 MeV.cm²/mg. SEFIs were detected for this test, with an LET of 67.7 MeV.cm²/mg.