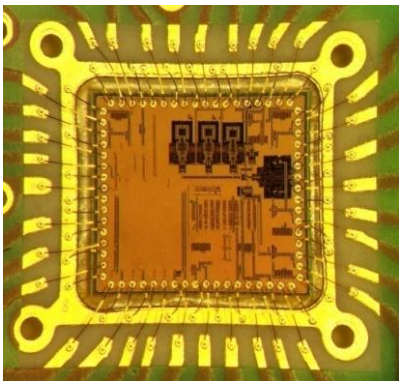
PRELIMINARY INFORMATION

Applications

- Down- and Up-Converters
- Measurement equipment
- Radar
- General Purpose Frequency Generation
- Radiation hard version available

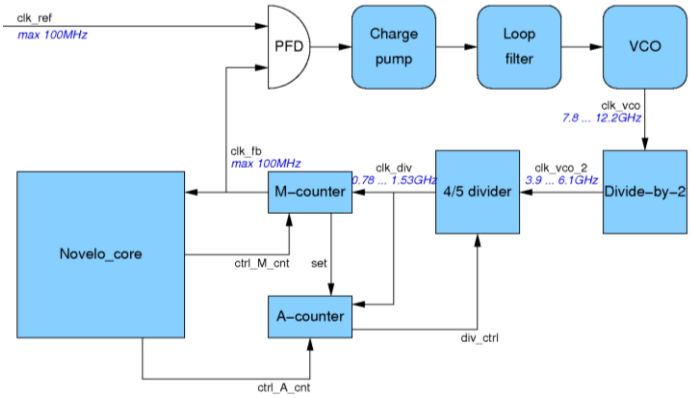


Chip size 2.46 x 2.22 mm²

Product Features

- 8-12 GHz, external VCO possible (1.5-12 GHz in preparation)
- +3 dBm Output Power (single ended)
- 1 mHz Fractional-N accuracy
- -100 dBc/Hz typ. in loop phase noise (10 KHz offset)
- No reference spurs
- 4-wire SPI (Read/Write, Master/Slave)
- XILINKS Prom option

Block Diagram



General Description

The IMST NOV8G12 is an 8-12 GHz fractional-N synthesizer, which can be programmed in mHz steps. The synthesizer can be programmed using a SPI (read/write mode). It features an output amplifier and provides a differential output power of +6 dBm (diff.) over the entire frequency range.

Ordering Information

Part No.	Description
NOV8G12	8-12 GHz Synthesizer
NOV8G12RH	Radiation hard variant
NOV8G12EB	Evaluation Board
NOV8G12PUD	PFD output for active filter

Standard order size is 25 chips.

Chip Pin Description

Pin#	Label	Type	Value	Description
01	CP_vcc	IN	+3.3 V	External supply voltage (type A).
02	CP_ldo	LDO	+2.7 V	LDO voltage regulator output (generated on-chip).
03	gnd_cp	GND		
04	PFD_ldo_in	IN	+2.7 V	External connection to CP_ldo needed.
05	PD_up	OUT		Phase detection output 'UP'. Turns from HIGH to LOW if reference frequency is ahead of feedback frequency.
06	PD_down	OUT		Phase detection output 'DOWN'. Turns to LOW if feedback frequency is ahead of reference frequency.
07	gnd_pfd	GND		
08	REF_in	IN	100 MHz	External reference frequency. The input is DC coupled, an external decoupling capacitor (1 nF) is necessary.
09	ISO1	GND		Ground connection for on-chip guard rings.
10	gnd_cmos	GND		
11	SPI_clk	IN	12.5 MHz	Clock for the Serial Peripheral Interface (SPI).
12	gnd_cmos	GND		
13	SPI_data_in	IN		SPI data input.
14	gnd_cmos	GND		
15	SPI_Data_out	OUT		SPI data output.
16	Sealring1	GND		Ground connection for on-chip seal rings.
17	Reset_ext	IN		External reset (LOW active, HIGH at normal operation).
18	gnd_cmos	GND		
19	SPI_enable	IN		SPI enable (LOW active).
20	gnd_cmos	GND		
21	LockDetectA	OUT		Analog PFD lock detect output voltage (0 to 2.5 V).
22	LockDetectD	OUT		Digital lock detect output (also provided via SPI).
23	gnd_cmos	GND		
24	CMOS_ldo	LDO	+2.5 V	
25	gnd_cmos	GND		
26	CMOS_vcc	IN	+3.3 V	External supply voltage (type A).
27	ISO2	GND		
28	CLK_fb_out	OUT		Optional feedback frequency output.
29	gnd_cntr	GND		
30	CNTR_ctrl	IN	+2.5 V	Best connected to CNTR_ldo via 100 Ω externally.
31	CNTR_ldo	LDO	+2.7 V	
32	gnd_cntr	GND		
33	CNTR_vcc	IN	+3.3 V	External supply voltage (type A).
34	Sealring2	GND		
35	gnd_div	GND		
36	DIV_vcc	IN	+3.3 V	External supply voltage (type A).
37	DIV_ldo	LDO	+2.7 V	
38	gnd_div	GND		

PRELIMINARY INFORMATION

Pin#	Label	Type	Value	Description
39	ISO3	GND		
40	AMP_vcc	IN	+5.0 V	External supply voltage (type B).
41	AMP_ldo	LDO	+3.6 V	
42	gnd_amp	GND		
43	RF_outN	OUT		Differential RF output (N), AC coupled to on-chip voltages, but 1 KΩ to GND for ESD protection.
44	gnd_amp	GND		
45	RF_outP	OUT		Differential RF output (P), AC coupled to on-chip voltages, but 1 KΩ to GND for ESD protection. Single ended output is possible (termination of the unused port via 50 Ω load is recommended).
46	gnd_amp	GND		
47	gnd_buf	GND		
48	BUF_ldo	LDO	+2.7 V	
49	BUF_vcc	IN	+3.3 V	External supply voltage (type A).
50	gnd_buf	GND		
51	Sealring3	GND		
52	VCO_vcc	IN	+5.0 V	External supply voltage (type B).
53	gnd_vco	GND		
54	VCO_extN	IN		Differential external RF input (N), AC coupled to on-chip voltages, but 1 KΩ to GND for ESD protection.
55	VCO_extP	IN	+5 dBm	Differential external RF input (P), AC coupled to on-chip voltages, but 1 KΩ to GND for ESD protection. Single ended input possible (keep unused port floating).
56	VCO_ldo_out	LDO	+4.0 V	
57	gnd_vco	GND		
58	gnd_vco	GND		
59	VCO_ldo_in	IN	+4.0 V	External connection to VCO_ldo_out necessary.
60	gnd_vco	GND		
61	Coarse_in	IN	0 to 2.7 V	Coarse voltage control input for on-chip VCOs. External connection to Fine_out via filter needed.
62	gnd_vco	GND		
63	Fine_in	IN	0 to 2.7 V	Fine voltage control input for on-chip VCOs. External connection to Fine_out via filter needed.
64	ISO4	GND		
65	gnd_cp	GND		
66	Fine_out	OUT		Fine charge pump output current.
67	Coarse_out	OUT		Coarse charge pump output current.
68	Sealring4	GND		

The given values are nominal. Please refer to the table 'recommended operating' for valid ranges.

IN: Input port OUT: output port GND: Direct down bond to the carrier board ground plane (keep bonds short)
LDO: Voltages generated on-chip, off-chip shunt capacitors needed (100 pF, 100 nF, and 2.2 µF in SMD 0201)

PRELIMINARY INFORMATION

Absolue Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
RF Input Power	+13 dBm
Device voltage	+3.6 V/+5.5 V
SPI I/O	+3.6 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating

Parameter	Min	Typ	Max	Units
Temperature	-40	+23	+85	°C
Device Voltage A	+3.0	+3.3	+3.6	V
Device Voltage B	+4.5	+5.0	+5.5	V
SPI I/O	+2.25	+3.3	+3.6	V

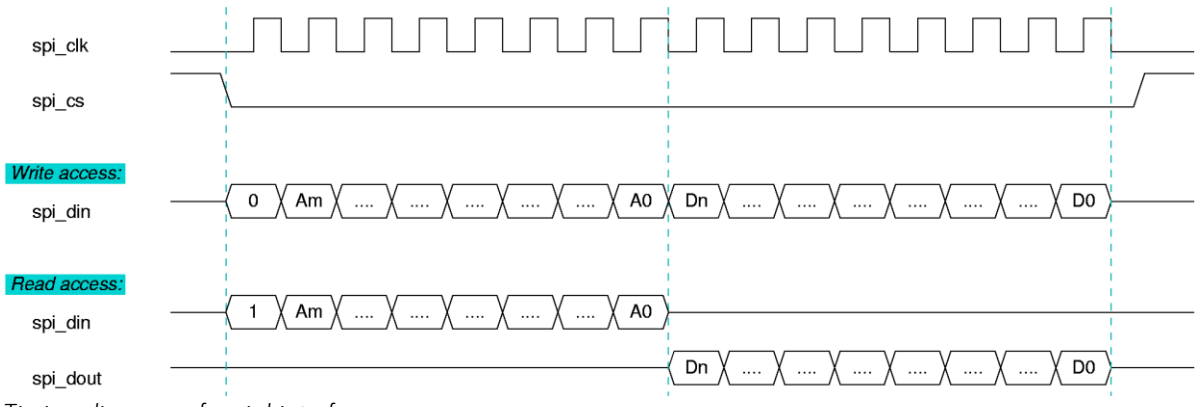
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD}=+5 V, Temp=+25 °C, 50 Ω system.

Parameter		Conditions	Min	Typ	Max	Units
Operation Frequency Range			8		12	GHz
Frequency step			0.1			Hz
Output power		Differential, single ended 3 dB less		+5		dBm
SSB phase noise						
Offset	10 Hz				-70	dBc/Hz
	100 Hz				-80	dBc/Hz
	1 KHz				-90	dBc/Hz
	10 KHz				-95	dBc/Hz
	100 KHz				-100	dBc/Hz
	1 MHz				-120	dBc/Hz
	10 MHz				-140	dBc/Hz
AM Noise		At 5 MHz offset			-115	dBc/Hz
Harmonics					-40	dBc
Reference Spurs					-145	dBc
FOM_{FLOOR}		Complete loop $PN_{FLOOR}=FOM_{FLOOR}+10\log(f_{REF}/Hz)+20\log(f_{RF}/f_{REF})$ with f_{RF} = synthesizer output frequency and f_{REF} = reference input frequency			-225	dBc/Hz
FOM_{FLOOR}		PFD only			-229	dBc/Hz

Timing Diagram and Registers



Timing diagram of serial interface

Control registers (address range "0000" to "1011" registers are read-write).

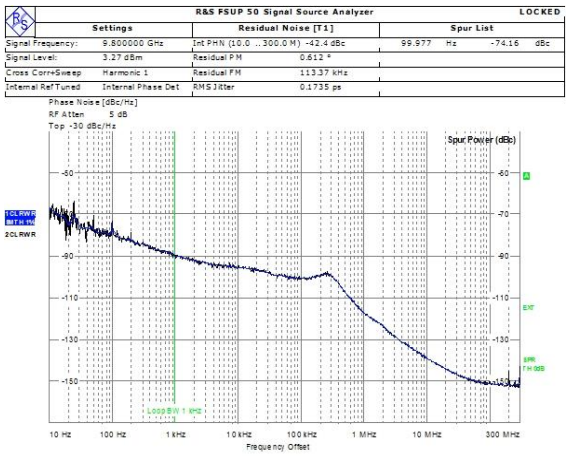
Address	Bit	Name	Function	Default
"0000" Divisor_reg_0	15...0	divisor(35:20)	M/A-counter divisor bits 7...0, -1...-8 Default divider setting is 45.0, with a minimum of 12 and a maximum of 255. The M/A settings are calculated from the programmable integer divider value *D*: $D = 5A+4(M+1-A)$ and $A \leq M + 1$ *A* is calculated from the two LSB of *D* (max. 3) For example results the default divider setting ($D = 45$) in $M = 10$ and $A = 1$	0x2D00
"0001" Divisor_reg_1	15...0	divisor(19:4)	Divisor bits -9...-24	0x0000
"0010" Divisor_reg_2	15...12	divisor(3:0)	Divisor bits -25...-28	"0000"
	11...0	unused		
"0011" Config_reg	15...8	unused		
	7	reset_sd	Low-active reset for Sigma Delta Modulator (SDM)	"0"
	6...5	sd_mux	Number of SDM accumulator stages: "00", "01", "10", "11" = 1, 2, 3, 4	"00"
	4	ref_div_bypass_en	Enable for reference clock bypass switch	"0"
	3...0	ref_div_ctrl	Divisor for reference clock divider (0…15) 0 activates the divider bypass within the reference divider. 1 divides by one.	"0000"
"0100" Preload_reg	15...0	Preload	Preloads first accumulator bits -1...-16	0x0000
"0101" CP_reg	15...14	Unused		
	13...12	cp_test	Test modus for charge pump currents. PFD switched to constant outputs. "01" 'UP' current activated, also PD_up "10" 'DOWN' current and PD_down on "11" both activated, 'UP' and 'DOWN'	"00"
	11	cp_fine_en	Enable for charge pump fine current	"1"
	10	cp_coarse_en	Enable for charge pump coarse current Coarse charge current is 500 µA	"1"
	9...5	cp_fine	Charge pump fine current (*Icpf*) settings MSB 4 mA, 2 mA, 1 mA, 500 µA, 250 µA	"01000"
	4...0	Unused		
"0110" Offset_reg	15...10	Unused		
	9...5	offset_fine	Fine offset current *Iosf* = *n***Icpf*/50; *n* 0…31	"00001"
	4...0	offset_coarse	Coarse offset current setting *Iosc* = *n**100 µA; *n* 0…31	"00001"

Address	Bit	Name	Function	Default
"0111" VCO_reg	15...8	Unused		
	7	ldo_vco_en	Enable for VCO LDO	"1"
	6...3	vco_band_ctrl	Band selection for internal VCO arrays. In the current configuration, 8 bands are used from "0000" (lowest) to "0111" (highest).	"0011"
	2...0	vco_ctrl	VCO control. "000", "001", "010" enables internal low, medium, or high band VCO. "011" enables external VCO path	"000"
Address	**Bit**	**Name**	**Function**	**Default**
"1000" Enable_reg	15...8	unused		
	7	lock_detect_en	Enable for lock detect buffer	"0"
	6	ldo_div_en	Enable for pre-divider LDO	"1"
	5	ldo_buf_en	Enable for VCO output chain LDO	"1"
	4	ldo_amp_en	Enable for output power amplifier LDO	"1"
	3	pfd_vout_en	Enable for PFD voltage output	"0"
	2	pfd_en	Enable for PFD	"1"
	1	div_en	Enable for feedback clock pre-divider	"1"
	0	clk_fb_out_en	Enable for feedback clock output	"0"
"1001" GPO_reg	15...12	Unused		
	11...8	gpo_default_1	General purpose outputs with default "1"	"1111"
	7...4	Unused		
	3...1	gpo_default_0	General purpose outputs with default "0"	"0000"
	0	lockdetectD_en	Enables digital lock detect output buffer	"0"

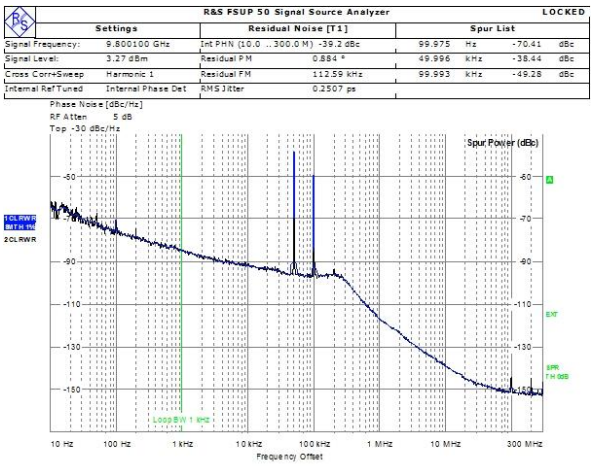
Status registers (address range "1100" to "1111" registers are read-only).

Address	Bit	Name	Function	Default
"1100" Status_reg	15...8	gpi	General purpose inputs	
	7...4	version	Version number, increases on full mask run	"0001"
	3...0	subversion	Subversion number, increases on metal change run	"0000"
"1101" Error_reg	15...11	unused		
	10	lock_detect	PLL lock detect	
	9...0	error_cnt	Triple mode error count	

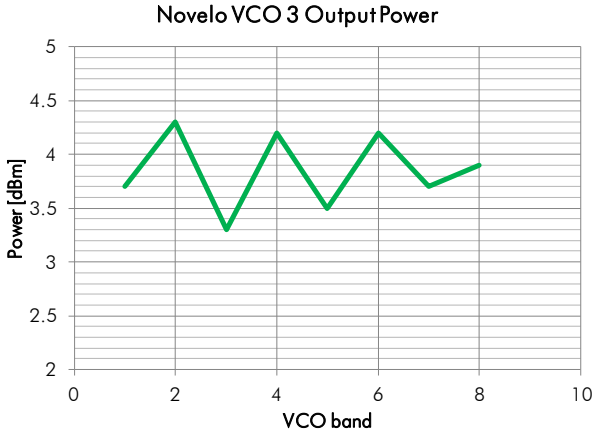
Typical Measurement Results



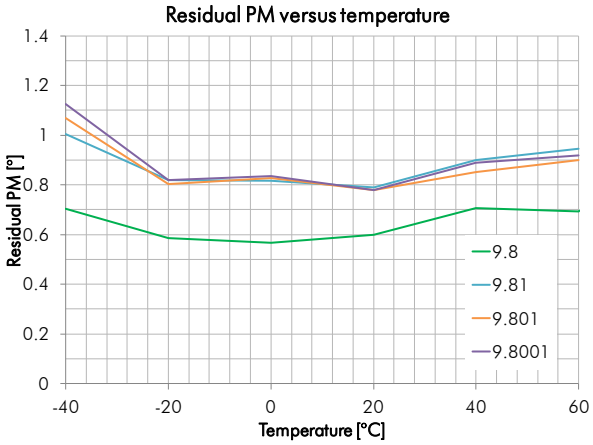
Integer mode performance at 9.8 GHz including all spurs (+20 °C).
Residual phase modulation is 0.6°.



Fractional mode performance at 9.8001 GHz including all spurs (+20 °C).
Residual phase modulation is 0.88°.



NOVELO output power versus VCO band.

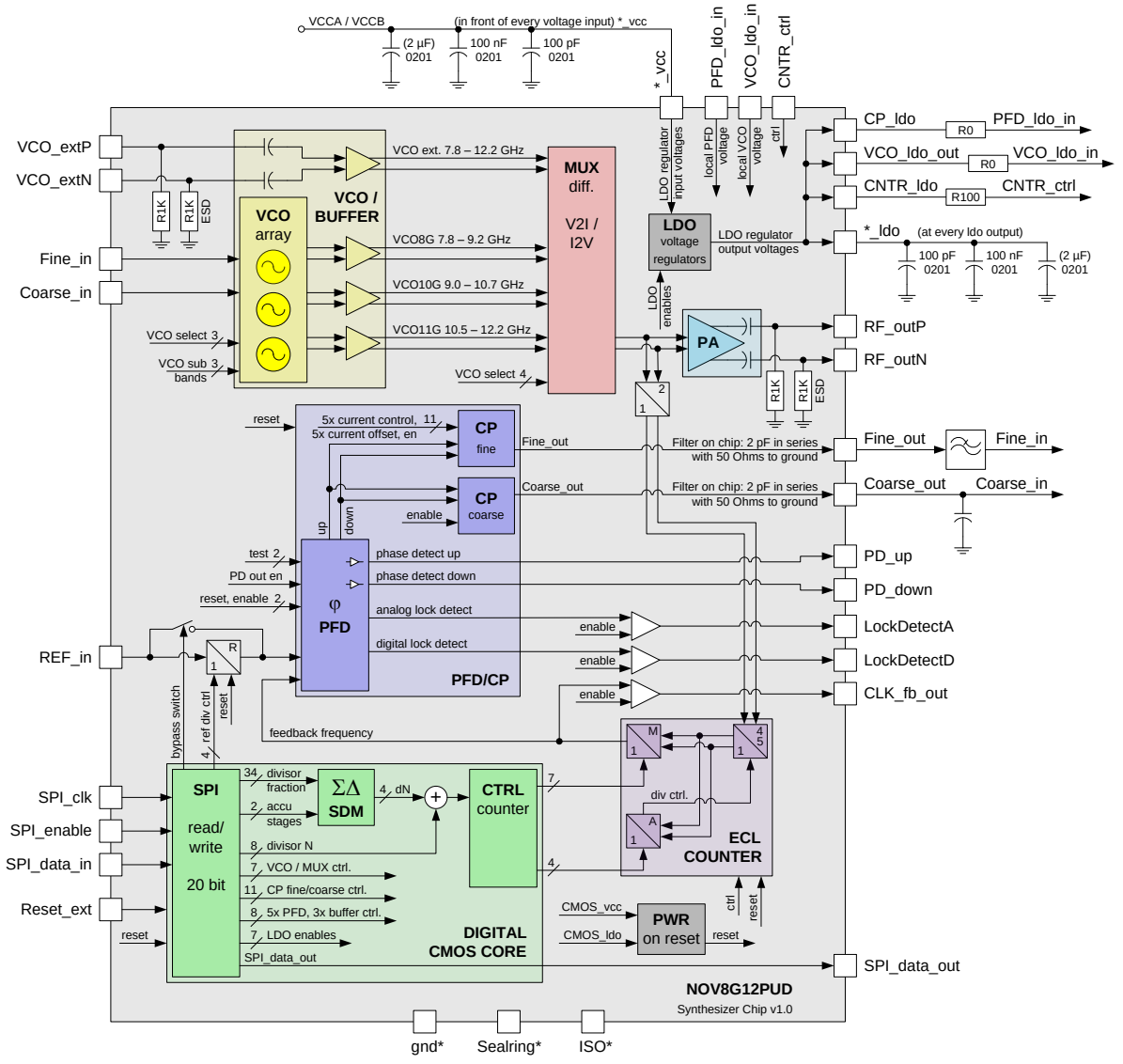


Temperature behaviour of residual phase modulation. Variation is 0.1° over 100 K.

Functional Description and Functional Block Diagram

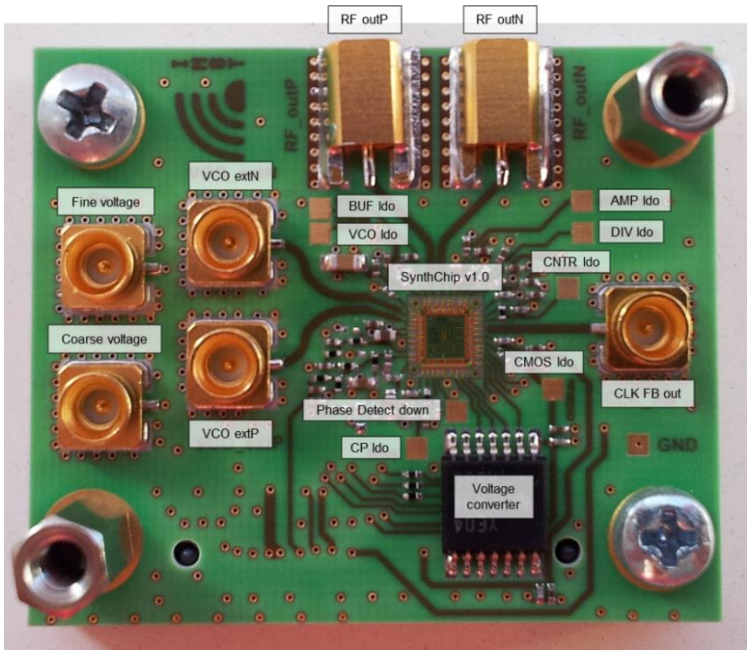
NOV8G12 is a full functional fractional-N synthesizer. The frequency generation is performed internally, by an array of voltage controlled oscillators with 3 VCOs covering the frequency range of 8 to 12 GHz. In parallel, the connection of an external RF source is possible. Via multiplexer, the buffered VCO outputs are connected to the output amplifier and a feedback path with prescaler (divide-by-two circuit) and ECL based 4/5 dual modulus divider in combination with a master and assistant (M/A) counter. The ECL-counter output is feed to a phase frequency detector (PFD), which generates voltage up- and down-pulses depending on the down-divided signal phase compared to the reference frequency phase. The following charge pump (CP) converts these pulses into up- and down-currents, charging external loop filter capacitances. The voltages across the capacitances regulate the VCO output frequency – the loop (PLL) is closed.

The synthesizer can be operated in two modes, integer and fractional. During integer mode, a fixed divider ratio is applied to the divider chain. This way, the output frequency can be adjusted to multiple of divider ratio and reference frequency (e.g. 2*45*100MHz=9GHz). Employing a programmable sigma delta modulator (SDM) based on CMOS logic, dynamic changes of the main divider factor *N* are performed (Gauss distribution). This results in a fractional main divider factor Q with the possibility to access frequencies down to 1 mHz step size at moderate spur and quantization noise levels.

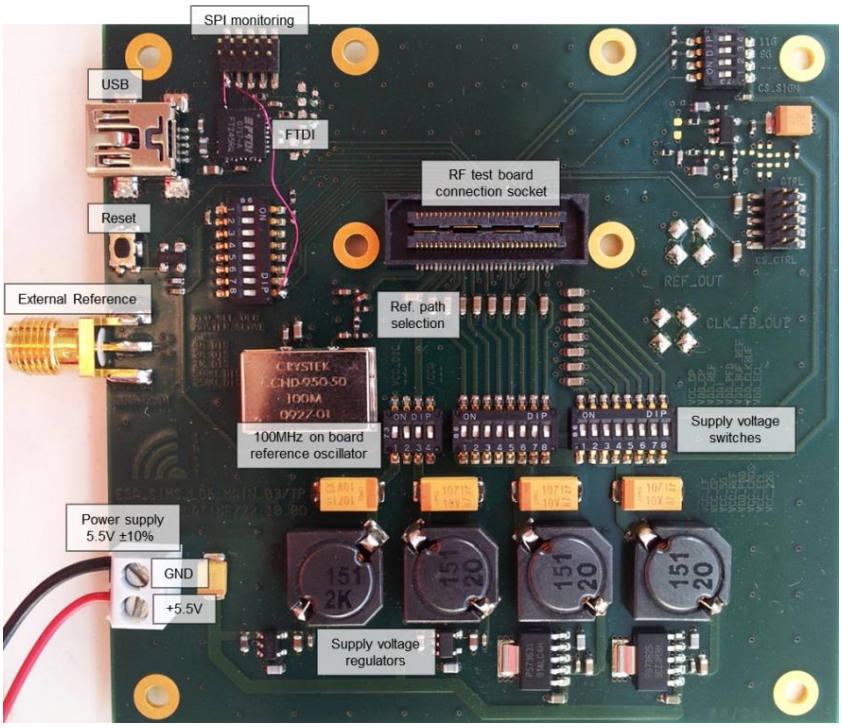


Detailed functional block diagram

NOV8G12EB Evaluation Board



Synthesizer board with connectors



Main board with voltage supply, crystal reference clock and socket for synthesizer board

Bill of Material - NOV8G12EB

Reference Designation	Value
Crystek low phase noise reference clock	100 MHz, -160 dBc/Hz phase noise
Voltage regulators from single +5 V supply	5 V, 3.3 V and 2.5 V
SMD components	Various values (capacitances and resistors for loop filter)
RF connectors	Various

Typical Performance

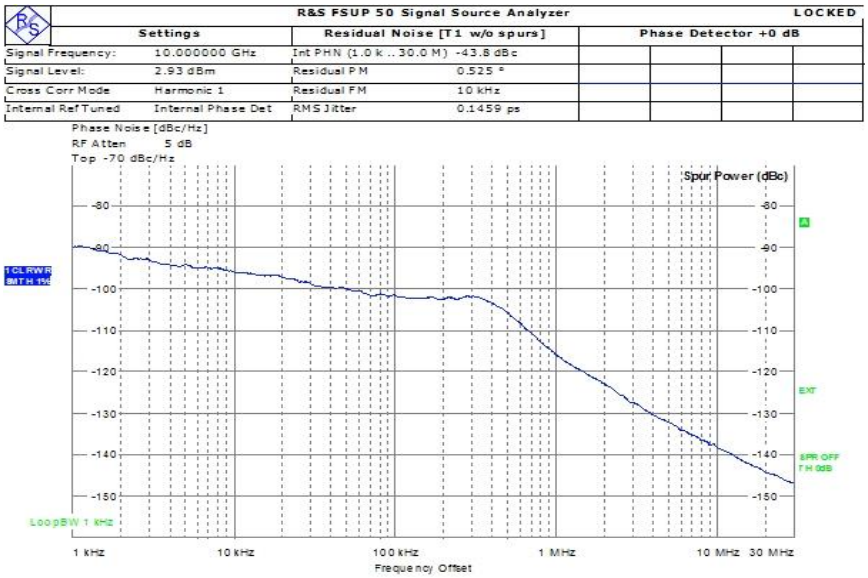
Test conditions unless otherwise noted: V_{DD} = +5 V, Temp = +25 °C, 50 Ω system.

Parameter	Typical Value				Units
Frequency	**8**	**9**	**10**	**12**	**GHz**
Output power[1]	+3	+3	+3	+3	dBm
Phase noise @ 1 MHz offset	-120	-120	-120	-120	dBc/Hz
Power consumption	<1.5	<1.5	<1.5	<1.5	W

Notes:
1. Output power values in the table above include board losses. (approx. =1…2 dB at 12 GHz).

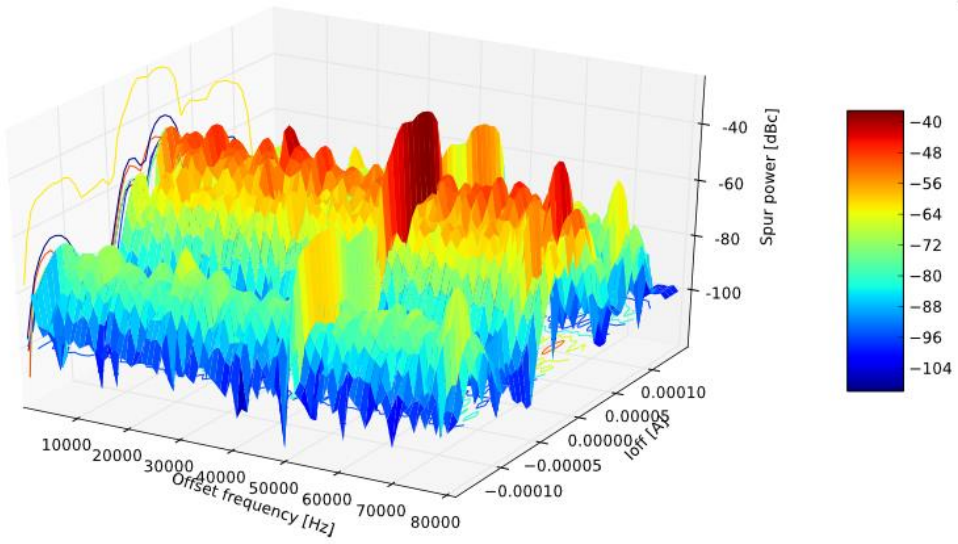
Performance Plots

Test conditions unless otherwise noted: V_{DD} = +5 V, Temp = +25 °C, 50 Ω system.



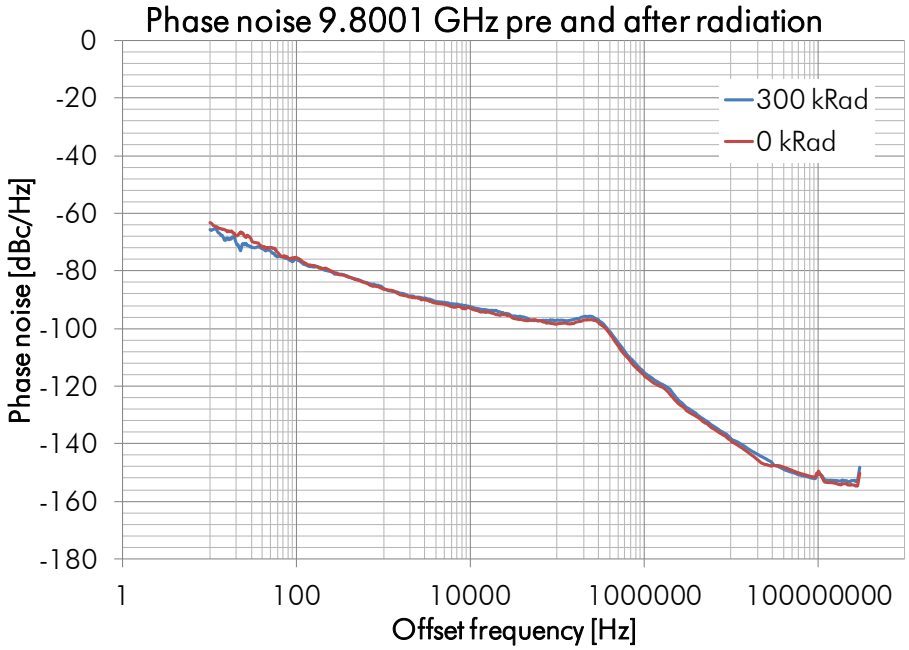
Residual phase modulation at 10 GHz is 0.5°. Optimized loop filter setting and optimized charge pump current/offset current settings.

Simulation Tool



Precise simulation of phase noise and spurs

Radiation Tests

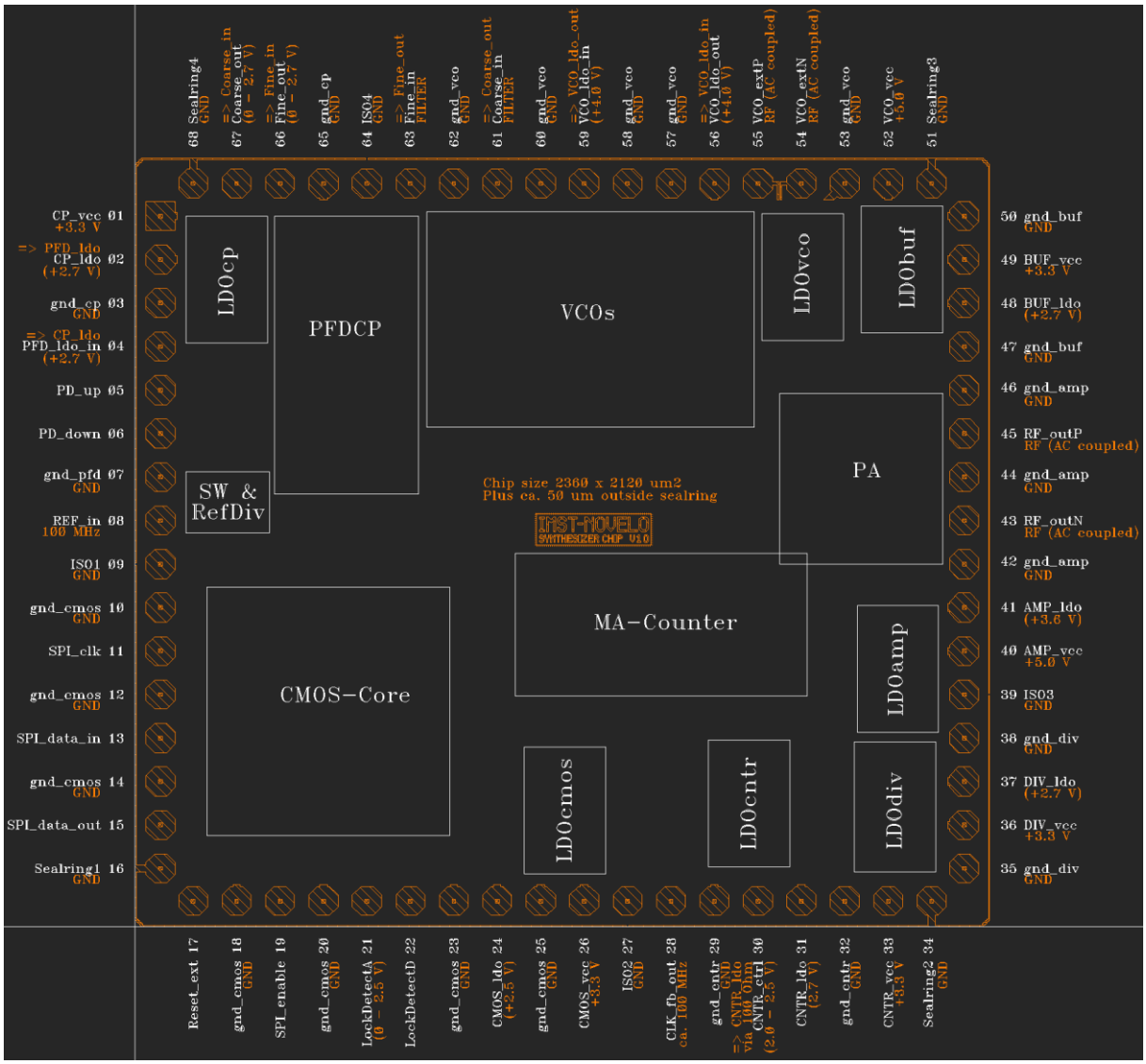


NOVELO fractional mode before (red) and after TID (blue) of 300 kRad.

Evaluation Board PCB Information

Evaluation main board is FR4 multilayer. Evaluation synthesizer board is Rogers multilayer. Evaluation board comes with controlling software (read/write). IMST also offers embedded board web server based software.

Chip Marking and Dimensions



Chip size is 2.46 x 2.22 mm². Pad one (square) is upper left corner (CP_vcc).

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
4. Contact plating: NiPdAu

PCB Mounting Pattern

TBD

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation.
4. Do not remove or minimize via hole structure in the PCB. Thermal and RF grounding is critical.
5. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
6. Ensure good package backside paddle solder attach for best electrical and thermal performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating:	Class 1A
Value:	Passes ≥ 250 V to < 500 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
ESD Rating:	Class IV
Value:	Passes ≥ 1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 3
Test: 260 °C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C maximum reflow temperature) and tin/lead (245 °C maximum reflow temperature) soldering processes.
Contact plating: NiPdAu

RoHs Compliance

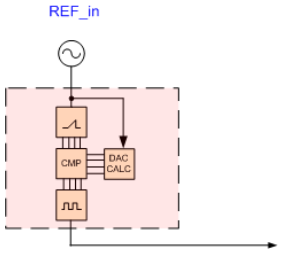
This part is compliant with EU 20M/65/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Product Highlights

- Dual loop concept (coarse and fine regulating loop)
- Complete analog temperature compensation on chip
- 3.6 V resistant SPI I/O pins
- Externally noise filtered voltage regulators on chip
- ESD protection for all pins
- Patented reference generator (WO 2013/167196 A1) in development. This will eliminate all fractional spurs.
- High quality simulation tool available (SpurSIM)
- Programmable charge pump and offset currents (both coarse and fine)
- Chip aspect ratio 1:1 for easy packaging
- 1.5-12 GHz version in preparation (internal VCOs)
- External VCO and external active loop filter possible
- Programmable Delta Sigma modulator (1, 2, 3 or 4 stages)
- No SDM quantization noise
- Noise optimized output multiplexer and amplifier for low RF noise
- On-chip shielded triplate lines and noise shields
- Level shifters between voltage domains



Patented reference generator concept (WO 2013/167196 A1)

Contact Information

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Email: contact@imst.com

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