ΠΑΝΕΠΙΣΤΗΜΙΟ ΠΕΙΡΑΙΩΣ
UNIVERSITY OF PIRAEUS

Embedded Systems Lab (ESLab)
Department of Informatics

SINGLE EVENT UPSETS (SEU) TEST REPORT

Single-Event Upsets Characterization of the 28nm Kintex-7-based Programmable Logic of Xilinx Zynq-7000 FPGA

Radiation Testing Date	15 April 2019
Participants	University of Piraeus/Embedded System Lab, ESA/ESTEC
DUT	Xilinx Zynq-7000 AP SoC XC7Z045-2FFG900
Board	Xilinx ZC706
Radiation type	High Energy Heavy ions (Fe ions)
Accelerator	GSI Helmholtz Centre for Heavy Ion Research
Radiation source	Energy: 230 MeV/c, effective LET 2.29 MeVcm2/mg
Test type	Single Event Upsets (SEUs)

Reference: ESL-TR-1902

Version: 1.0

Date: 1 July 2019

Authors: Vasileios Vlagkoulis, Mihalis Psarakis (University of Piraeus)

Revision History

Version	Date	Authors	Comments
1.0	1 July 2019	V.Vlagkoulis, M.Psarakis	First release for review

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1. Scope

1.1 Scope of the document

This document reports the results of the radiation testing of the 28nm Xilinx Zynq-7000 FPGA device with high-energy heavy ions (Fe) in the **GSI Helmholtz Centre for Heavy Ion Research**.

1.2 References

[1] Single-Event Upsets Characterization of the 28nm Artix-7-based Programmable Logic of Xilinx Zynq-7000 FPGA, SEU TEST REPORT, ESL-TR-1901, June 2019

[2] Vasileios Vlagkoulis et al., “Analysis of the Single Event Upsets in the Programmable Logic of 28 nm Xilinx Zynq-7000 FPGA due to Heavy Ion Irradiation”, Single Event Effects (SEE) Symposium and Military and Aerospace Programmable Logic Devices (MAPLD) Workshop, May 2019.

[3] Amrbar, Mehran, et al. "Heavy ion single event effects measurements of Xilinx Zynq-7000 FPGA." 2015 IEEE Radiation Effects Data Workshop (REDW). IEEE, 2015.

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[9] A. Sari, V. Vlagkoulis and M. Psarakis, “An Open-source Framework for Xilinx FPGA Reliability Evaluation”, Workshop on Open Source Design Automation (OSDA) 2019, Florence, Italy, in conjunction with DATE 2019.

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2. Introduction

This document presents the **Single-Event Upsets (SEUs)** characterization of the **28nm Kintex-7-based Programmable Logic (PL) of a Xilinx Zynq-7000** device due to heavy ion irradiation. All the embedded memories of the PL part of the Xilinx Zynq-7000 device, i.e. Configuration memory (CRAM), Block RAM (BRAM) and user Flip-Flops (FFs), are investigated.

The main target of the experiment is to complete the SEU characterization results reported in [1] for the Xilinx Zynq-7000 device. In [1] an Artix-7-based Xilinx Zynq-7000 device was studied while in the current experiment a Kintex-7-based Xilinx Zynq-7000 device. The purpose of both experiments is to record the Single Bit Upsets (SBUs) and Multiple Cell Upsets (MCUs) of the embedded memories of the PL part due to heavy ion irradiation and calculate their cross section.

A preliminary analysis of the experimental results has been presented in [2].

This work was partially funded by ESA/ESTEC under the purchase order N.5201016857.

3. Test objectives

The main purpose of the radiation test is to analyze in-depth the SEU vulnerability of the PL part of the Xilinx Zynq-7000 FPGA device under heavy ion irradiation and study the feasibility of using Xilinx Zynq-7000 in space applications.

The objectives of the radiation test are:

i) Calculate the cross sections for all the different memory types of the PL part: CRAM, Flip-Flops (FFs), Shift Register LUTs (SRLs) and Block RAMs (BRAMs)

ii) Calculate the cross sections for the essential bits of the CRAM, i.e. including only upsets in the essential bits of the CRAM. Essential bits are the device configuration bits associated with the circuitry of the design

iii) Determine and analyze the Single Bit Upsets (SBUs) and the Multiple Cell Upsets (MCUs) in CRAM

4. Test facility

The radiation tests were performed in the GSI Helmholtz Centre for Heavy Ion Research under heavy ions (Fe) irradiation. The energy of the lead ions was 230MeV/u. The beam arrives at the facility in form of spills of 1s length, with a periodicity of ~3s. A beam size of ~31 mm × 31 mm was set, and the beam flux was around 10^3 ions/cm^2 per spill.

5. Test setup

The FPGA device under test (DUT) is the Xilinx Zynq-7000 SoC device. These devices integrate a processing system (PS) based on a single or dual-core ARM Cortex-A9 CPU and Xilinx programmable logic (PL) in a single device built on a 28nm, high-k metal gate process technology. The PL includes several different types of resources including among others: configurable logic blocks (CLBs), BRAMs, DSP slices, etc. The radiation tests have been performed in an Xilinx ZC706

(see **Figure 1**) which integrates an XC7Z045-2FFG900 Zynq-7000 APSoC device. The PL part of the Xilinx XC7Z045 device is derived from the Xilinx Kintex-7 series technology and is the main target of this study.

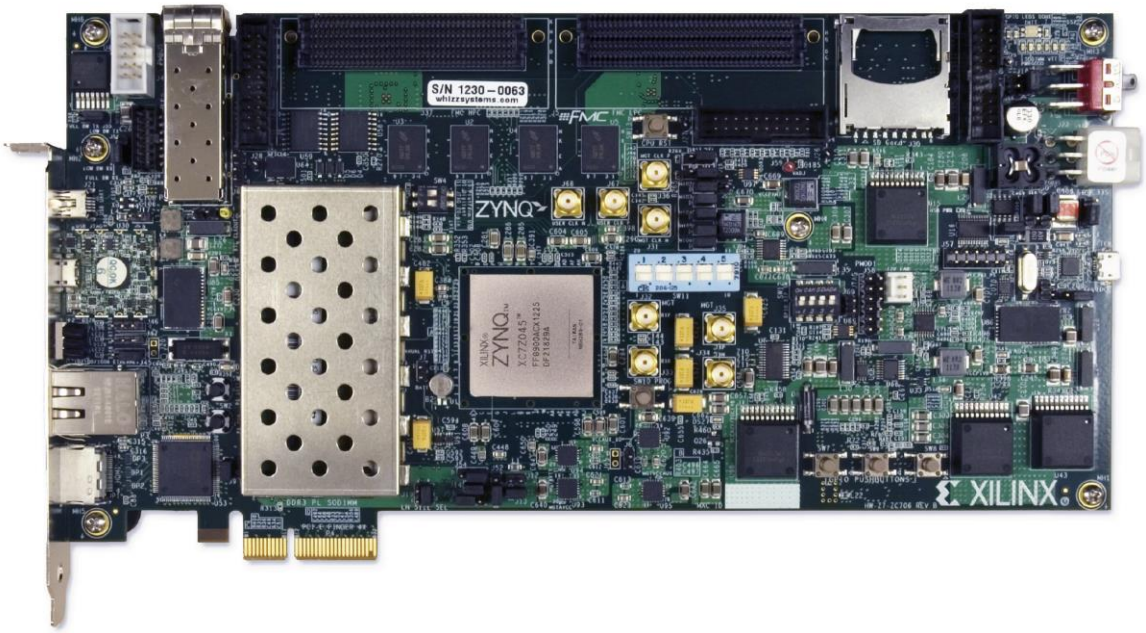

Figure 1: Board under test (Xilinx ZC706)

The test setup is shown in **Figure 2**:

- The Xilinx board is powered by an N6705 power supply which is remotely controlled by the Control Room Laptop 2 (CRL 2).
- The Xilinx board is connected through the JTAG port with the Beam Room Laptop (BRL), for bitstream configuration and readback purposes.
- The BRL is remotely controlled and monitored through Windows Remote Desktop by CRL 1.
- The BRL runs the test_app. Test_app performs FPGA configuration, data acquisition (FPGA readback capture) and logging. More information about the test application running in BRL is given in [1].
- All system clocks were synchronized before the tests with the facility's clock. All instruments' (PSU, BRL, CRLs) logs are time-stamped for post processing.

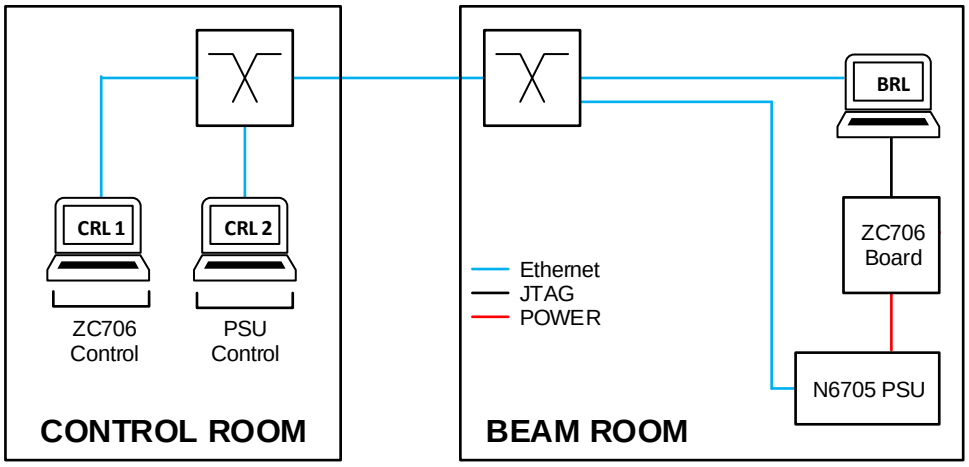

Figure 2: Test setup

Figure 3 photo depicts the Xilinx board connected in the beam room.

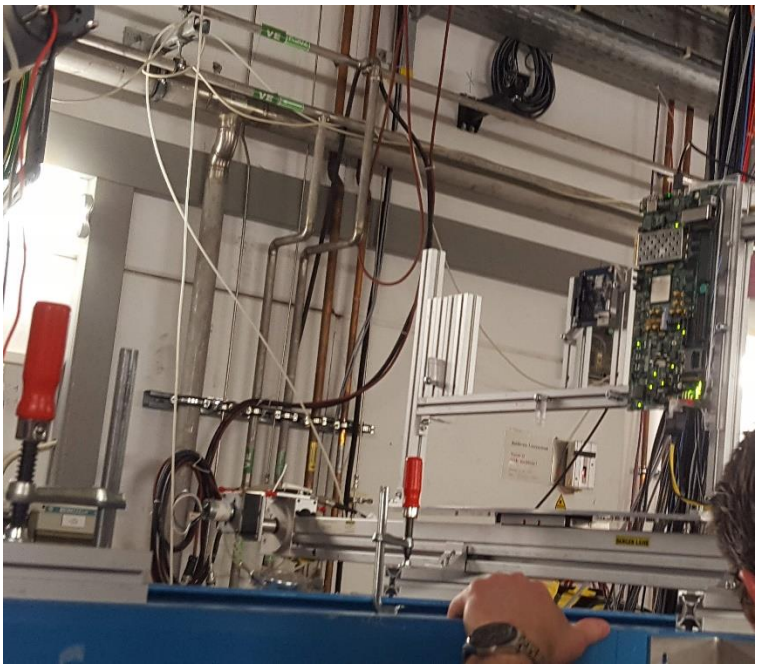

Figure 3: Photo of board under test

6. SEU characterization

The goal of this test is to study the upsets due to heavy ion irradiation in the embedded memories of a Kintex-7-based Xilinx Zynq-7000 device in order to enhance the radiation test results reported in [1] for an Artix-7-based Xilinx Zynq-7000 device. Last years, several studies of the radiation effects in Xilinx Zynq-7000 devices have been presented in the literature. These experiments have investigated the SEUs in the various memories of the device [3],[4],[5],[6], i.e. configuration memory (CRAM) and BRAM of the programmable logic (PL) and caches and on-chip memory (OCM) of the processing system (PS) or the SEE impact in the entire PS area [7]. In [1] we attempted to provide a deeper insight in the SEU vulnerability of the memories of the PL part of device. Therefore, the main differences of the current radiation experiments compared with the one performed in CERN [1] are:

- In CERN we studied an Artix-7-based Xilinx Zynq-7000 device (XC7Z020) while in the current experiment a larger Kintex-7-based Xilinx Zynq-7000 device (XC7Z045).
- In CERN the CRAM readback and reconfiguration tasks were performed during the beam idle periods in order to reduce the possibility to be affected by an SEU or SEFI in the CRAM access logic, while in the current experiment they can be executed anytime. In other words, the CRAM is readback regardless if the beam is off or on and it is re-written to remove upsets after a number of readbacks. This is because in CERN there was a sufficiently long idle period (e.g. 30s) between spills allowing the execution of readback/reconfiguration cycles while in GSI the time distance between spills was 2s.

6.1 Design under test (DUT)

A synthetic, parameterized benchmark has been designed for the purposes of the radiation tests.

- The FPGA DUT communicates with the BRL through the JTAG interface (use of BSCANE2 primitive) as shown in Figure 9 (The figures of Test DUT are included in Appendix).
- The DUT is not clocked during irradiation, so we can capture Single Event Upsets (SEUs) in the user memories of the PL part, i.e. BRAM, SRL and FFs using the Xilinx Readback Capture[1] command. Otherwise (i.e. if the CUT is clocked), upsets in user memory elements would be overwritten by normal circuit operation. Given that the clock is paused, any difference observed in the BRAM, SRL and FFs contents compared to their initial values can be caused by either an SEU in the configuration bits or a single event transient (SET) in the global signals (e.g. Clock or reset) of the corresponding CUT chains.
- All available slices, FFs, BRAMs and DSPs have been instantiated in the CUT as shown in Figure 10. Specifically:

[1] There are two styles of readback: Readback and Readback Capture. During Readback, the configuration memory cells are read, including the current values on all user memory elements (LUT RAM, SRL, and BRAM). Readback Capture is a superset of Readback. In addition to reading all configuration memory cells, the current state of all internal CLB and IOB registers is read, storing all CLB and IOB register values into configuration memory cells. The register values are stored in the same configuration memory cell on which the corresponding register initial values have been programmed, thus sending the GRESTORE/GSR command to the FPGA configuration logic after the Readback Capture can cause registers to return to an unintended state [8].

- All slices are connected in long register chains (see Figure 11 and Figure 12).
    - The SLICEL LUTs are configured as route-through, the SLICEM LUTs are configured as 32-bit Shift Registers LUTs (SRLs) and LUT outputs are connected with CLB FFs to form long register chains.
    - The FFs are preloaded with alternate 0 and 1, while the SRLs with continuous 0s and 1s or alternate 0-1 patterns.
    - Register chain is not clocked (clock signal input is pulled down into the IOB), the CE signal of the FFs and SRLs is connected to '1' (through Routing Static Source - HARD1 of the TIEOFF[2]) and the FFs reset or preset is configured to be asynchronous and pulled-down into the IOB (in CERN [1] the reset was synchronous); this means that transients in the clock and the reset/preset tree can be captured.
- All available BRAMs of the device are instantiated in the CUT (see Figure 13)
    - Initialized with a predefined pattern (to test SEUs in BRAMs), i.e. data are set to all 1s or all 0s or checkerboard values and parity bits to 0s
    - Cascaded through the Data Bus either horizontal (raw) or vertical (column).
    - BRAM chain is not clocked and the WREN/RDEN signals of the BRAMs are connected to '0' (pulled-down into the IOB); this means that upsets in the BRAMs due to transients in the clock tree are unlikely to happen.
- All available DSP slices of the device are instantiated in the DUT (see Figure 14)
    - Connected in cascade mode either horizontal (raw) or vertical (column) -configurable
    - Configured to implement multiply and accumulate (MAC) operation
    - DSP chain is not clocked.

The outcome is a highly utilized and densely routed design (100% slice, BRAM and DSP utilization) (see Figure 15). The following Tables presents details about the configuration bitstream of the CUT.

Table 1: CUT - bits type details

Bit Type	Number of Bits	%
Configuration bits (unmasked)	71.017.108	66.65
CLB FF bits (masked)	437.200	0.41
CLB SRL bits (masked)	4.505.600	4.23
Unknown masked bits	661.116	0.62
BRAM bits (masked)	20.090.880	18.85
Other unused masked bits (PS area or dummy frames)	9.843.904	9.24
Total bits	106.555.808	100.00

[2] The basic primitive in Xilinx FPGAs to supply VCC and GND signals to a design is the TIEOFF. The TIEOFF accompanies every switch matrix and has several connections to all sink connections to its neighboring logic tile (CLB, BRAM, DSP, etc). It has 2 pins, HADR0 (GND) and HADR1 (VCC).

Table 2: CUT – initial bit values

Bit Value	Number of Bits	%
Configuration bits (unmasked) zeros	60.798.772	85.61
Configuration bits (unmasked) ones	10.218.336	14.39
Total Configuration bits (unmasked)	71.017.108	100.00
CLB FF bits (masked) zeros	218.600	50.00
CLB FF bits (masked) ones	218.600	50.00
Total CLB FF bits (masked)	437.200	100.00
CLB SRL bits (masked) zeros	2.252.800	50.00
CLB SRL bits (masked) ones	2.252.800	50.00
Total CLB SRL bits (masked)	4.505.600	100.00
BRAM bits (masked) zeros	11.489.280	57.19
BRAM bits (masked) ones	8.601.600	42.81
Total BRAM bits (masked)	20.090.880	100.00
Unknown & Unused masked bits zeros	10.505.020	100.00
Unknown & Unused masked bits ones	0	0.00
Total Unknown & Unused masked bits	10.505.020	100.00

Table 3: CDUT – Essential bits

Bit Type	Number of Bits	%
Configuration Essential bits	31.295.881	44.07
Configuration Non-Essential bits	39.721.227	55.93
Total Configuration bits	71.017.108	100.00
CLB FF Essential bits	437.200	100.00
CLB FF Non-Essential bits	0	0.00
Total CLB FF bits	437.200	100.00

* All the other bits (SRL, BRAM, unused) are non-essential bits

For test purposes an open-source platform has been developed [9]. The platform provides access to the FPGA configuration memory and circuit logic via the JTAG protocol. It provides a non-intrusive tool to perform various configuration memory functions, such as bitstream readback and verify, configuration frames/registers write and read, etc. For more information about the platform see [1].

6.2 Test flow

The test flow is shown in **Figure 4**.

It performs the following steps:

1. The board ZC706 is configured through the JTAG interface.
2. The BRL reads back the device configuration memory through JTAG using readback-capture and records the readback data. This step is used to record the CRAM configuration data and the content of user state elements (i.e. FFs); given that the CUT is paused during the test, any changes in their content would be due to upsets or SETs in the clock and reset signals (note that reset is asynchronous).

3. The BRL reads all the Configuration Registers according to Table 5-23 of [8] and records the data. This step is used to record the state of the FPGA Configuration Registers such Frame Address Register, Control Register, Status Register in order to find any abnormal register values during the test.
4. The steps 2 and 3 are repeated for N times (10 times for the current test).
5. The FPGA is reconfigured and the Configuration Registers are read in order to record their state after the reconfiguration. In case of success, the test goes to step (2). Otherwise, a power cycle (power-off and power-on) is executed and the test goes to step (1).

All the configuration memory write and readback operations are performed by Vivado TCL scripts using JTAG commands. Note that in contrast with the CERN test [1], the readback/ reconfiguration tasks are performed at any time of the experiment, i.e. regardless if the beam is off or on.

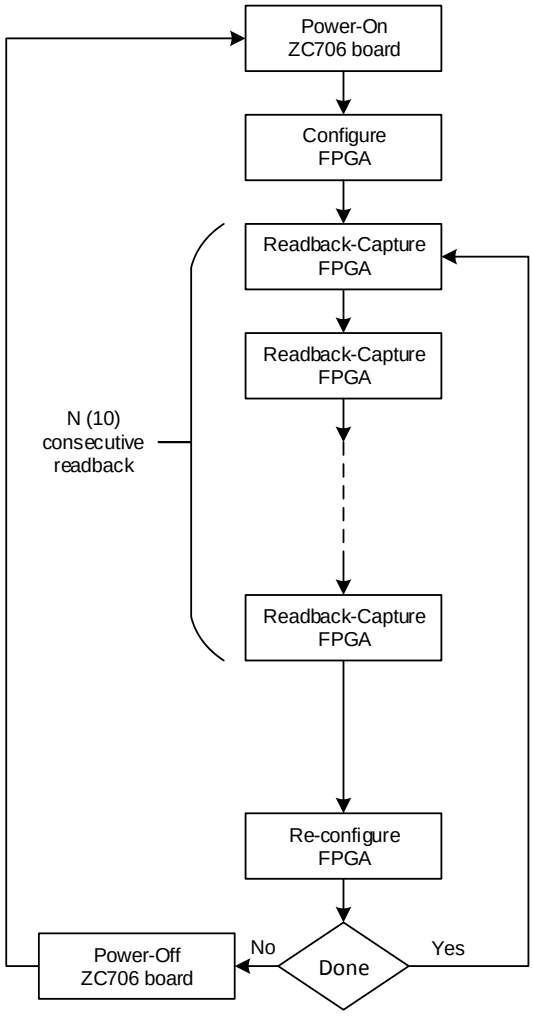

Figure 4: Test flow

The execution times of the FPGA configuration memory access functions (e.g. FPGA memory configuration, readback capture and read configuration registers) used in the test are presented in Table below.

Table 4: Execution time of FPGA Configuration access functions

Configuration access function	Execution time (sec)
FPGA Configuration	5.00
Readback Capture	13.50
Read Configuraton Registers	0.10

Given that the irradiation period is approximately 3 secs (1 secs beam on, 2 secs beam off), the beam is active more than once (4 to 5 times) during the Readback Capture. This means that a Readback Capture records accumulated upsets, which include the upsets recorded by the previous Readback Capture and the upsets occurred during the last irradiation periods.

7. Test results

Test was performed for 0° angle of incidence with an effective LET of 2.29 MeVcm^2/mg.

Table 5: Test sessions

Duration		Angle of incidence (θ)/ Effective LET (MeVcm^2/mg)	Fluence (ions/cm^2)
Start (CET)	End (CET)		
15.04.19 18:06	15.04.19 18:46	0° / 2.29	3.58 x 10^5

7.1 Post-processing software

The Zynq device is divided into two halves, the top and the bottom. All configuration frames in the device have a fixed, identical length of 3,232 bits (101 32-bit words). The configuration frame address is divided into five fields (**Table 6**).

Table 6: Configuration frame address fields

Address fields	Bit index	Description
Block Type	[25:23]	0: Interconnect & Block Configuration (CLB, IOB, DSP, CLK) and FF & LUTRAM values 1: BRAM content 2: CFG_CLB 3: Unknown type (a normal bitstream does not include this type) 4: Unknown type
Top/Bottom	[22]	0: Top 1: Bottom
Row Address	[21:17]	Defines a row of the device. The row addresses start at 0 and increment from center to top and from center to bottom
Column Address	[16:7]	Defines a column of the device. Column addresses start at 0 on the left and increase to the right
Minor Address	[6:0]	Defines a frame within a column

Both the configuration bit file and the readback file (generated using Xilinx Readback commands) include the configuration frames with block type 0 and 1. Xilinx does not provide documentation for the block types 2, 3 and 4. In [10], it is mentioned that the CFG_CLB block type 2 defines which part of the FPGA needs to be reset or reconfigured. It only appears in a partial bitstream, if the RESET_AFTER_RECONFIG attribute has been set for this region.

For the SEU/MCU analysis, a database with all the erroneous bits was created comparing the readback-capture files with the readback-capture golden files. For each bit difference between a readback-capture with the golden file, a database entry is created with the fields shown below. If an error recorded in the current readback-capture, it had been also recorded in the previous readback-capture cycle, then it is not stored in the database because it is an accumulated error. On the other hand, if a bit not be upset in the current readback-capture, it had been recorded as error in the previous readback-capture cycle, then it is stored as error in the database.

Table 7: Test Post-Processing Database fields

Database fields	Valid values	Description
Timestamp		The timestamp of the readback-capture file
Golden Bit value	0 or 1	Bit value of the golden file, e.g. if this bit is 0 then the bit is flipped from 0 to 1
Frame Address	32 bit hex value	Address of the configuration frame of the erroneous bit
Block Type	Interconnect & Block Configuration or Block RAM Content	The value of the frame address bits [25:23] 000: Interconnect & Block Configuration 001: BRAM Content These block types are only included in the readback/readback capture files
Top/Bottom	Top or Bottom	The value of the frame address bit 22 0: Top 1: Bottom
Row Address		The value of the frame address bits [21:17]
Column Address		The value of the frame address bits [16:7]
Minor Address		The value of the frame address bits [6:0]
Word of frame	integer (0 to 100)	The word position in the frame of the erroneous bit
Bit of Word	integer (0 to 31)	The bit position in the word
Bit of Frame	integer (0 to 3231)	The bit position in the frame
Masked Bit	0 or 1	0: The bit is unmasked 1: The bit is masked
Masked Frame	False or True	False: The bit is located into a non-masked frame (at least one bit of the frame is unmasked) True: The bit is located into a masked frame (all the bits of the frame are masked). Such frames are a) the BRAM content (block type 1) frames, b) the dummy frames and the PS area frames of all the block types
Essential Bit	0 or 1	0: The bit is non-essential 1: The bit is essential
Non Essential Frame	False or True	False: The bit is located into a frame which has at least one essential bit True: The bit is located into a non-essential frame (all the bits of the frame are not essential)

Database fields	Valid values	Description
Logic Block	String (SLICE_XnYm or RAMB36_XnYm)	In case of masked bit, this field identifies the specific logic block position (SLICE, RAMB)
Specific Logic	String (e.g. Latch=D5FF.Q or RAM=A:1)	In case of masked bit, this field identifies the specific logic of the above block (FF, SRL bit, BRAM bit)

All the results below are extracted from the database using queries.

7.2 SEU analysis

To analyze the SEUs we studied the effects in four different memory categories: CRAM, BRAM, FFs and SRLs.

7.2.1 CRAM testing

CRAM category includes all the unmasked bits of the configuration bitstream and has been obtained by the analysis of the readback-capture files. Since all these bits are static to the device operation, any upset is supposed to be an SEU (**Table 8**). The CRAM SEUs and the cross section are shown in **Table 9**.

Table 8: CRAM Upsets in a frame

Upsets in a frame	CRAM Bits Occurrences
1	5790
2	64
3	1
16	2

We have also calculated the cross sections considering only the upsets in the essential CRAM bits, as extracted by the Xilinx ebd file, in order to provide a more realistic probability metric of SEUs affecting the CUT behavior.

Table 9: CRAM SEUs

CRAM	**SEUs**	5953
	Cross section [cm2/bit]	2.49×10^{-10}
CRAM Essential	**SEUs**	2935
	Cross section [cm2/bit]	1.23×10^{-10}

In case of the two 16-bit upsets per frame (**Table 8**), these events occurred in two consecutive readbacks. The first readback recorded 16 bits in a frame having erroneous values compared with the golden value and the second readback recorded the same 16 bits in the same frame having

the golden value without performing reconfiguration between these two readbacks (double flip). A similar event (double flip) was also observed in three cases of 1-bit upset per frame. This specific case needs further investigation.

7.2.2 BRAM testing

BRAM category include the masked bits of the configuration bitstream for the BRAM data and has been obtained by the analysis of the readback-capture data. Upsets in these bits are mostly due to SEUs. Given that the CUT clock is paused during the radiation experiments and the CE signal is '0', upsets due to transients in the clock tree or the data busses are unlikely to happen.

Table 10 presents the number of upsets in a frame and the number of occurrences while **Table 11** presents the cross section of the BRAM.

Table 10: BRAM Upsets in a frame

Upsets in a frame	BRAM Bits Occurrences
1	3875
2	103
3	2

Table 11: BRAM SEUs

BRAM	**SEUs**	4087
	Cross section [cm2/bit]	6.05×10^{-10}

7.2.3 Flip-Flop testing

FF and SRL categories include the masked bits of the configuration bitstream for the CLB FFs and shift register LUT data, respectively and have been obtained by the analysis of the readback-capture data. The CUT clock is also paused for the FFs and SRLs, so any upset in these bits compared to their initial values can be caused by either an SEU in the configuration bits or FFs or a single event transient (SET) in the clock net and reset signals of the corresponding CUT chains (remember that all FFs and SRLs are cascaded in long chains).

Table 12: FF + SRL Upsets in a frame

Upsets in a frame	FF Bits Occurrences	SRL Bits Occurrences
1	16	1189
2	-	38
3	-	1
100	1	-

In the case of FFs, a single event was observed that affects several (100) FFs extending in several slices that belong to a physical half-row column (**Table 12**). These FFs – which are the 4 FFs of the SLICEM AFF, BFF, CFF and DFF (**Figure 11**b) of all the 25 Slices of a half-row SLICEM column (SLICE_X136Y75 to SLICE_X136Y99) – were changed to 0. They were configured as FFs with asynchronous preset and they were preloaded with 1s. This means that this phenomenon is not a SET on the preset signal. Furthermore, neither the SLICEM SRLs, which were preloaded with alternate 1-0 pattern, nor the other 4 SLICEM FFs, which were configured with asynchronous preset and preloaded with 0s, were flipped. This means that this phenomenon is not a SET on the clock signal too, assuming that each Slice is connected to a single clock net. The root cause of this phenomenon is currently investigated.

Moreover, five double flips in 1-bit upset per FF frame were also observed, as in the case of CRAM.

In **Table 13**, the SEUs and the cross section of the FFs and the SRLs are presented.

Table 13: FF + SRL Upsets & SEUs

FFs	**Upsets**	116
	SEUs	116
	Cross section [cm2/bit]	7.89×10^{-10}
SRLs	**Upsets**	1268
	SEUs	1268
	Cross section [cm2/bit]	8.37×10^{-10}

The cross section of all the different memory categories of the current test (2.29 $MeVcm^2/mg$ LET) is shown in **Figure 5** along with the cross sections of the radiation test performed in CERN [1] (8.8 and 12.45 MeVcm2/mg LETs).

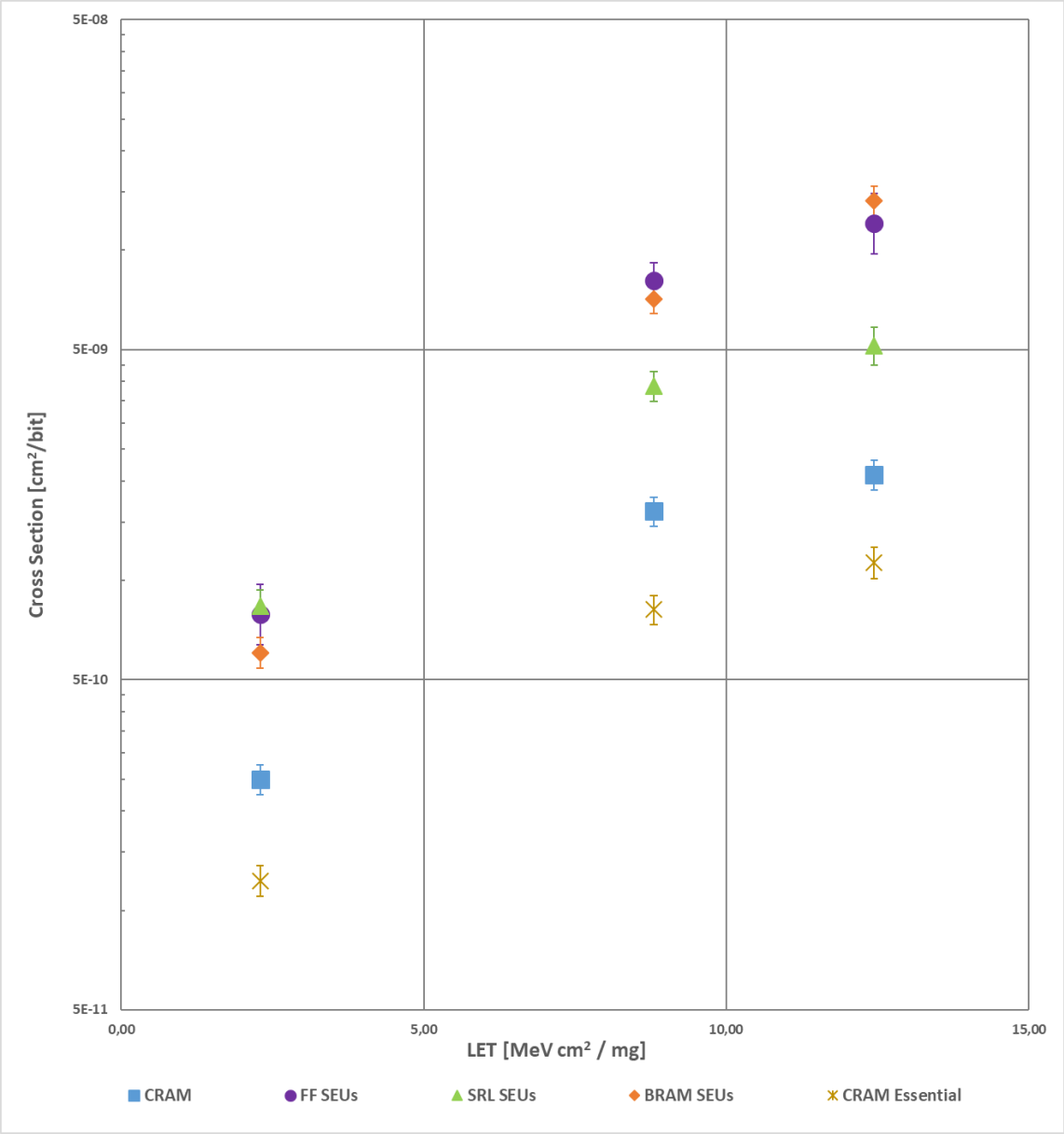

Figure 5: Cross section vs. LET

Notice that we did not observe errors in the FPGA Configuration Registers.

7.2.4 Initial values analysis

Table 14 presents: a) the percentage of the occurrences of the bit flip 0 to 1 and 1 to 0 for all the memory categories (column 3) and b) the ratios of the number of 0-to-1 (1-to-0) upsets/number of bits preloaded with 0 (1) (column 4). For the calculation of the ratios, we took into account the percentage of the initial values for each memory category as shown in **Table 2**.

Table 14: SEU according to bit flip type

Memory Type	Bit Flip Type	% occurrences	Upsets per preloaded bits ratio
CRAM	**0 to 1**	82.70%	0.08×10^{-3}
	1 to 0	17.30%	0.10×10^{-3}
BRAM	**0 to 1**	58.04%	0.20×10^{-3}
	1 to 0	41.96%	0.19×10^{-3}
FFs	**0 to 1**	5.17%	0.03×10^{-3}
	1 to 0	94.83%	0.50×10^{-3}
SRLs	**0 to 1**	50.55%	0.29×10^{-3}
	1 to 0	49.45%	0.28×10^{-3}

Observing the results of the above Table we can conclude that (**Table 15**):

i. for the cases of CRAM and SRLs the likelihood to occur upset in memory cells preloaded with '0' is approximately equal with those preloaded with '1', as also observed in [5] and [1].

ii. For the cases of BRAMs, the likelihood to occur upset in memory cells preloaded with '0' is also approximately equal with those preloaded with '1'

iii. for the cases of FFs, the '1' cells upset more frequently compared to the '0' cells, including the phenomenon described in section 7.2.3, which is under investigation

Table 15: Likelihood to upset 0->1 : 1->0

Memory Category	Likelihood to upset 0->1 : 1-> 0
CRAM	1 : 1.25
BRAM	1 : 0.95
FFs	1 : 16.7
SRLs	1 : 0.97

7.3 MBU/MCU analysis

As shown in **Table 8** most events are single bit upsets (SBUs). However, there is a considerable number of multiple bit upsets (MBUs) (mainly 2-bit upsets per frame). We can assume that when two or more upsets are observed in a frame, they are MBUs, i.e. caused by a single particle. Moreover, we observed multiple upsets expanding in more than one (neighboring) configuration frames called Multiple Cell Upsets (MCUs). We adopted the approach proposed in [5] to identify the MCUs in different frames and described in [1].

Figure 6 presents the patterns (shapes) of the MCUs and their frequency of occurrence. The x-axis of the shapes represents consecutive frame address, while the y-axis consecutive bits in a frame. The total number of SBUs are significantly higher than the number of MCUs. The second and third shapes of the first row prove the bit interleaving scheme adopted in the FPGA configuration memory [5]. For example, the hamming distance of the two upsets of the second shape is (1,1), i.e. the first upset is in the i-bit of the frame j and the second upset is in the i+1-bit of the frame j+1. Note that in the above analysis, only the unmasked bits of the configuration memory have been considered, i.e. that are not dynamically altered by the CUT and possible upsets in these bits can be detected and corrected by a scrubbing mechanism.

The MCU patterns for this LET are similar with the most frequent MCU patterns in [1]. Furthermore, the likelihood of occurrence of N-bits patterns with N > 2 is very low.

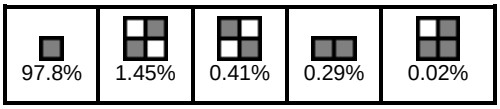

Figure 6: MCU patterns (unmasked bits)

Figure 7 presents the MCUs patterns in case of masked bits. The occurrence of these patterns depends on the CUT, because the masked bit of the configuration memory corresponds to the LUTs used to shape the SRLs and the configuration bits used to preload the FFs.

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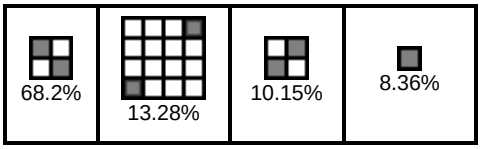


Figure 7: MCU patterns (masked bits)

The above MCU patterns with masked bits confirm the corresponding patterns observed in [1]. Given that for the FFs, SRLs and BRAMs masked configuration bits, the slice/LUT position can be extracted, it is possible to correlate the hamming distances (from the frame/bit logical addresses) of **Figure 7** with the bit positions of SRLs and BRAMs. For example, the relation between the bits of four configuration frames containing the LUTs of a SLICEM and the bits of the four corresponding SRLs is shown in **Figure 8**. Specifically, it shows how the bits 0 to 63 of four consecutive configuration frames (address offsets 0x0, 0x1, 0x2 and 0x3) form four 64-bit SRLs (LUTA, LUTB, LUTC and LUTD). The observation is that the first, second and third MCU shapes of **Figure 7** may occur in two contiguous bits of an SRL (bits of **Figure 8** with red color). For example, the MCU of the first shape may affect the bits 3 and 4 of the LUTA SRL, the MCU of the third shape may affect the bits 31 and 32 of the LUTA SRL and the MCU of the second shape may affect the bits 23 and 24 of the LUTB SRL.

	Frame Address Offset 0x0	Frame Address Offset 0x1	Frame Address Offset 0x2	Frame Address Offset 0x3
Bit 0	LUTA BIT1	LUTA BIT0	LUTA BIT9	LUTA BIT8
Bit 1	LUTA BIT3	LUTA BIT2	LUTA BIT11	LUTA BIT10
Bit 2	LUTA BIT5	LUTA BIT4	LUTA BIT13	LUTA BIT12
Bit 3	LUTA BIT7	LUTA BIT6	LUTA BIT15	LUTA BIT14
Bit 4	LUTA BIT17	LUTA BIT16	LUTA BIT25	LUTA BIT24
Bit 5	LUTA BIT19	LUTA BIT18	LUTA BIT27	LUTA BIT26
Bit 6	LUTA BIT21	LUTA BIT20	LUTA BIT29	LUTA BIT28
Bit 7	LUTA BIT23	LUTA BIT22	LUTA BIT31	LUTA BIT30
Bit 8	LUTA BIT33	LUTA BIT32	LUTA BIT41	LUTA BIT40
Bit 9	LUTA BIT35	LUTA BIT34	LUTA BIT43	LUTA BIT42
Bit 10	LUTA BIT37	LUTA BIT36	LUTA BIT45	LUTA BIT44
Bit 11	LUTA BIT39	LUTA BIT38	LUTA BIT47	LUTA BIT46
Bit 12	LUTA BIT49	LUTA BIT48	LUTA BIT57	LUTA BIT56
Bit 13	LUTA BIT51	LUTA BIT50	LUTA BIT59	LUTA BIT58
Bit 14	LUTA BIT53	LUTA BIT52	LUTA BIT61	LUTA BIT60
Bit 15	LUTA BIT55	LUTA BIT54	LUTA BIT63	LUTA BIT62

	Frame Address Offset 0x0	Frame Address Offset 0x1	Frame Address Offset 0x2	Frame Address Offset 0x3
Bit 16	LUTB BIT1	LUTB BIT0	LUTB BIT9	LUTB BIT8
Bit 17	LUTB BIT3	LUTB BIT2	LUTB BIT11	LUTB BIT10
Bit 18	LUTB BIT5	LUTB BIT4	LUTB BIT13	LUTB BIT12
Bit 19	LUTB BIT7	LUTB BIT6	LUTB BIT15	LUTB BIT14
Bit 20	LUTB BIT17	LUTB BIT16	LUTB BIT25	LUTB BIT24
Bit 21	LUTB BIT19	LUTB BIT18	LUTB BIT27	LUTB BIT26
Bit 22	LUTB BIT21	LUTB BIT20	LUTB BIT29	LUTB BIT28
Bit 23	LUTB BIT23	LUTB BIT22	LUTB BIT31	LUTB BIT30
Bit 24	LUTB BIT33	LUTB BIT32	LUTB BIT41	LUTB BIT40
Bit 25	LUTB BIT35	LUTB BIT34	LUTB BIT43	LUTB BIT42
Bit 26	LUTB BIT37	LUTB BIT36	LUTB BIT45	LUTB BIT44
Bit 27	LUTB BIT39	LUTB BIT38	LUTB BIT47	LUTB BIT46
Bit 28	LUTB BIT49	LUTB BIT48	LUTB BIT57	LUTB BIT56
Bit 29	LUTB BIT51	LUTB BIT50	LUTB BIT59	LUTB BIT58
Bit 30	LUTB BIT53	LUTB BIT52	LUTB BIT61	LUTB BIT60
Bit 31	LUTB BIT55	LUTB BIT54	LUTB BIT63	LUTB BIT62

	Frame Address Offset 0x0	Frame Address Offset 0x1	Frame Address Offset 0x2	Frame Address Offset 0x3
Bit 32	LUTC BIT1	LUTC BIT0	LUTC BIT9	LUTC BIT8
Bit 33	LUTC BIT3	LUTC BIT2	LUTC BIT11	LUTC BIT10
Bit 34	LUTC BIT5	LUTC BIT4	LUTC BIT13	LUTC BIT12
Bit 35	LUTC BIT7	LUTC BIT6	LUTC BIT15	LUTC BIT14
Bit 36	LUTC BIT17	LUTC BIT16	LUTC BIT25	LUTC BIT24
Bit 37	LUTC BIT19	LUTC BIT18	LUTC BIT27	LUTC BIT26
Bit 38	LUTC BIT21	LUTC BIT20	LUTC BIT29	LUTC BIT28
Bit 39	LUTC BIT23	LUTC BIT22	LUTC BIT31	LUTC BIT30
Bit 40	LUTC BIT33	LUTC BIT32	LUTC BIT41	LUTC BIT40
Bit 41	LUTC BIT35	LUTC BIT34	LUTC BIT43	LUTC BIT42
Bit 42	LUTC BIT37	LUTC BIT36	LUTC BIT45	LUTC BIT44
Bit 43	LUTC BIT39	LUTC BIT38	LUTC BIT47	LUTC BIT46
Bit 44	LUTC BIT49	LUTC BIT48	LUTC BIT57	LUTC BIT56
Bit 45	LUTC BIT51	LUTC BIT50	LUTC BIT59	LUTC BIT58
Bit 46	LUTC BIT53	LUTC BIT52	LUTC BIT61	LUTC BIT60
Bit 47	LUTC BIT55	LUTC BIT54	LUTC BIT63	LUTC BIT62

	Frame Address Offset 0x0	Frame Address Offset 0x1	Frame Address Offset 0x2	Frame Address Offset 0x3
Bit 48	LUTD BIT1	LUTD BIT0	LUTD BIT9	LUTD BIT8
Bit 49	LUTD BIT3	LUTD BIT2	LUTD BIT11	LUTD BIT10
Bit 50	LUTD BIT5	LUTD BIT4	LUTD BIT13	LUTD BIT12
Bit 51	LUTD BIT7	LUTD BIT6	LUTD BIT15	LUTD BIT14
Bit 52	LUTD BIT17	LUTD BIT16	LUTD BIT25	LUTD BIT24
Bit 53	LUTD BIT19	LUTD BIT18	LUTD BIT27	LUTD BIT26
Bit 54	LUTD BIT21	LUTD BIT20	LUTD BIT29	LUTD BIT28
Bit 55	LUTD BIT23	LUTD BIT22	LUTD BIT31	LUTD BIT30
Bit 56	LUTD BIT33	LUTD BIT32	LUTD BIT41	LUTD BIT40
Bit 57	LUTD BIT35	LUTD BIT34	LUTD BIT43	LUTD BIT42
Bit 58	LUTD BIT37	LUTD BIT36	LUTD BIT45	LUTD BIT44
Bit 59	LUTD BIT39	LUTD BIT38	LUTD BIT47	LUTD BIT46
Bit 60	LUTD BIT49	LUTD BIT48	LUTD BIT57	LUTD BIT56
Bit 61	LUTD BIT51	LUTD BIT50	LUTD BIT59	LUTD BIT58
Bit 62	LUTD BIT53	LUTD BIT52	LUTD BIT61	LUTD BIT60
Bit 63	LUTD BIT55	LUTD BIT54	LUTD BIT63	LUTD BIT62

Figure 8: SRLs (LUTRAMs) – Configuration Memory mapping

APPENDIX: Test DUT

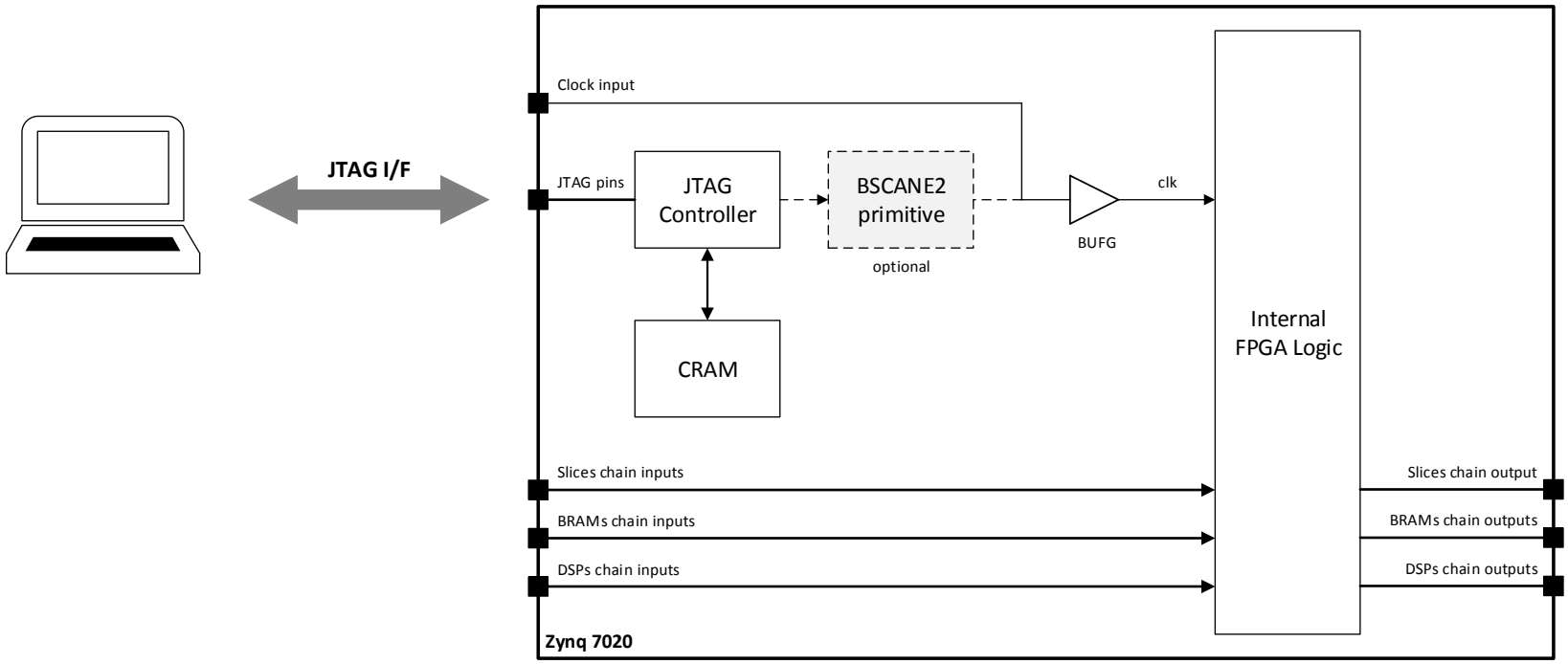


Figure 9: DUT for test setup - Communication between the Host PC and the DUT

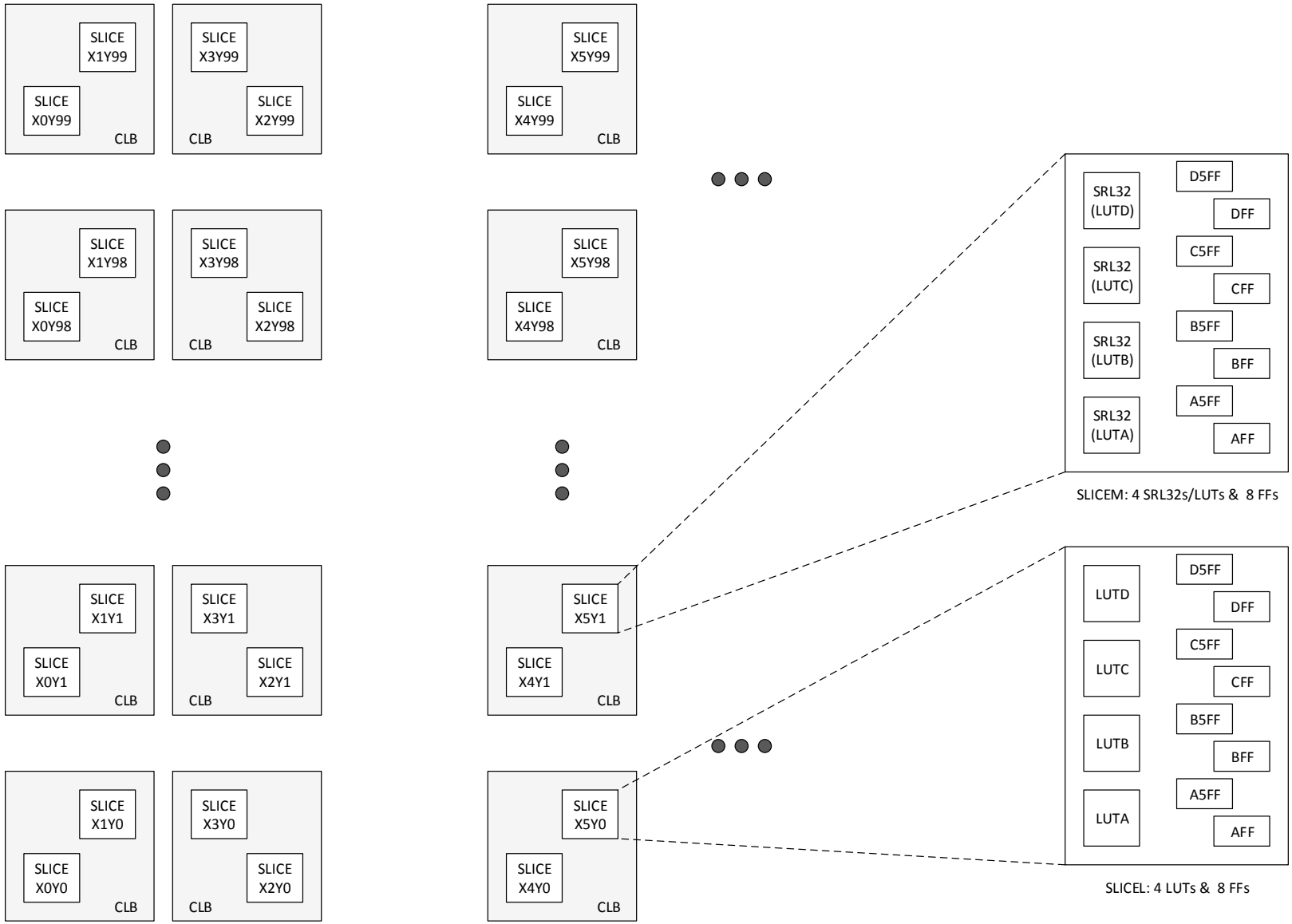
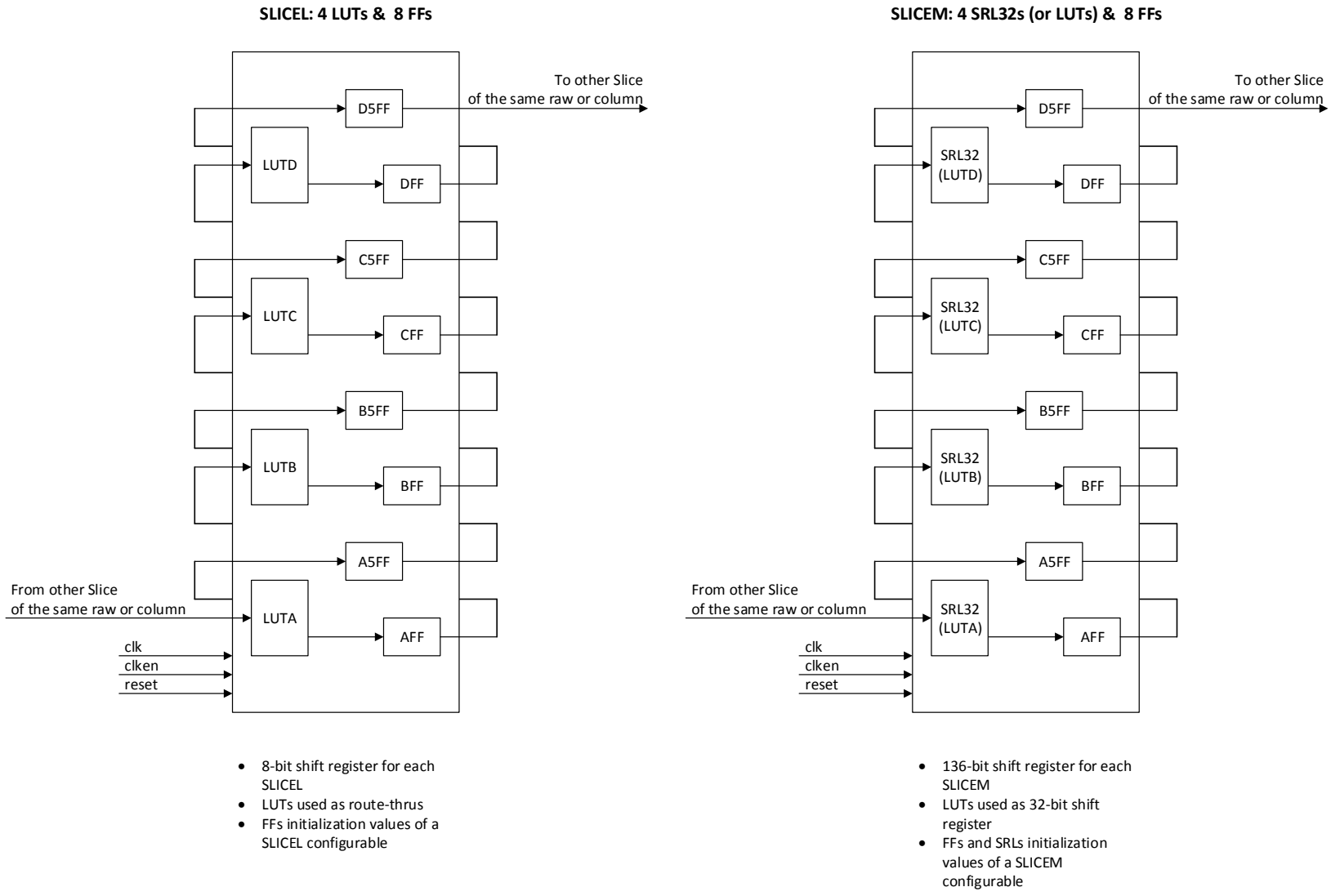


Figure 10: Zynq-7000 CLB architecture (all slices are connected in a row or a column fashion)



- 8-bit shift register for each SLICEL
- LUTs used as route-thrus
- FFs initialization values of a SLICEL configurable

- 136-bit shift register for each SLICEM
- LUTs used as 32-bit shift register
- FFs and SRLs initialization values of a SLICEM configurable

Figure 11: Slice configuration as FF chains

SLICEL: 4 LUTs & 8 FFs

SLICEM: 4 SRL32s (or LUTs) & 8 FFs

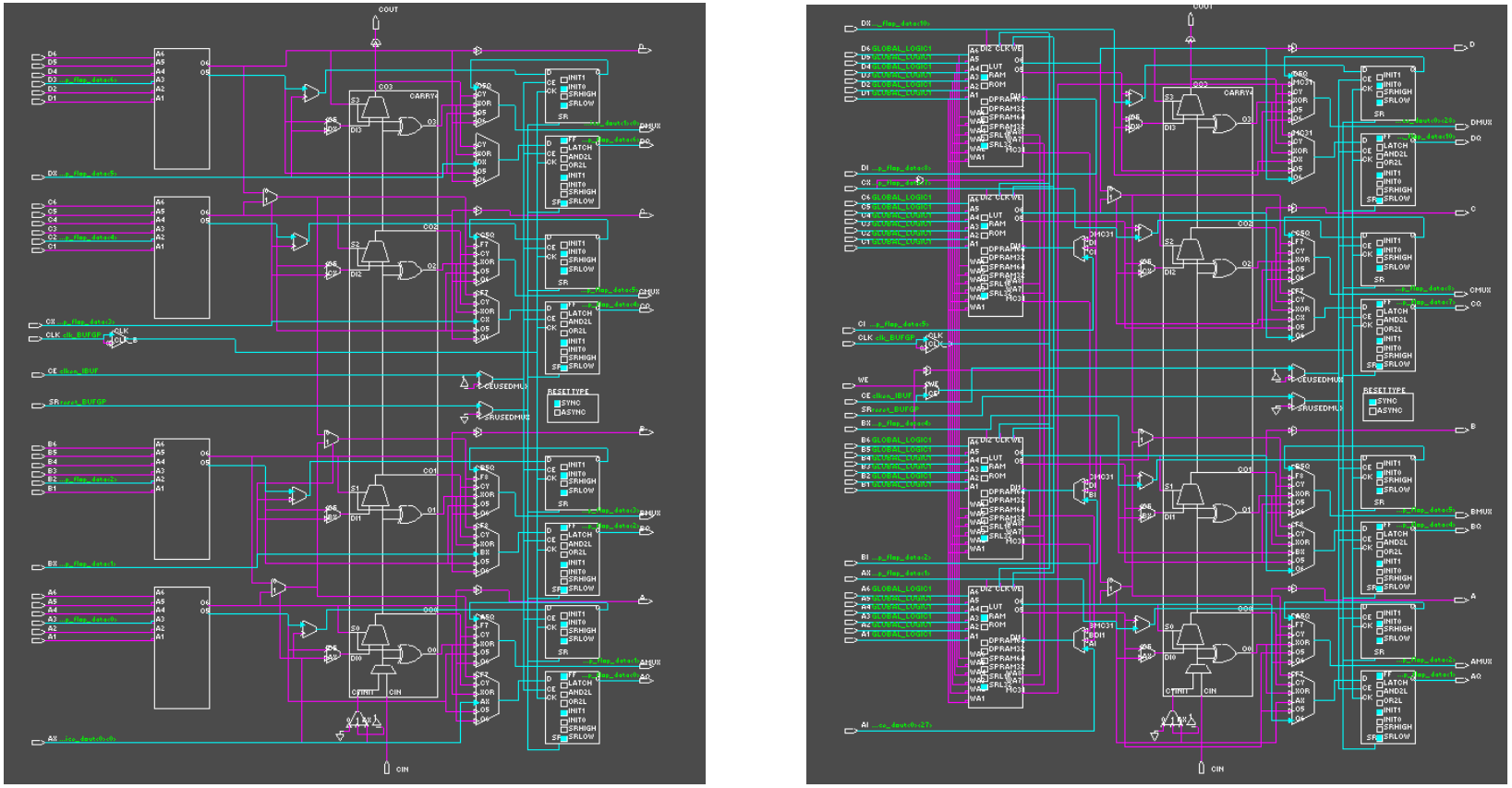
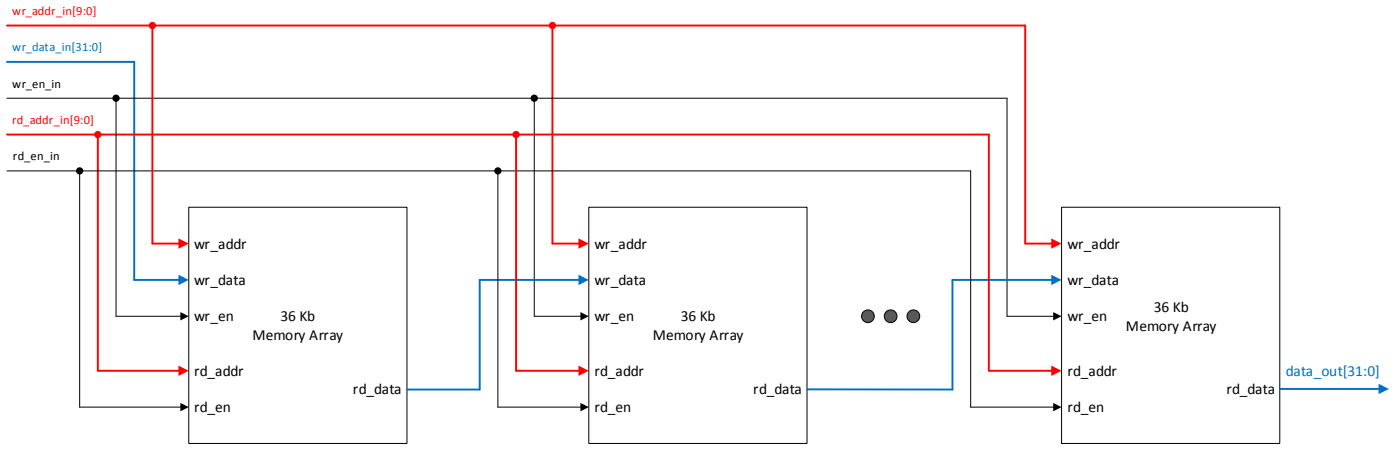
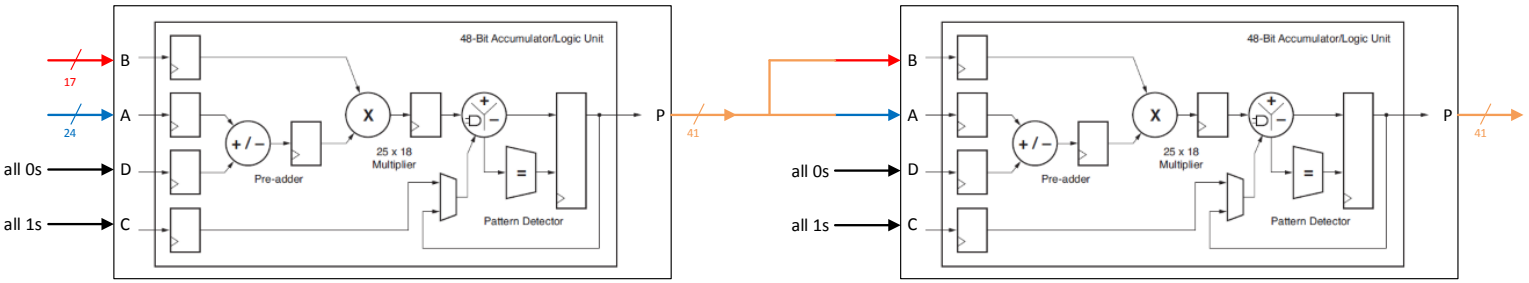


Figure 12: Slice configuration and routing



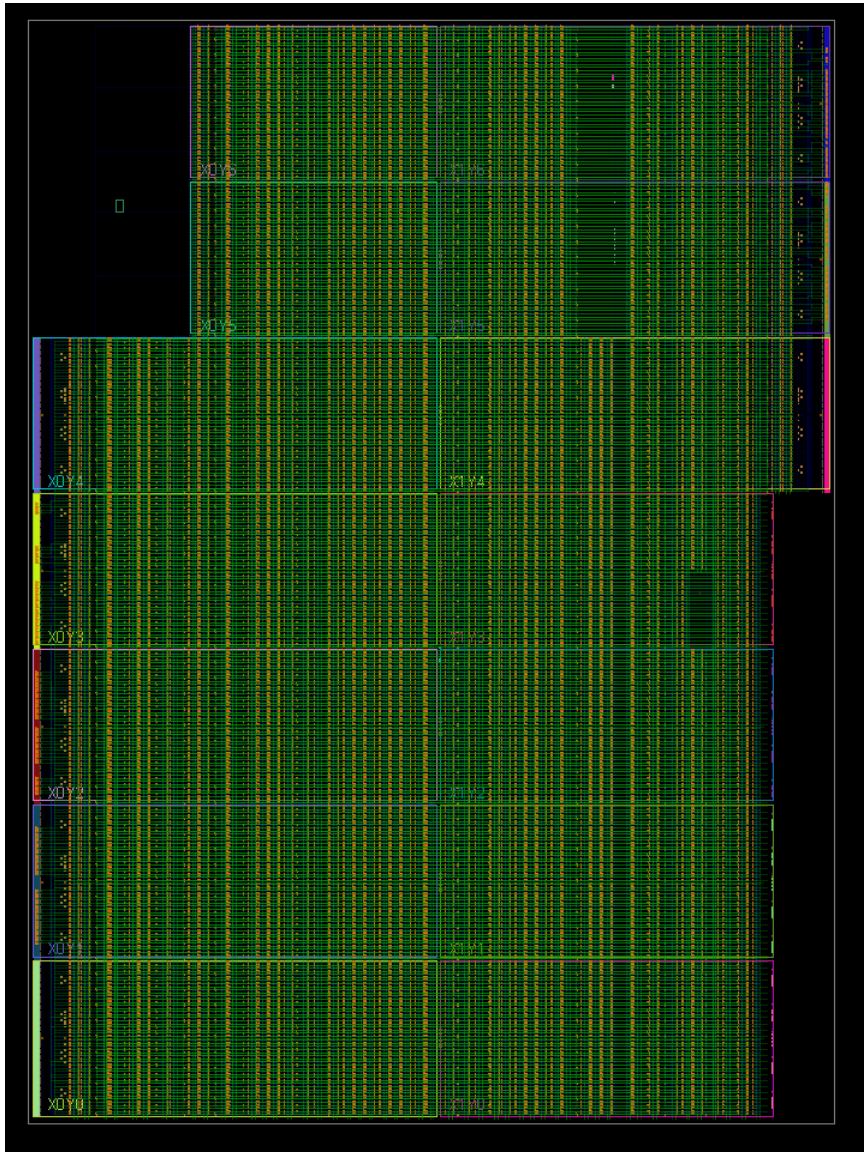
- BRAMs initialized with a predefined pattern
- BRAMs connected in cascade mode through Data Bus either horizontal (raw) or vertical (column) -> configurable
- Each Memory size 1024 x 32 = 32.768 bits (36 Kb)

Figure 13: BRAM configuration and connection in cascade mode



- DSPs connected in cascade mode
- DSPs implement multiplication
- DSPs connected in cascade mode either horizontal (raw) or vertical (column) -> configurable

Figure 14: DSP slices configuration and connection in cascade mode



Resource	Utilization	Available	Utilization %
LUT	70400	218600	32.20
LUTRAM	70400	70400	100.00
FF	437200	437200	100.00
BRAM	545	545	100.00
DSP	900	900	100.00
IO	173	362	47.79
BUFG	3	32	9.38

SLICELs = 37050

LUTs used as Route-Thrus and not as Logic

LUTs = 37050 * 4 = LUTs per SLICEL = 148200

SLICEMs = 17600

SRLs = 17600 * 4 SRLs per SLICEM = 70400

Total SLICEs = 37050 + 17600 = 54650

SLICE FF = 54650 * 8 Regs per Slice = 437200

Figure 15: FPGA resource utilization and routing