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UNIVERSITY OF PIRAEUS

Embedded Systems Lab (ESLab)
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RADIATION TEST REPORT

Single-Event Effects (SEEs) characterization of the Xilinx Zynq-7000 APSoC device under proton irradiation

Radiation Testing Date	10-12 September 2021
Participants	University of Piraeus/Embedded System Lab, ESA/ESTEC
DUT	Xilinx Zynq-7000 AP SoC XC7Z045-2FFG900
Board	Xilinx ZC706
Radiation type	Proton beam
Accelerator	Paul Scherrer Institute (PSI) – PIF
Radiation source	Energy: 30, 50, 100, 150, 200 MeV
Test type	SEUs, SEFIs

Reference: ESL-TR-2101

Version: 2.0

Date: 10 January 2022

Authors: Mihalis Psarakis, Vasileios Vlagkoulis (University of Piraeus)

Revision History

Version	Date	Authors	Comments
1.0	25 Nov 2021	Mihalis Psarakis, Vasileios Vlagkoulis	First release for review
2.0	10 Jan 2022	Mihalis Psarakis	A.Tavoularis comments were addressed Section 8 “Error rates” was added

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1. Scope

1.1 Scope of the document

This document reports the results of the proton radiation tests in the Xilinx Zynq-7000 APSoC device performed at **Paul Scherrer Institute (PSI) - Proton Irradiation Facility (PIF)**.

1.2 References

[1] Single-Event Upsets Characterization of the 28nm Artix-7-based Programmable Logic of Xilinx Zynq-7000 FPGA, SEU TEST REPORT, ESL-TR-1901, June 2019.

[2] Single-Event Upsets Characterization of the 28nm Kintex-7-based Programmable Logic of Xilinx Zynq-7000 FPGA, SEU TEST REPORT, ESL-TR-1902, July 2019.

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[4] Tambara, Lucas Antunes, et al. "On the characterization of embedded memories of Zynq-7000 all programmable SoC under single event upsets induced by heavy ions and protons." 2015 15th European Conference on Radiation and Its Effects on Components and Systems (RADECS). IEEE, 2015.

[5] Greg Allen, et al., Zynq SoC Radiation Test Results and Plans for the Altera MAX10, NEPP Electronic Technology Workshop 2015.

[6] Du, Xuecheng, et al. "Single event effects sensitivity of low energy proton in Xilinx Zynq-7010 system-on chip." Microelectronics Reliability 71 (2017): 65-70.

[7] Lindoso, A., et al. "Evaluation of the suitability of NEON SIMD microprocessor extensions under proton irradiation." IEEE Transactions on Nuclear Science 65.8 (2018): 1835-1842.

[8] Single Event Effects Test Method and Guidelines, ESA ESCC Basic Specification No. 25100 Issue 2, October 2014.

[9] JEDEC Test Method for Beam Accelerated Soft Error Rate, JESD89-3A, November 2007.

[10] Wirthlin, Michael, et al. "A method and case study on identifying physically adjacent multiple-cell upsets using 28-nm, interleaved and SECDED-protected arrays." IEEE transactions on nuclear science 61.6 (2014): 3080-3087.

[11] Xilinx, “Soft Error Mitigation Controller v4.1,” LogicCORE IP Product Guide, PG036, April 2018.

[12] G.Tsiligiannis et al., “Dynamic Test Methods for CTOS SRAMs”, IEEE Transactions on Nuclear Science, vol.61, no.6, p.3095-3102, December 2014.

[13] TRAD OMERE Software, versions 5.5.1. https://www.trad.fr/en/space/omere-software/

2. Introduction

This document presents the Single-Event Upsets (SEUs) characterization of the Xilinx Zynq-7000 APSoC device due to proton irradiation. Both the ARM-based Processing System (PS) and the Programmable Logic (PL) part of Xilinx Zynq-7000 APSoC device were tested. The following embedded memories of the targeted device were monitored for SEUs: L1 Data cache, L2 cache and On-chip memory (OCM) in the PS part and Configuration memory (CRAM), Block RAM (BRAM), LUT RAM and user Flip-Flops (FFs) in the PL part.

The goals of the experiment are: a) to assess the SEU vulnerability of the ARM processor core and the embedded memories of the Xilinx Zynq-7000 SoC and b) to complete the SEU characterization report for the PL part with proton radiation tests; our team has previously performed heavy-ion radiation tests for the programmable resources of the Zynq-7000 device [1], [2]. Providing cross sections for heavy ions and protons, a more accurate estimation of the error rates for the target orbits will be feasible.

This work was partially funded by ESA/ESTEC under the purchase order N. 5001026904.

3. Test objectives

The main objective of the radiation test is to analyze in-depth the SEU vulnerability of the Xilinx Zynq-7000 FPGA device (both the PL and PS part) under proton irradiation and provide useful reliability data for missions using Xilinx Zynq-7000.

The objectives of the radiation test for the PL part are:

i) Calculate the cross sections for all the different memory types: Configuration RAM (CRAM), Flip-Flops (FFs), Shift Register LUTs (SRLs), Distributed RAMs (DRAMs) and Block RAMs (BRAMs).

ii) Determine and analyze the Single Bit Upsets (SBUs) and the Multiple Cell Upsets (MCUs) in CRAM .

The objectives of the radiation test for the PS part are:

i) Calculate the cross sections for all the different memory types: L1 Data cache, L2 cache, and on-chip memory (OCM).

ii) Monitor the impact of radiation-induced errors at the application-level by executing sw benchmarks on the ARM CPU and measuring the cross sections for Silent Data Corruptions (SDC) and system crashes (SEFIs).

4. Test facility

The radiation tests were performed at the Paul Scherrer Institute (PSI) – Proton Irradiation Facility (PIF). The tests were performed under different proton energies: 30 MeV, 50 MeV, 100 MeV, 150 MeV and 200 MeV. The beam spot was rectangular with a size of 4cm × 4cm. The beam flux ranged from 1.8E+07 to 2.0E+08 depending on the proton energy.

5. Test setup

The FPGA device under test (DUT) is the Xilinx Zynq-7000 SoC device. This device integrates a Processing System (PS) based on a dual-core ARM Cortext-A9 CPU and the Xilinx Programmable Logic (PL) in a single device built on 28nm, high-k metal gate process technology. The Arm Cortex-A9 CPUs are the heart of the PS, including an on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces. The radiation tests have been performed in the Xilinx ZC706 development board (see **Figure 1**), which integrates an XC7Z045-2FFG900 Zynq-7000 APSoC device.

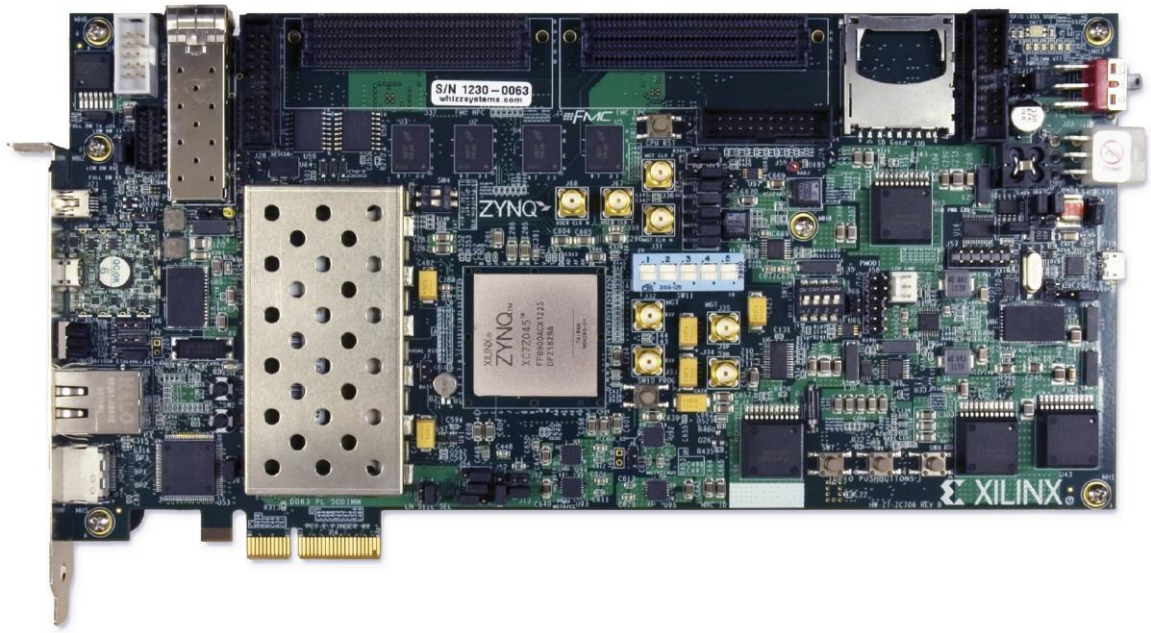


Figure 1: Board under test (Xilinx ZC706)

The test setup is shown in **Figure 2**:

1. The Xilinx board is powered by a DC power supply (Siglent SPD3303X-E) remotely controlled through an Ethernet port by Control Laptop 1.

   Note: During the 2nd day, we encountered problems with the remote connection of the PSU, i.e., frequent loss of connection between laptop and PSU, and we decided to use its USB port for remote control. The PSU was connected through its USB port to Control Laptop 2.

2. The Xilinx board reset line (PS_POR_B) is remotely controlled through a relay module; Control Laptop 1 can set/reset (on/off) the relay module through a USB-to-serial (TTL FTDI) converter. This option is used to reset the device in case of system crashes.

3. A Texas Instrument (TI) USB Interface Adapter is connected through a 10-pin ribbon cable to a PMBus connector to provide access to the onboard TI power controller. The TI Fusion Digital Power Designer tool is running in Control Laptop 2 to monitor the voltage and current values of the chip power rails.

4. Control Laptop 1 is connected with the JTAG port of the Xilinx board for configuration, read-back and logging purposes.

5. Control Laptop 1 is connected through an onboard USB-to-UART bridge with the UART interface of the ARM SoC; ARM CPU uses this connection to send results from the execution of the benchmarks to the host PC.

   Note: For most tests, logging is performed through the PL JTAG port (Xilinx PL TAP); for redundancy reasons, the PS UART interface is also used to send the reports to the host PC.

6. Control Laptop 1 is connected through a USB-to-serial (TTL FTDI) converter with the UART serial interface (RX/TX lines) of the SEM IP core. SEM IP core is integrated into the Zynq-7000 FPGA device to mitigate the SEUs from the CRAM during the execution of the PS tests.

7. Control Laptops 1 and 2 (in the beam room) are remotely controlled and monitored through Windows Remote Desktop by Remote Laptop (in the control room).

8. All system clocks were synchronized before the tests with the facility's clock. All logs are time-stamped for post-processing.

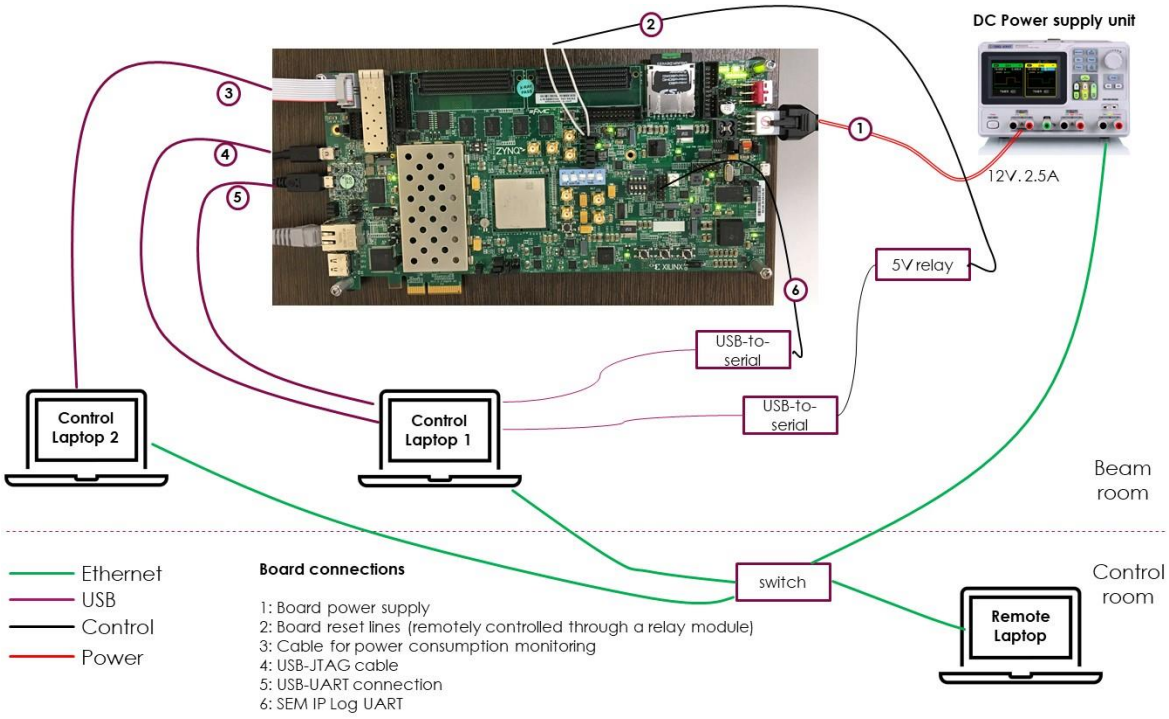


Figure 2: Test setup

Figure 3 photo depicts the Xilinx board connected in the beam room.

Figure 3: Photo of the board in PSI facility

Two different ZC706 boards were used for the tests, Board 1 and Board 2, to avoid board damage due to Total Ionizing Dose (TID). During the experiments, Board 1 received a TID of 117 krad and Board 2 received 58 krad.

6. PL tests

The main objective of these tests was to study the SEU vulnerability of the PL part of the Zynq-7000 device under proton irradiation. Several radiation experiments in the Xilinx Zynq-7000 device have been previously presented in the literature, but in most cases with heavy ions. Our team has performed two heavy-ion radiation experiments at CERN (2018) and GSI (2019) and published detailed results in [1],[2],[3]. The impact of proton radiation has been previously studied in [4],[5],[6],[7]. In [5], the researchers have presented preliminary results for the SEE characterization of the Zynq-7000 device under heavy ions and protons; they have calculated the cross section for the memories (OCM, Caches) of the PS part for a 62 MeV proton energy. In [6], they have performed proton radiation experiments to characterize the SEE sensitivity of both the memories (CRAM, D-cache) and the functional components (ALU, FP unit, DMA) of the Zynq-7000 devices but with a low-energy proton beam (<10 MeV). In [7], they have studied the SEE sensitivity of the SIMD coprocessor of the ARM core (NEON) but again with low energy protons (15.4 MeV). Only in [4], they performed experiments with the full range of proton energies, from 50 MeV to 250 MeV, but they presented results only for the CRAM and the L2 cache. To the best of our knowledge, no results have been presented in the literature for the SEE characterization of the BRAM, FFs and LUT RAMs under proton irradiation.

Therefore, the goal of these experiments was to provide a complete SEE characterization of all the embedded memories of the PL part for the full range of proton energies, from 30 MeV up to 250 MeV.

6.1 Design under test

A synthetic, parameterized benchmark has been designed for the radiation tests of the PL part. The main features of the benchmark are the following:

- FPGA design under test (DUT) communicates with the host PC through the JTAG interface (use of BSCANE2 primitive).
- DUT is not clocked during irradiation, so we can capture Single Event Upsets (SEUs) in the user memories of the PL part, i.e., BRAM, LUT RAMs and FFs using the Xilinx Readback Capture[1] command.
- All available slices, FFs, BRAMs and DSPs have been instantiated in the DUT. Specifically:
    - All slices are connected in long register chains: the SLICEL LUTs are configured as route-through and the LUT outputs are connected with CLB FFs to form long register chains. The FFs are preloaded with alternate 0 and 1, while the SRLs with continuous 0s and 1s or alternate 0-1 patterns.
    - SLICEM LUTs are configured either as 32-bit Shift Registers LUTs (SRLs) or as Distributed RAM (DRAM) (see note below).

[1] There are two styles of readback: Readback and Readback Capture. During Readback, the configuration memory cells are read, including the current values on all user memory elements (LUT RAM, SRL, and BRAM). Readback Capture is a superset of Readback. In addition to reading all configuration memory cells, the current state of all internal CLB and IOB registers is read, storing all CLB and IOB register values into configuration memory cells. The register values are stored in the same configuration memory cell on which the corresponding register initial values have been programmed.

- All available BRAMs of the device are instantiated in the DUT. They are initialized with a predefined pattern (to test SEUs in BRAMs), i.e., data are set to all 1s or all 0s or checkerboard values and parity bits to 0s, and they are cascaded through the Data Bus either horizontal (raw) or vertical (column).
- All available DSP slices of the device are instantiated in the DUT. They are connected in cascade mode, either horizontal (raw) or vertical (column), and configured to implement multiply and accumulate (MAC) operation.

The outcome is a highly utilized and densely routed design (100% slice, BRAM, and DSP utilization). More information about the FPGA hardware benchmark can be found in [1] and [2].

Note: Two hardware benchmarks, namely PL1 and PL2, have been applied for the PL radiation tests: in PL1, the SLICEM LUTs have been configured as 32-bit Shift Registers LUTs (SRLs) while in PL2 as Distributed RAMs (DRAMs). The results from the execution of both benchmarks have been taken into account for the calculation of the SEU cross sections for the CRAM, BRAM and FFs, while the results of PL1 for the cross section of LUT SRL and the results of PL2 for the cross section of LUT DRAM.

Table 1 presents details about the configuration bitstream of the benchmarks.

Table 1: CUT - bits type details

Bit Type	Number of Bits	%
Configuration bits (unmasked)	71.017.108	66.65
CLB FF bits (masked)	437.200	0.41
CLB SRL/DRAM bits (masked)	4.505.600	4.23
Unknown masked bits	661.116	0.62
BRAM bits (masked)	20.090.880	18.85
Other unused masked bits (PS area or dummy frames)	9.843.904	9.24
Total bits	106.555.808	100.00

For test purposes, an open-source platform has been developed [2]. The platform provides access to the FPGA configuration memory and circuit logic via the JTAG protocol. It provides a non-intrusive tool to perform various configuration memory functions, such as bitstream readback and verify, configuration frames/registers write and read, etc.

6.2 PL test flow

The flow of PL tests is shown in **Figure 4**.

It performs the following steps:

1. Board ZC706 is configured through the JTAG interface.

[2] https://github.com/unipieslab/FREtZ

2. Host PC reads back the device configuration memory (CRAM) through the JTAG port using readback-capture and records the readback data. This step is used to record the CRAM data and the contents of the user state elements (i.e. FFs); given that the CUT is paused during the tests, any changes in the data stored in user memory would be due to upsets or SETs in the clock and reset signals (note that reset is asynchronous).
3. Host PC also reads all the Configuration Registers and records the data. This step is used to record the state of the FPGA Configuration Registers such Frame Address Register, Control Register, Status Register in order to find any abnormal register values during the tests.
4. Steps 2 and 3 are repeated for N times (N equals 10 for the current test).
5. FPGA is reconfigured and the Configuration Registers are read to record their state after the reconfiguration. In case of success, the test goes to step (2). Otherwise, a power cycle (power-off and power-on) is executed and the test goes to step (1).

All the configuration memory write and readback operations are performed by Vivado TCL scripts using JTAG commands.

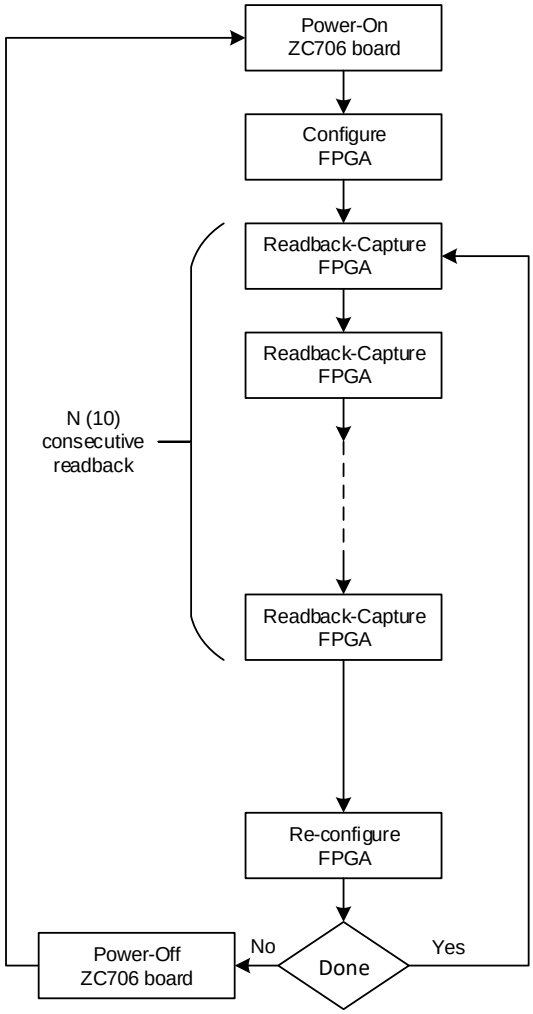


Figure 4: PL test flow

The execution times of the FPGA configuration memory access functions (e.g. FPGA memory configuration, readback capture and read configuration registers) used in the test are presented in **Table 2**.

Table 2: Execution time of the FPGA configuration memory access functions

Configuration memory access function	Execution time (sec)
FPGA Configuration	7.80
Readback Capture	16.50
Read Configuration Registers	0.10

6.3 PL test results

The following test sessions were performed for the PL part. It must be noted that all the inactive periods of the tests (e.g., during device resets or host application initialization) have been removed from the total fluence, and thus, from the calculation of the cross sections in the following sections.

Table 3: PL test sessions

Bench	Board	Energy [MeV]	Duration [in secs]	Flux [p/cm^2/sec]	Fluence [p/cm^2]
PL-1	Board-1	30	263	3.803E+07	1.000E+10
PL-2	Board-1	30	237	4.230E+07	1.003E+10
PL-1	Board-2	50	529	3.784E+07	1.963E+10
PL-2	Board-2	50	528	3.793E+07	1.964E+10
PL-1	Board-2	100	546	3.667E+07	1.963E+10
PL-2	Board-2	100	526	3.809E+07	1.965E+10
PL-1	Board-1	150	302	3.321E+07	1.003E+10
PL-2	Board-1	150	234	4.274E+07	1.000E+10
PL-1	Board-1	200	1087	2.422E+07 to 1.947E+08	4.946E+10
PL-2	Board-1	200	1029	4.865E+07	4.929E+10

6.3.1 Post-processing software

For the SEU analysis, a database with all the memory cell upsets has been created comparing the readback-capture files with the readback-capture golden files. More information about this database can be found in [1] and [2].

All the results below are extracted from this database using queries.

6.3.2 SEU analysis

To analyze the SEUs, we studied the effects in five different memory categories: CRAM, BRAM, FFs, LUT SRLs and LUT DRAMs.

6.3.2.1 CRAM testing

CRAM category includes all the unmasked bits of the configuration bitstream and has been obtained by analyzing the readback-capture files. Since all these bits are static to the device operation, any upset is supposed to be an SEU (**Table 4**). The CRAM SEUs and the cross section are shown in **Table 5**.

Table 4: CRAM Upsets in a frame

Upsets in a frame	CRAM Bits Occurrences				
	30 MeV	50 MeV	100 MeV	150 MeV	200 MeV
1	2223	10440	11789	6593	31892
2	73	514	751	521	2758
3	5	88	159	98	602
4	3	18	26	28	182
5		2	7	6	59
6	2	4	5		17
7		4		1	8
8			4	4	3
9		1			
10		1	1		3
11		1			1
12	1		1		2
13		1			
14			1		2
15			1		
16			1		1
18		1			3
20		2	1		1
22					1
24			1		
26					1
33					2

Table 5: CRAM SEUs

Energy [MeV]	Fluence [p/cm^2]	CRAM SEUs	CRAM cross section per device [cm^2]	CRAM cross section per bit [cm^2/bit]
30	2.003E+10	2417	1.207E-07	1.699E-15
50	3.928E+10	11950	3.043E-07	4.284E-15
100	3.929E+10	14080	3.584E-07	5.047E-15
150	2.003E+10	8110	4.049E-07	5.701E-15
200	9.874E+10	41128	4.165E-07	5.865E-15

6.3.2.2 BRAM testing

BRAM category includes the masked bits of the configuration bitstream for the BRAM data and has been obtained by analyzing the readback-capture data. Upsets in these bits are mostly due to SEUs. Given that the CUT clock is paused during the radiation experiments and the CE signal is '0', upsets due to transients in the clock tree or the data busses are unlikely to happen. As mentioned in Section 6.1 BRAMs are cascasded through the Data Bus. The address lines of all BRAM are set to 0. Thus, a SET that will cause an unexpected write transaction will result to writing the value of BRAM i - location 0 to BRAM i+1 - location 0. Given that each BRAM is initialized with different patterns, we can identiy if such a write transaction has corrupted the data of a BRAM. Such behavior was not observed in the experiments.

Table 6 presents the SEU cross section of the BRAM.

Table 6: BRAM SEUs

Energy [MeV]	Fluence [p/cm^2]	BRAM SEUs	BRAM cross section per device [cm^2]	BRAM cross section per bit [cm^2/bit]
30	2.003E+10	1124	5.612E-08	2.489E-15
50	3.928E+10	4242	1.080E-07	4.790E-15
100	3.929E+10	4616	1.175E-07	5.211E-15
150	2.003E+10	2643	1.320E-07	5.852E-15
200	9.874E+10	13655	1.383E-07	6.134E-15

6.3.2.3 Flip-Flop, LUT SRL and LUT DRAM testing

Flip-flop (FF), LUT SRL and LUT DRAM categories include the masked bits of the configuration bitstream for the CLB FFs, the Shift Register LUT (SRL) data and the Distributed RAM (DRAM) LUT data, respectively, and have been obtained by analyzing the readback-capture data. It must be noted that the CUT clock is paused for the FFs, LUT SRLs and LUT DRAM. So, any upset in these bits compared to their initial values can be caused by either an SEU in the configuration bits or FFs or a single event transient (SET) in the clock net and reset signals of the corresponding CUT chains (remember that all FFs, SRLs and DRAM are cascaded in long chains).

In **Table 7** and **Table 8**, the SEUs and the cross section of the FFs, LUT SRLs and LUT DRAMs are presented.

Table 7: FF SEUs

Energy [MeV]	Fluence [p/cm^2]	FF SEUs	FF cross section per device [cm^2]	FF cross section per bit [cm^2/bit]
30	2.003E+10	27	1.348E-09	3.083E-15
50	3.928E+10	129	3.284E-09	7.512E-15
100	3.929E+10	181	4.607E-09	1.054E-14
150	2.003E+10	91	4.543E-09	1.039E-14
200	9.874E+10	530	5.367E-09	1.228E-14

Table 8: LUT SRL and LUT DRAM SEUs

Energy [MeV]	Fluence (PL-1)	LUT SRL SEUs	LUT SRL cross section per device [cm^2]	LUT SRL cross section per bit [cm^2/bit]	Fluence (PL-2)	LUT DRAM SEUs	DRAM cross section per device [cm^2]	LUT DRAM cross section per bit [cm^2/bit]
30	1.000E+10	209	2.090E-08	4.639E-15	1.003E+10	227	2.263E-08	5.023E-15
50	1.963E+10	980	4.992E-08	1.108E-14	1.964E+10	929	4.729E-08	1.050E-14
100	1.963E+10	1063	5.414E-08	1.202E-14	1.965E+10	981	4.992E-08	1.108E-14
150	1.003E+10	575	5.733E-08	1.272E-14	1.000E+10	542	5.420E-08	1.203E-14
200	4.946E+10	2909	5.882E-08	1.305E-14	4.929E+10	2838	5.758E-08	1.278E-14

The SEU cross sections for all the different memory categories and proton energies are shown in **Figure 5**. For calculating the error bars, we assumed a Poisson distribution of the SEUs, confidence level 95%, and uncertainty on the measured fluence 10% [8],[9].

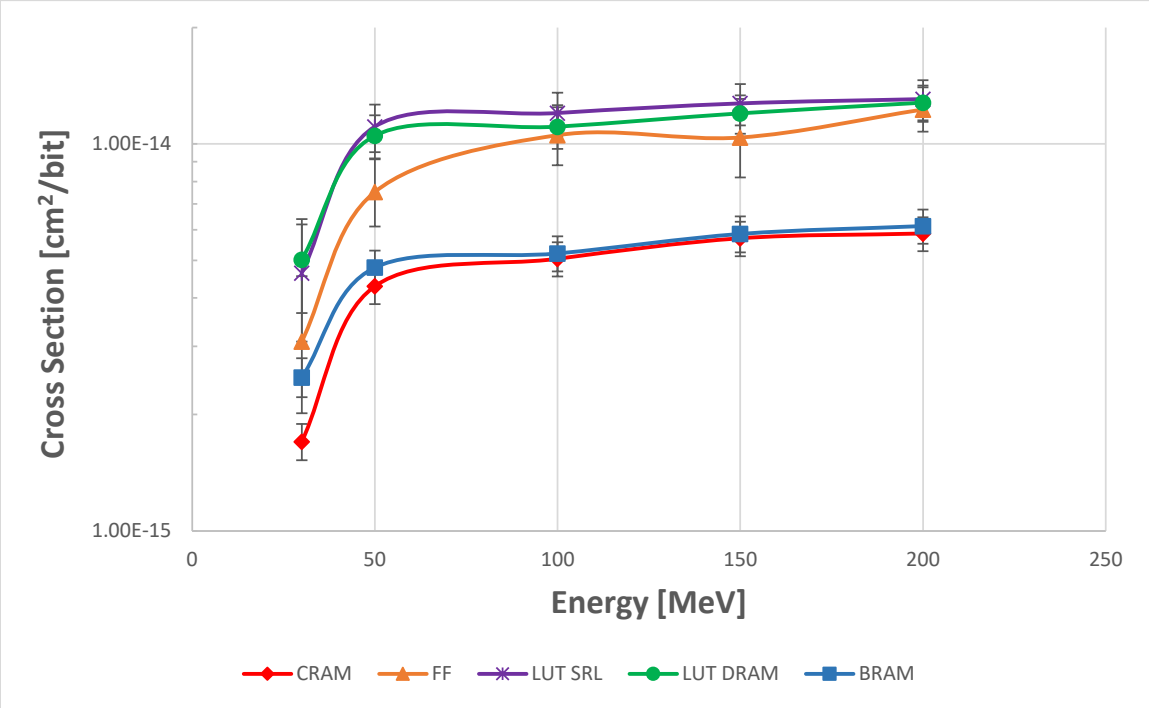


Figure 5: PL memories SEU cross section vs. proton energies

Comments for the SEU analysis:

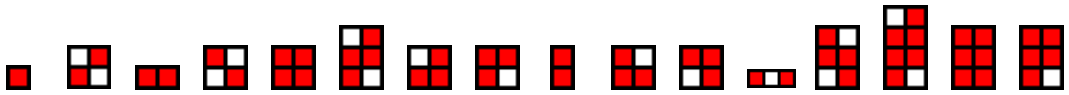
1. Our proton radiation tests show one order of magnitude higher cross section for the CRAM compared to the literature, e.g. in [4] CRAM SEU cross section saturates at ~6.0E-15 instead of ~6.0E-16.

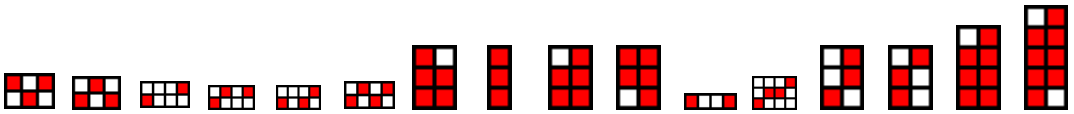
2. It is the first time that proton radiation results are presented in the literature for FFs and SLICEM LUTs.
3. FF, LUT SRL and LUT DRAM cross sections are higher than CRAM cross section.

6.3.3 MCU analysis

As shown in **Table 4** most events are single bit upsets (SBUs). However, there is a considerable number of multiple bit upsets (MBUs). We can assume that when two or more upsets are observed in a frame, they are MBUs, i.e., caused by a single particle. Moreover, we observed multiple upsets expanding in more than one (neighboring) configuration frame, so called Multiple Cell Upsets (MCUs). We adopted the approach proposed in [10] to identify the MCUs in different frames. More details about our MCU identification approach can be found in [1].

In the following, we analyze the MCU patterns (shapes) observed in the CRAM for different proton energies. **Figure 6** and **Figure 7** presents the MCU patterns (first line of the tables) and their number and frequency of occurrence per energy, respectively. The x-axis of the shapes represents consecutive frame addresses, while the y-axis consecutive bits in a frame.

																
200 MeV	16569	4303	2032	517	298	288	241	216	204	163	154	147	70	67	48	48
150 MeV	3347	872	447	88	64	60	44	42	37	36	22	32	14	3	8	10
100 MeV	6113	1705	718	150	59	87	63	65	67	50	43	40	29	23	12	16
50 MeV	5950	1529	497	164	28	82	50	44	46	21	24	18	25	23		2
30 MeV	1434	291	69	28		15	8	9	9	3			4	1		1

																
200 MeV	48	47	44	43	41	41	39	38	34	32	27	24	24	22	22	21
150 MeV	12	12	8	9	10	11	7	11	9	4	3	2	2	4	4	2
100 MeV	15	19	10	9	8	12	6	16	9	6	10	6	9	9	2	8
50 MeV	2	4	4	4		4	3	13	11	2			3			2
30 MeV				1				1	1				1	1		

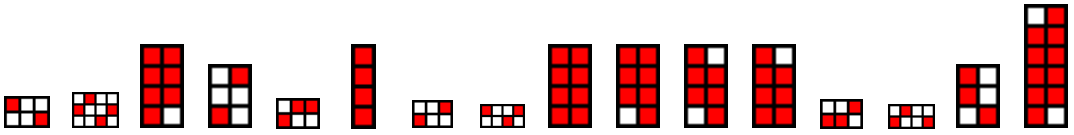
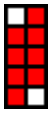
																
200 MeV	19	18	17	15	15	14	13	12	12	12	11	10	10	9	9	8
150 MeV	3	8		1	8	6	2	2		4			4	6	2	2
100 MeV	4	5	3	2	6	4	2	3			4		2	5	2	
50 MeV	2		2	2		2					3		1	2		
30 MeV			1						1							

Figure 6: MCU patterns in CRAM (total number)

																
200 MeV	63.0	16.4	7.73	1.97	1.13	1.09	0.92	0.82	0.77	0.62	0.59	0.56	0.27	0.25	0.18	0.18
150 MeV	63.1	16.4	8.43	1.66	1.21	1.13	0.83	0.79	0.70	0.68	0.42	0.60	0.26	0.06	0.15	0.19
100 MeV	65.6	18.3	7.71	1.61	0.63	0.93	0.67	0.70	0.72	0.54	0.46	0.43	0.31	0.25	0.13	0.17
50 MeV	69.4	17.8	5.79	1.91	0.33	0.96	0.58	0.51	0.54	0.24	0.28	0.21	0.29	0.27		0.02
30 MeV	76.3	15.5	3.67	1.49		0.80	0.43	0.48	0.48	0.16			0.21	0.05		0.05

																
200 MeV	0.18	0.18	0.17	0.17	0.16	0.16	0.15	0.15	0.13	0.12	0.10	0.09	0.09	0.08	0.08	0.08
150 MeV	0.23	0.23	0.15	0.17	0.19	0.21	0.13	0.21	0.17	0.07	0.06	0.04	0.04	0.07	0.07	0.04
100 MeV	0.16	0.20	0.11	0.10	0.09	0.13	0.06	0.17	0.10	0.06	0.11	0.06	0.10	0.10	0.02	0.09
50 MeV	0.02	0.05	0.05	0.05		0.05	0.03	0.15	0.13	0.02			0.03			0.02
30 MeV				0.05				0.05	0.05				0.05	0.05		

																
200 MeV	0.07	0.07	0.07	0.06	0.06	0.05	0.05	0.05	0.05	0.05	0.04	0.04	0.04	0.03	0.03	0.03
150 MeV	0.06	0.15		0.02	0.15	0.11	0.04	0.04		0.07			0.07	0.11	0.04	0.04
100 MeV	0.04	0.05	0.03	0.02	0.06	0.04	0.02	0.03			0.04		0.02	0.05	0.02	
50 MeV	0.02		0.02	0.02		0.02					0.03		0.01	0.02		
30 MeV			0.05						0.05							

Figure 7: MCU patterns in CRAM (percentage)

Note that only the unmasked bits of the configuration memory have been considered in the above analysis, i.e., that are not dynamically altered by the CUT. This means that possible upsets in these bits can be detected and corrected by a scrubbing mechanism. The highlighted patterns are the MBU patterns that the Xilinx SEM IP core is not able to correct. Notice that Xilinx SEM IP in enhanced repair mode [11] supports the correction of single-bit or adjacent double-bit errors per frame, while it cannot correct MBUs with multiplicity higher than two.

The number of uncorrectable - by SEM IP core - MBUs and their cross sections for different proton energies are shown in **Table 9** and **Figure 8**.

Table 9: Uncorrectable (by SEM IP) MBUs

Energy [MeV]	Fluence	Uncorrectable (by SEM IP) MBUs	Cross section per device [cm^2]	Cross section per bit [cm^2/bit]
30	2.003E+10	6	2.996E-10	4.218E-18
50	3.928E+10	63	1.604E-09	2.259E-17
100	3.929E+10	109	2.775E-09	3.907E-17
150	2.003E+10	70	3.495E-09	4.921E-17
200	9.874E+10	433	4.385E-09	6.175E-17

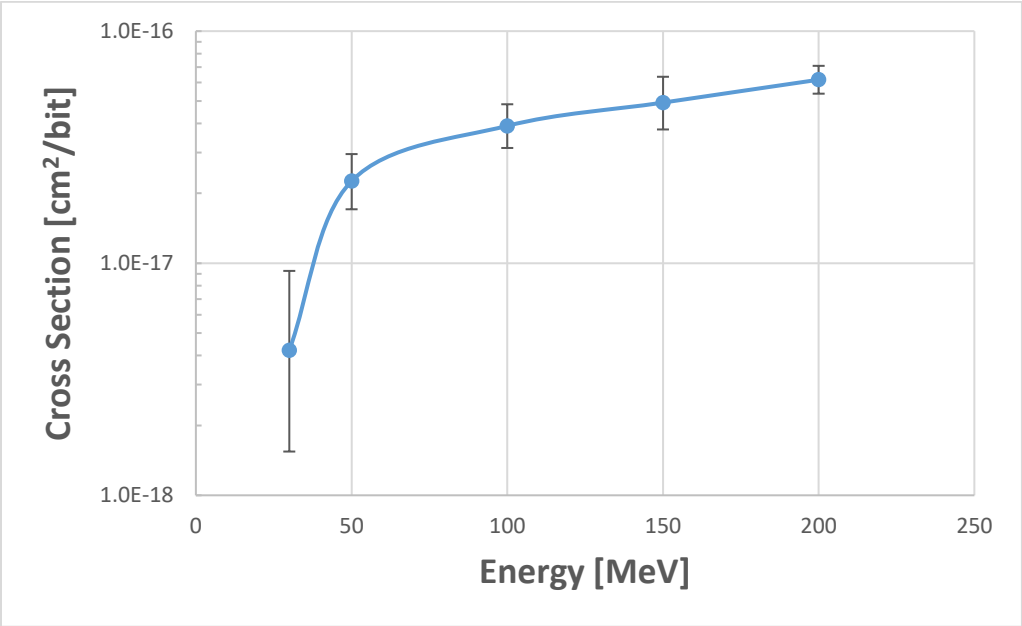


Figure 8: Uncorrectable MBUs cross section

7. PS tests

The main objective of these tests was to study the SEU vulnerability of the PS part of the Zynq-7000 device under proton irradiation. As mentioned in Section 6, the impact of proton radiation-induced SEEs in the behavior of the Zynq-7000 device has been previously studied [4],[5],[6],[7]. In this experiment, we aimed to: a) calculate the SEU cross sections of the embedded memories of the PS part (OCM, L1 and L3 caches) by running different memory tests, b) study the impact of proton radiation at the application level by running various processor benchmarks and c) for different cache configurations and for the full range of proton energies, from 30 up to 250 MeV.

7.1 Circuit under test

Figure 9 illustrates the functional blocks of the Zynq-7000 ARM SoC architecture.

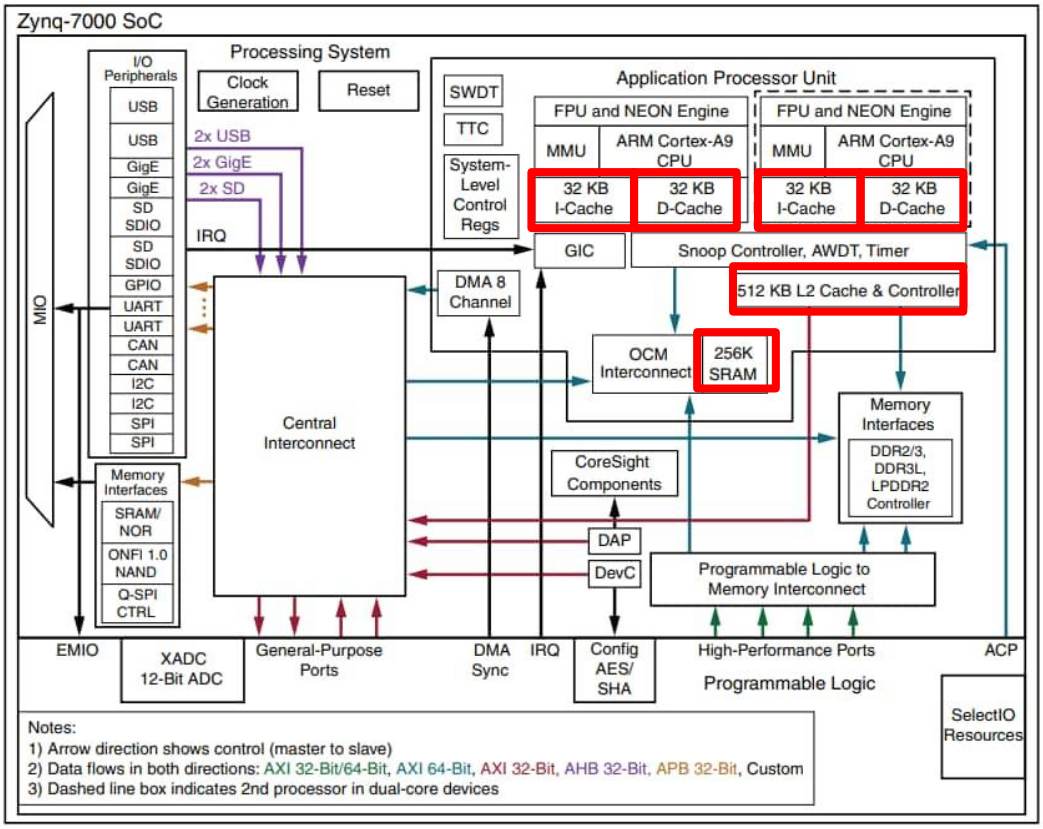


Figure 9: Zynq-7000 ARM SoC Architecture overview (highlighted memories have been targeted)

The following memory components of the Zynq-7000 APSoC (highlighted in the figure) have been targeted in our radiation tests:

- L1 Caches (Instruction and Data), 32KB each, 4-way set-associative.
- L2 Cache, 512KB, 8-way set-associative.
- Dual-ported On-chip RAM (OCM), 256KB SRAM.

Figure 10 shows the interfaces between the target system and the host PC. Host PC can access the targeted memories (OCM, caches) through the PL logic by sending JTAG commands. Two JTAG-to-AXI bridges have been integrated into PL to translate the JTAG commands to AXI transactions and then access the OCM memory through the HP-AXI port and the caches through the ARM accelerator coherency port (ACP). Host PC can also access the DDR memory through the HP-AXI port in the same way. These connections are used by the host PC to initiate the execution of the software tests and capture the test responses stored either in the targeted memories (OCM, caches) or the DDR memory.

There are also two UART connections between the target board and the host PC: UART 0 is used by the ARM CPU to transmit test responses, while UART 1 is used by the SEM IP core to log messages.

Xilinx SEM (Soft Error Mitigation) IP core was used to avoid upset accumulation in the CRAM during the execution of the PS tests, thus reducing the possibility that the tests will fail due to malfunction in the PL circuit. For that reason, all the components in the PL part, including the SEM IP, have been triplicated.

The same open-source platform used to run the PL tests, was also used to implement the JTAG transactions for accessing the CPU memories in the PS tests.

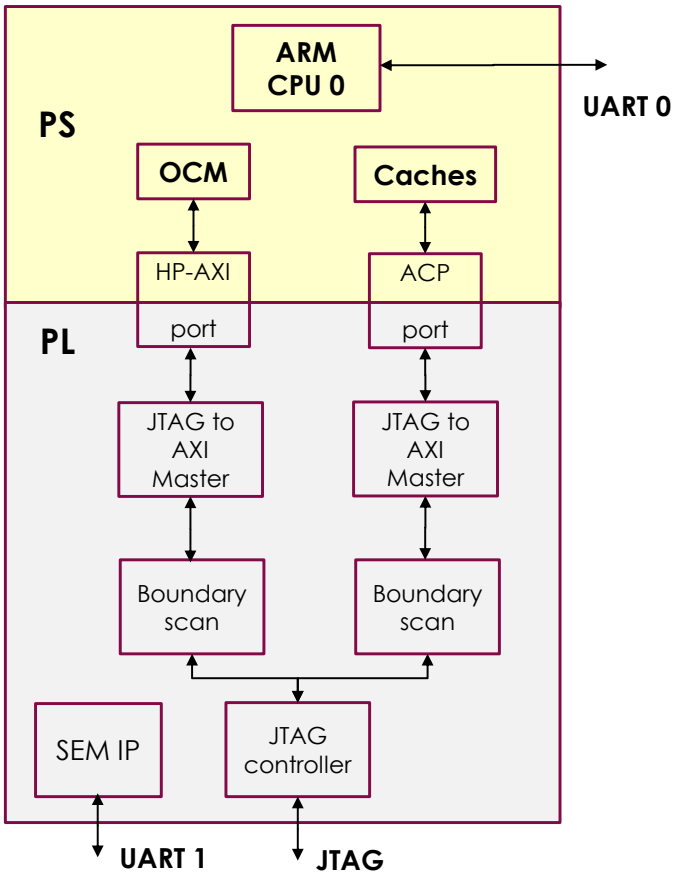


Figure 10: Interfaces between the host PC and the targeted components

7.2 Test programs

Two types of test programs have been used in the experiments:

- **Memory tests**: synthetic static and dynamic test programs. Static test programs are mainly executed by the host application, i.e., host reads and checks the contents of the targeted memories. Dynamic test programs are executed and by the ARM CPU, which also checks and logs the results.
- **Embedded microprocessor benchmarks**: standard embedded microprocessor benchmarks are executed to emulate real-world applications. The benchmarks run in ARM CPU without having an OS booted (i.e., bare-metal execution).

7.2.1 Static memory tests

Static memory tests apply a fixed test pattern into all memory addresses of the targeted memory, and then the memory is scanned several times to capture possible upsets. In our tests, the memory is written by the ARM CPU and read/scanned by the host PC. The test pattern is configurable, e.g. all 0s, or all 1s, or checkerboard pattern, or memory address value. In the current experiment, the test pattern was the memory address value. **Figure 11** presents the flow of a static memory test program.

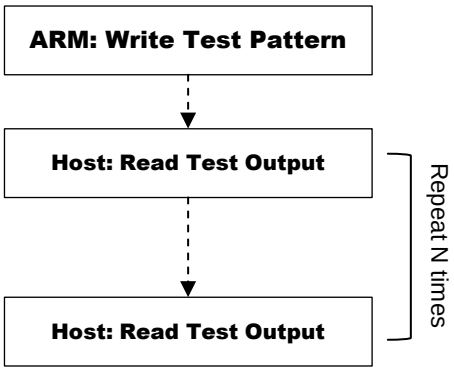


Figure 11: Static memory test flow

Table 10 summarizes all the static test programs executed in our experiments, including the targeted memory component, the fixed pattern, the value of N, the cache configuration, and comments for implementing the test.

Note: Static memory tests were performed for the OCM, L1 data, and L2 cache.

Table 10: Static memory tests features

Targeted memory	Pattern	N	Cache configuration	Comments
OCM	Address	100	All caches disabled	-
L1 data	Address	200	L2 cache disabled	A 32 Kb memory region is written to fill all the L1 data cache lines. During the test, no cache replacements occur, so all memory write/read transactions access the same L1 data lines.
L2 cache	Address	10	L1 caches disabled	Eight 64 KBytes memory regions are written to fill the L2 cache. After writing each memory region, one L2 cache way is locked to avoid data replacement. When all the eight memory regions have been written, the contents of the entire L2 cache are locked. Since the L1 cache is disabled, the memory transactions through the ACP port are forwarded to the L2 cache.

7.2.2 Dynamic memory tests

Dynamic memory tests write and read a known test pattern into all memory addresses of the targeted memory. The test pattern is configurable, e.g. all 0s, or all 1s, or checkerboard pattern, or memory address value. **Figure 12** presents the flow of a dynamic test program.

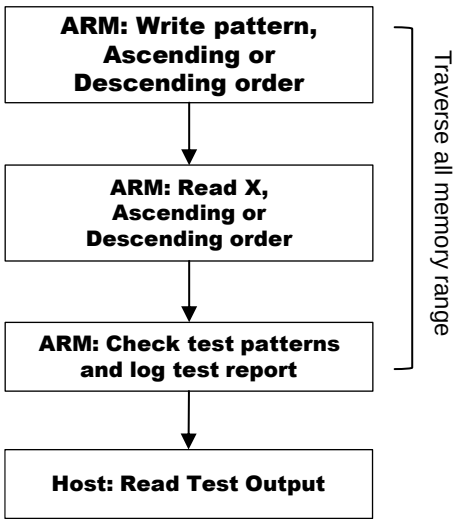


Figure 12: Dynamic memory test flow

In our experiment, the dynamic test programs implement the March algorithm. A March algorithm consists of a finite sequence of March Elements. A March Element is a Read and/or Write ONE or ZERO operation applied to every memory cell in either increasing or decreasing address order of the targeted component. This test plan exploits the March-C algorithm, the most basic form of March algorithms, which consist of six March elements: {⇕(w0); ↑(r0,w1); ↑(r1,w0); ↓(r0,w1); ↓(r1,w0); ⇕(r0)}.

According to [12], dynamic memory tests can stress a memory during radiation experiments and may reveal upset phenomena not observed from the static tests.

The March-C tests are described in **Table 11**.

Table 11: March-C tests

Test	Comments
⇕(w0)	Write ZERO to all memory cells in increasing or decreasing address order
↑(r0,w1)	Read (and compare with ZERO) and then write ONE to all memory cells in increasing address order
↑(r1,w0)	Read (and compare with ONE) and then write ZERO to all memory cells in increasing address order
↓(r0,w1)	Read (and compare with ZERO) and then write ONE to all memory cells in decreasing address order
↓(r1,w0)	Read (and compare with ONE) and then write ZERO to all memory cells in decreasing address order
⇕(r0)	Read (and compare with ZERO) all memory cells in increasing or decreasing address order

Note: Dynamic memory tests were performed for the OCM and L2 cache.

7.2.3 Embedded microprocessor benchmarks

The following six (6) embedded microprocessor benchmarks were executed: CRC32, FFT, Qsort, BasicMath, SHA, MatrixMul. All benchmarks, except the MatrixMul, are sourced from the MiBench suite[3]. MiBench programs are modified to be ported in the ARM CPU as bare metal applications.

The memory footprint of the benchmarks is shown in **Table 12**. Data Segment includes global and static variables, while ReadOnly (RO) Data includes constant data. The memory stack is not considered for the calculation of the data segments; this is why the data segment in the cases of SHA and MatrixMul benchmarks is zero. Note that the input test sets of the benchmarks have been selected or modified to achieve different data memory segment lengths:

- The data segments of the FFT, BasicMath, SHA and MatrixMul fit into the L1 data cache (32 KB)

[3] https://vhosts.eecs.umich.edu/mibench/index.html

- The data segment of Qsort does not fit into the L1 data cache, but it fits into the L2 cache (512 Kb); this means that during the execution of QSort, several replacements in L1 occur.
- The data segment of CRC32 does not fit into the L2 data cache (512 Kb); this means that during the execution of CRC32, several replacements in L2 occur.

Table 12: Benchmarks' memory footprint

Benchmark	Data Segment	RO Data
CRC32	1337.78 KB	0.01 KB
FFT	2.09 KB	0.11 KB
Qsort	156.25 KB	312.50 KB
BasicMath	6.09 KB	0 KB
SHA	0 KB	2.32 KB
MatrixMul	0 KB	7.32 KB

Three different test configurations were executed, as shown in the following figure:

- Bench 1: the host PC initiates the first benchmark (e.g., it sends the test configuration and commands the ARM to start executing the test), the benchmark is executed once, and its results are recorded back in the host application, then the host PC initiates the second benchmark, and so on. When all six benchmarks have been executed, the test starts again.
- Bench 20: the host PC initiates the first benchmark, which is executed 20 consecutive times, and the results from all 20 runs are recorded in the host application, then the second benchmark, and so on. When all six benchmarks have been executed, the test starts again.
- Bench continuous: a sequence of benchmarks (CRC32-FFT-QSort-BasicMath, SHA, MatrixMul) is executed and the results from all the benchmarks are recorded in the host application. The same sequence is repeated several times.

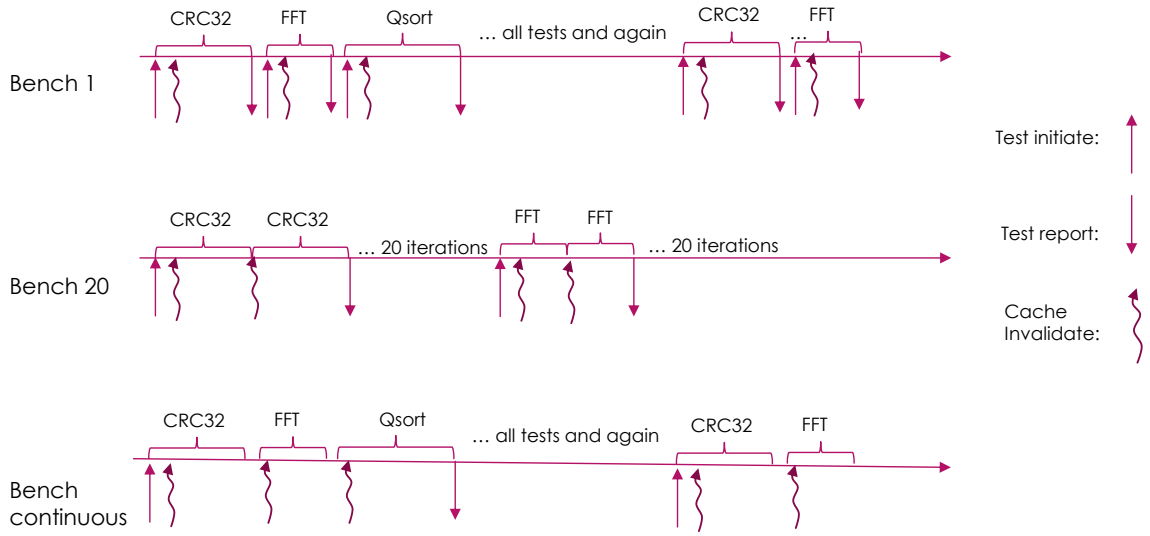


Figure 13: Test configurations for embedded benchmarks

In all the above test configurations, the caches are invalidated before every benchmark iteration. These configurations were implemented to emulate different workload conditions for the ARM CPUs.

Each test configuration was performed with four different cache settings in order to emulate the impact of caches at the application level failures:

- Both caches disabled
- L1 cache enabled, L2 cache disabled
- L1 cached disabled, L2 cache enabled
- Both caches enabled

Note: the results from the execution of the benchmarks were recorded with two different ways for redundancy reasons: (a) ARM CPU checks the output of the benchmarks, e.g., compares it with the golden signature, and sends the results into the serial port (UART 0), (b) ARM CPU stores the output of the benchmarks in a specific DDR memory region (2KB size) and the host PC reads this memory region using JTAG-to-AXI transactions.

7.3 PS test flow

The flow of PS tests is shown in **Figure 14**.

It performs the following steps:

1. The host application resets the target device activating the PS_POR_B switch of the ZC706 board through a relay module. The FPGA device is configured and the ARM CPU 0 boots from the QSPI Flash memory. The bootloader copies the test programs (static, dynamic and benchmarks) stored in the QSPI Flash to the DDR memory. If the system has been configured and initialized properly, the ARM CPU asserts a READY flag and waits for the host application to start the tests. Note that all the flags used for the handshake between the host application and the ARM CPU are bits stored in predefined memory addresses in the DDR. The host application accesses the flags through the JTAG-to-AXI interface.
2. The host application polls the READY flag. READY flag equals zero means that the system has not been initialized properly or the test program has been crashed and cannot be recovered through reset. In this case, the host application power cycles the board.
3. If the READY flag is set, the host application initiates the test sending the test parameters, including the test sequence (e.g., a list of tests to be executed), the number of iterations (how many times the ARM CPU will repeat the sequence of tests), and the cache configurations. The test parameters are written to the DDR through the JTAG-to-AXI interface. Then, it activates a START flag.
4. If the ARM CPU receives the START flag, it executes the test sequence for the specified number of iterations. After each iteration, the ARM CPU checks the output (e.g., compares it with the golden data) and logs the report to the serial port (UART 0) and a specified memory region in the DDR. When it completes the test, it activates a DONE flag.

5. The host application polls the DONE flag; if a timer in the host application expires and the DONE flag is still zero, it means that the system has been crashed. In this case, the host application logs the crash event and resets the board. Otherwise, it goes to the next test.
6. In our experiments, the host application repeatedly executes the same test sequence until the target fluence is reached for the current test setup. Then, we stop the test.

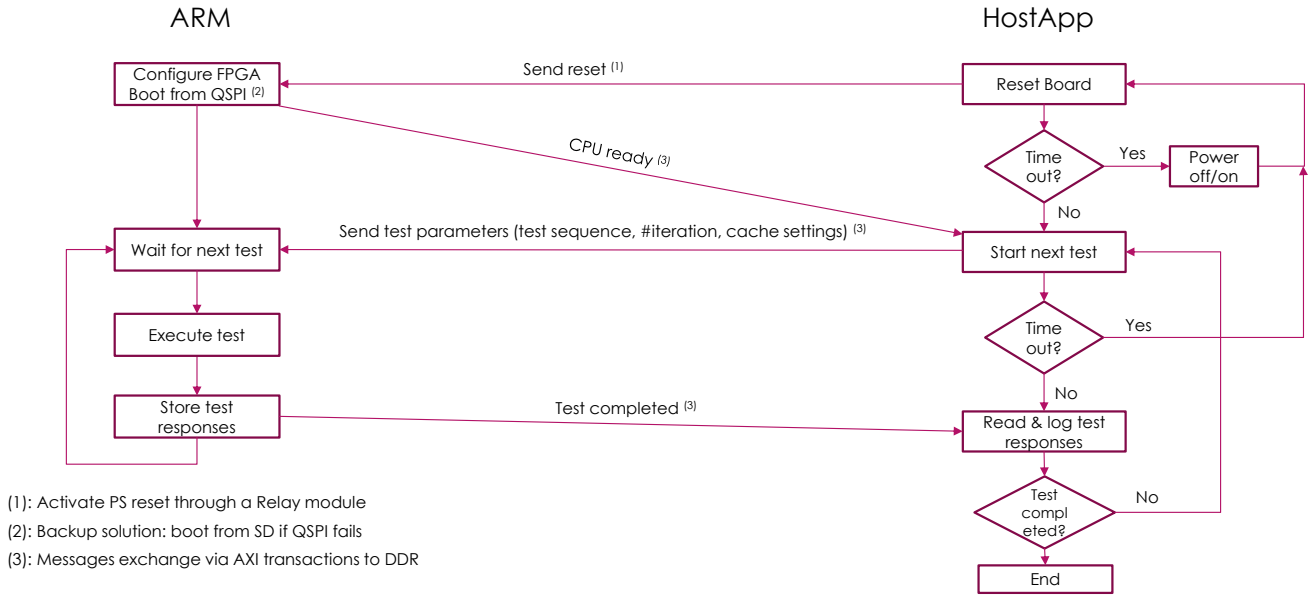


Figure 14: PS test flow

7.4 PS test results

This section presents the results from the execution of the static memory tests, dynamic memory tests, and benchmarks.

7.4.1 Memory tests

Table 13 and **Table 14** present the results of the static memory tests performed for the OCM and L1 data cache for different energies, respectively.

Table 13: OCM static tests – SEUs and cross sections

Test	Energy [MeV]	Duration [secs]	Flux [p/cm^2/sec]	Fluence [p/cm^2]	SEUs	Cross section per device [cm^2]	Cross section per bit [cm^2/bit]
OCM	30	236	4.244E+07	1.001E+10	531	5.305E-08	2.529E-14
OCM	50	528	1.895E+07	9.570E+09	120	1.254E-08	5.979E-15
OCM	100	537	1.863E+07	1.001E+10	220	2.198E-08	1.048E-14
OCM	150	221	4.522E+07	1.004E+10	388	3.865E-08	1.843E-14
OCM	200	165	1.214E+08	1.784E+10	371	2.080E-08	9.919E-15

Table 14: L1 data cache static tests – SEUs and cross sections

Test	Energy [MeV]	Duration [secs]	Flux [p/cm^2/sec]	Fluence [p/cm^2]	SEUs	Cross section per device [cm^2]	Cross section per bit [cm^2/bit]
L1 data	30	236	4.246E+07	1.002E+10	61	6.088E-09	2.322E-14
L1 data	50	533	1.878E+07	1.001E+10	34	3.397E-09	1.296E-14
L1 data	100	527	1.899E+07	1.003E+10	19	1.894E-09	7.226E-15
L1 data	150	228	4.405E+07	1.004E+10	2	1.992E-10	7.599E-16
L1 data	200	165	1.216E+08	1.793E+10	42	2.342E-09	8.935E-15

Table 15 and **Table 16** present the results of the dynamic memory tests performed for the OCM and L2 cache for different energies, respectively.

Table 15: OCM dynamic tests – SEUs and cross sections

Test	Energy [MeV]	Duration [secs]	Flux [p/cm^2/sec]	Fluence [p/cm^2]	SEUs	Cross section per device [cm^2]	Cross section per bit [cm^2/bit]
OCM	30	209.7	4.224E+07	8.858E+09	73	8.241E-09	3.930E-15
OCM	50	322.2	3.775E+07	1.216E+10	38	3.124E-09	1.490E-15
OCM	100	326.6	3.728E+07	1.218E+10	64	5.256E-09	2.506E-15
OCM	150	148.2	4.493E+07	6.659E+09	46	6.908E-09	3.294E-15
OCM	200	831.4	4.860E+07	4.040E+10	241	5.965E-09	2.844E-15

Table 16: L2 cache dynamic tests – SEUs and cross sections

Test	Energy [MeV]	Duration [secs]	Flux [p/cm^2/sec]	Fluence [p/cm^2]	SEUs	Cross section per device [cm^2]	Cross section per bit [cm^2/bit]
L2-C	30	137.4	4.233E+07	5.815E+09	78	1.341E-08	3.198E-15
L2-C	50	375.8	2.264E+07	8.509E+09	116	1.363E-08	3.250E-15
L2-C	100	355.7	1.855E+07	6.598E+09	66	1.000E-08	2.385E-15
L2-C	150	203.4	4.496E+07	9.147E+09	72	7.871E-09	1.877E-15
L2-C	200	723.6	4.878E+07	3.530E+10	337	9.547E-09	2.276E-15

Figure 15 shows the SEU cross sections of all the PS memories (OCM, L1 data cache, L2 cache) observed in the previously described static and dynamic memory tests. For the calculation of the error bars, we assumed a Poisson distribution of the SEUs, confidence level 95%, and uncertainty on the measured fluence 10% [8],[9].

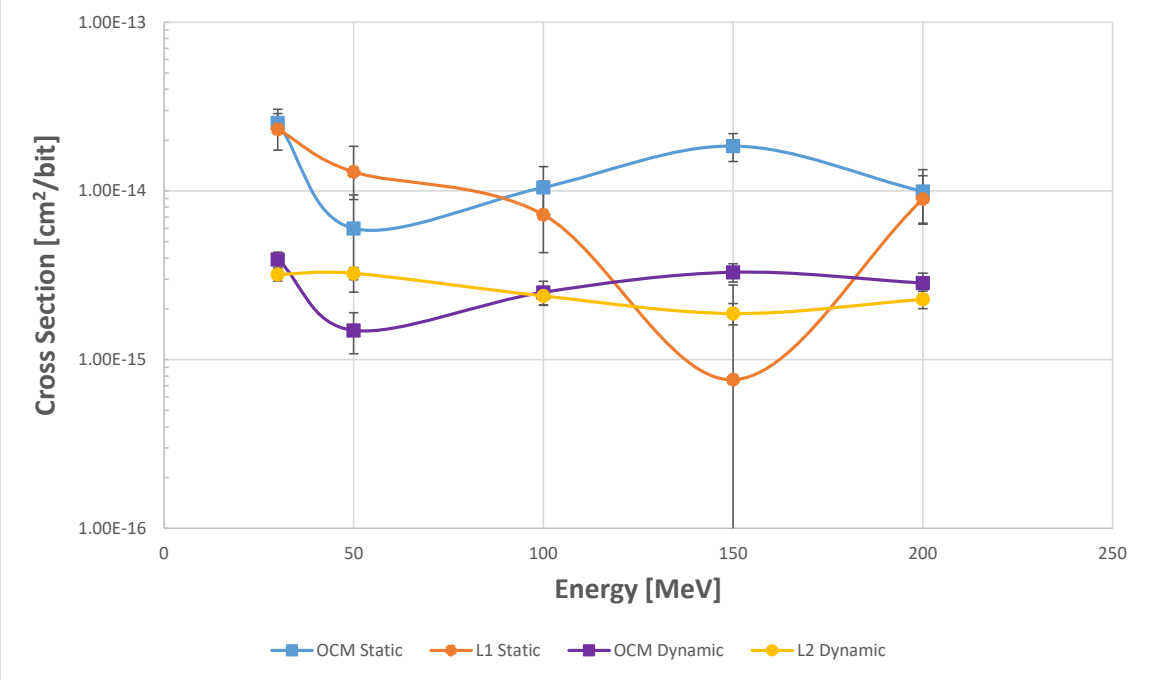


Figure 15: PS memories cross section vs. proton energies

Comments from the SEU analysis of the memory tests:

1. Higher SEU rates have been observed for all the memories at the lower proton energy (30 MeV); this observation is also true for the execution of processor benchmarks (i.e. higher SDC rates in 30 MeV) as described in the following sections. This could be justified due to charges caused by low-energy direct ionizing and result in SEUs.
2. The OCM static tests show a similar cross section with previously published works (e.g., it is 8.05E-15 at 62 MeV in [5]).
3. The L2 dynamic tests show higher cross section compared to previous works (e.g., it is less than 4E-16 at 62 MeV [5] and 250 MeV [4])
4. It is the first time that proton radiation results have been reported for the L1 data cache.
5. There is a constant offset between OCM static and OCM dynamic tests, which maybe due to upsets that occur in the FIFOs located in the OCM-HP ports. The HP port is used for scanning the OCM only for static tests.

7.4.2 Processor benchmarks

Table 17 shows the results for all the six (6) processor benchmarks (CRC32, FFT, QSort, BasicMath, SHA, MatrixMul), including three (3) different test configurations (Bench 1, Bench 20, Bench continuous), four (4) different cache configurations (all caches disabled, L1 enabled and L2 disabled, L1 disabled and L2 enabled, all caches enabled) and five (5) proton energies (30, 50, 100, 150 and 200 MeV).

Table 17: Processor benchmark tests

(Benchmark types are B1: Bench 1, B20: Bench 20, BC: Bench continuous,
Cache configurations are 0: all caches disabled, 1: L1 enabled and L2 disabled, 2: L1 disabled and L2 enabled, 3: all cached enabled)

Bench	Type	Cache Config.	30 MeV			50 MeV			100 MeV			150 MeV			200 MeV		
			Runs	Duration [secs]	SDC	Runs	Duration [secs]	SDC	Runs	Duration [secs]	SDC	Runs	Duration [secs]	SDC	Runs	Duration [secs]	SDC
CRC32	B1	0	161	125.8	0	346	269.4	0	336	261.5	0	117	91.4	0	76	59.5	0
CRC32	B1	1	614	32.0	0	1351	71.3	0	1288	69.4	1	647	33.0	0	2792	116.4	0
CRC32	B1	2	135	41.9	8	472	145.4	7	627	192.8	5	148	45.6	2	424	130.3	9
CRC32	B1	3	394	19.3	6	1277	62.2	1	1401	69.7	0	487	23.8	0	2092	102.3	9
CRC32	B20	0	171	134.0	0	437	342.5	0	380	297.9	0	171	134.0	0	233	182.6	0
CRC32	B20	1	1274	59.0	0	6098	282.6	0	5929	274.8	0	1577	73.1	2	2185	101.3	3
CRC32	B20	2	152	46.9	12				967	298.6	6	303	93.5	6	114	35.2	12
CRC32	B20	3	910	38.1	10	11168	467.7	17	5605	234.7	7	2452	102.7	15	1882	78.8	34
CRC32	BC	0	125	98.0	1	429	336.3	0	432	338.6	0	166	130.1	0	221	173.2	0
CRC32	BC	1	2017	93.5	0	4358	202.0	0	4411	204.4	0	1452	67.3	0	3212	148.9	1
CRC32	BC	2	199	61.4	23	853	263.4	10	785	242.4	10	292	90.2	7	72	22.2	6
CRC32	BC	3	855	35.8	12	4165	174.4	12	4032	168.9	6	1318	55.2	7	1407	58.9	16
FFT	B1	0	160	10.9	0	345	24.4	0	335	23.5	0	115	8.0	0	75	5.5	0
FFT	B1	1	605	10.1	0	1349	22.8	0	1277	22.2	0	636	10.4	0	1851	31.0	0
FFT	B1	2	140	4.4	0	476	15.1	0	632	20.5	0	150	5.1	0	426	14.1	0
FFT	B1	3	390	6.6	0	1335	22.7	0	1400	23.8	0	477	8.0	0	2067	33.9	1
FFT	B20	0	171	11.0	0	435	27.9	0	380	24.4	0	190	12.2	0	285	18.3	0
FFT	B20	1	2685	14.1	0	6042	31.7	0	5852	30.7	0	1577	8.3	0	2222	11.7	17
FFT	B20	2	152	3.9	1				950	24.3	0	323	8.3	0	115	2.9	0
FFT	B20	3	912	4.7	0	11058	57.5	0	5586	29.0	1	2793	14.5	0	1902	9.9	0
FFT	BC	0	191	12.3	0	429	27.6	0	434	27.9	0	166	10.7	0	220	14.1	0
FFT	BC	1	2018	10.6	0	4358	22.9	0	4412	23.2	0	1452	7.6	0	3211	16.9	1
FFT	BC	2	199	5.1	0	854	21.8	1	884	22.6	0	292	7.5	0	71	1.8	0
FFT	BC	3	977	5.1	0	4165	21.7	0	4032	21.0	0	1320	6.9	0	1407	7.3	0

Bench	Type	Cache Config.	30 MeV			50 MeV			100 MeV			150 MeV			200 MeV		
			Runs	Duration [secs]	SDC	Runs	Duration [secs]	SDC	Runs	Duration [secs]	SDC	Runs	Duration [secs]	SDC	Runs	Duration [secs]	SDC
Qsort	B1	0	158	47.8	0	347	104.8	0	334	100.7	0	115	34.7	0	75	22.9	0
Qsort	B1	1	612	14.6	0	1349	33.2	0	1752	39.1	0	644	15.0	0	1840	44.4	2
Qsort	B1	2	138	16.7	19	476	51.5	12	626	67.2	11	150	16.3	11	428	46.7	14
Qsort	B1	3	396	8.8	7	1292	30.3	1	1410	34.4	3	489	11.5	5	2086	46.4	17
Qsort	B20	0	171	50.9	0	436	129.7	0	380	113.0	0	152	45.2	0	266	79.1	0
Qsort	B20	1	2694	51.1	0	6041	114.6	0	5927	112.4	0	1577	29.9	1	2203	41.8	6
Qsort	B20	2	171	17.8	25				969	101.0	21	304	31.7	19	95	9.9	13
Qsort	B20	3	891	14.6	17	11113	181.9	34	5548	90.8	22	2812	46.0	25	1881	30.8	44
Qsort	BC	0	125	37.2	2	429	127.6	0	434	129.1	0	166	49.4	0	220	65.4	0
Qsort	BC	1	2011	38.1	0	4357	82.6	0	4411	83.7	0	1452	27.5	1	3211	60.9	2
Qsort	BC	2	199	20.7	33	854	89.0	14	884	92.2	10	292	30.4	19	71	7.4	8
Qsort	BC	3	972	15.9	18	4165	68.2	14	4032	66.0	8	1320	21.6	12	1407	23.0	40
BasicMath	B1	0	158	2.6	0	342	5.7	0	335	5.6	0	116	1.8	0	74	1.2	0
BasicMath	B1	1	607	10.1	0	1350	22.7	0	1275	21.7	0	642	10.7	0	1841	31.6	0
BasicMath	B1	2	138	2.3	0	471	7.8	0	626	10.3	0	147	2.5	0	421	7.3	0
BasicMath	B1	3	392	6.5	0	1329	22.4	0	1394	23.4	0	483	8.1	0	2075	34.3	0
BasicMath	B20	0	171	0.9	0	435	2.2	0	380	1.9	0	190	1.0	0	285	1.4	0
BasicMath	B20	1	2668	2.4	0	5985	5.3	0	5890	5.2	0	1558	1.4	0	2204	1.9	0
BasicMath	B20	2	152	0.3	0				893	2.0	0	323	0.7	0	115	0.3	0
BasicMath	B20	3	912	0.8	0	11115	9.9	0	5586	5.0	0	2774	2.5	0	1957	1.7	0
BasicMath	BC	0	191	1.0	0	429	2.2	0	434	2.2	0	166	0.8	0	220	1.1	0
BasicMath	BC	1	2018	1.8	0	4358	3.9	0	4412	3.9	0	1452	1.3	0	3211	2.8	0
BasicMath	BC	2	199	0.5	0	854	1.9	0	884	2.0	0	292	0.7	0	71	0.2	0
BasicMath	BC	3	977	0.9	0	4165	3.7	0	4032	3.6	0	1320	1.2	0	1407	1.3	0
SHA	B1	0	161	7.7	0	345	16.4	0	336	15.6	0	116	5.3	0	76	3.7	0
SHA	B1	1	606	10.0	0	1351	22.8	0	1275	21.8	0	642	10.5	0	1840	31.5	0
SHA	B1	2	139	3.3	1	475	11.4	0	631	15.0	0	149	3.5	0	428	10.7	0
SHA	B1	3	389	6.4	0	1322	22.6	0	1398	23.4	0	478	7.9	0	2074	34.0	0

Bench	Type	Cache Config.	30 MeV			50 MeV			100 MeV			150 MeV			200 MeV		
			Runs	Duration [secs]	SDC	Runs	Duration [secs]	SDC	Runs	Duration [secs]	SDC	Runs	Duration [secs]	SDC	Runs	Duration [secs]	SDC
SHA	B20	0	171	7.1	0	435	18.1	0	380	15.8	0	190	7.9	0	285	11.9	0
SHA	B20	1	2705	8.3	0	6080	18.6	0	5909	18.1	0	1577	4.8	1	2223	6.8	0
SHA	B20	2	152	2.8	0				969	17.9	0	323	6.0	0	114	2.1	0
SHA	B20	3	905	2.8	5	11115	34.6	1	5605	17.4	0	2793	8.7	0	1938	6.0	0
SHA	BC	0	191	8.0	0	429	17.9	0	434	18.1	0	166	6.9	0	220	9.2	0
SHA	BC	1	2017	6.2	0	4358	13.3	0	4411	13.5	0	1452	4.4	0	3211	9.8	1
SHA	BC	2	199	3.7	0	854	15.7	0	884	16.3	0	292	5.4	0	71	1.3	0
SHA	BC	3	976	3.0	0	4165	13.0	0	4032	12.5	0	1320	4.1	0	1407	4.4	0
MatrixMul	B1	0	159	4.1	0	345	7.7	0	336	7.8	0	115	2.5	0	75	1.9	0
MatrixMul	B1	1	601	9.6	0	1352	22.5	0	1274	22.0	0	639	10.4	0	1908	32.0	0
MatrixMul	B1	2	137	2.7	0	473	8.4	0	621	11.2	0	148	2.4	0	423	7.5	0
MatrixMul	B1	3	387	6.2	0	1238	20.5	0	1392	23.8	0	482	7.8	0	2074	33.5	0
MatrixMul	B20	0	190	3.1	0	435	7.1	0	380	6.2	0	190	3.1	0	285	4.6	0
MatrixMul	B20	1	2680	5.9	0	6023	13.2	0	5890	12.9	0	1577	3.4	0	2223	4.9	0
MatrixMul	B20	2	171	1.2	0				969	7.0	0	323	2.3	0	133	1.0	0
MatrixMul	B20	3	911	2.0	0	11123	24.0	0	5586	12.1	0	2755	5.9	0	1892	4.1	3
MatrixMul	BC	0	191	3.1	0	429	7.0	0	434	7.1	0	166	2.7	0	220	3.6	0
MatrixMul	BC	1	2018	4.4	0	4358	9.5	0	4412	9.6	0	1452	3.2	0	3211	7.0	0
MatrixMul	BC	2	199	1.4	0	854	6.2	0	884	6.4	1	292	2.1	0	71	0.5	0
MatrixMul	BC	3	977	2.1	0	4165	9.0	0	4032	8.7	0	1320	2.9	0	1407	3.0	0

7.4.3 Analysis of the benchmarks

We have analysed the results from the execution of all the above tests per benchmark, test configuration and cache configuration.

7.4.3.1 SDCs per benchmark

Table 18 shows the silent data corruption (SDC) cross section per benchmark for two cache configurations (only L2 enabled and both caches enabled) and different proton energies. The results were collected from the execution of the benchmarks for all the different test configurations.

Table 18: SDCs per benchmark

Bench	Energy [MeV]	L1 disabled, L2 enabled			Both caches enabled		
		Fluence [p/cm^2]	SDCs	Cross section per device [cm^2]	Fluence [p/cm^2]	SDCs	Cross section per device [cm^2]
Crc32	30	6.372E+09	43	6.75E-09	3.951E+09	28	7.09E-09
	50	7.766E+09	17	2.19E-09	1.338E+10	30	2.24E-09
	100	1.372E+10	21	1.53E-09	8.850E+09	13	1.47E-09
	150	1.032E+10	15	1.45E-09	8.176E+09	22	2.69E-09
	200	1.334E+10	27	2.02E-09	2.176E+10	59	2.71E-09
FFT	30	5.679E+08	1	1.76E-09	6.942E+08	0	0.00E+00
	50	7.016E+08	1	1.43E-09	1.935E+09	0	0.00E+00
	100	1.260E+09	0	0.00E+00	1.379E+09	1	7.25E-10
	150	9.359E+08	0	0.00E+00	1.323E+09	0	0.00E+00
	200	1.266E+09	0	0.00E+00	3.747E+09	1	2.67E-10
Qsort	30	2.342E+09	77	3.29E-08	1.667E+09	42	2.52E-08
	50	2.670E+09	26	9.74E-09	5.327E+09	49	9.20E-09
	100	4.869E+09	42	8.63E-09	3.575E+09	33	9.23E-09
	150	3.532E+09	49	1.39E-08	3.560E+09	42	1.18E-08
	200	4.384E+09	35	7.98E-09	8.813E+09	101	1.15E-08
Basic Math	30	1.319E+08	0	0.00E+00	3.453E+08	0	0.00E+00
	50	1.861E+08	0	0.00E+00	6.841E+08	0	0.00E+00
	100	2.684E+08	0	0.00E+00	5.971E+08	0	0.00E+00
	150	1.743E+08	0	0.00E+00	5.287E+08	0	0.00E+00
	200	4.069E+08	0	0.00E+00	2.036E+09	0	0.00E+00
SHA	30	4.140E+08	1	2.42E-09	5.186E+08	5	9.64E-09
	50	5.156E+08	0	0.00E+00	1.333E+09	1	7.50E-10
	100	9.187E+08	0	0.00E+00	9.984E+08	0	0.00E+00
	150	6.695E+08	0	0.00E+00	9.296E+08	0	0.00E+00

	200	9.338E+08	0	0.00E+00	2.923E+09	0	0.00E+00
Matrix Mul	30	2.279E+08	0	0.00E+00	4.371E+08	0	0.00E+00
	50	2.760E+08	0	0.00E+00	1.017E+09	0	0.00E+00
	100	4.588E+08	1	2.18E-09	8.330E+08	0	0.00E+00
	150	3.078E+08	0	0.00E+00	7.477E+08	0	0.00E+00
	200	5.449E+08	0	0.00E+00	2.497E+09	3	1.20E-09

The SDC cross sections for the CRC32 and Qsort benchmarks for two cache configurations are shown in **Figure 16**.

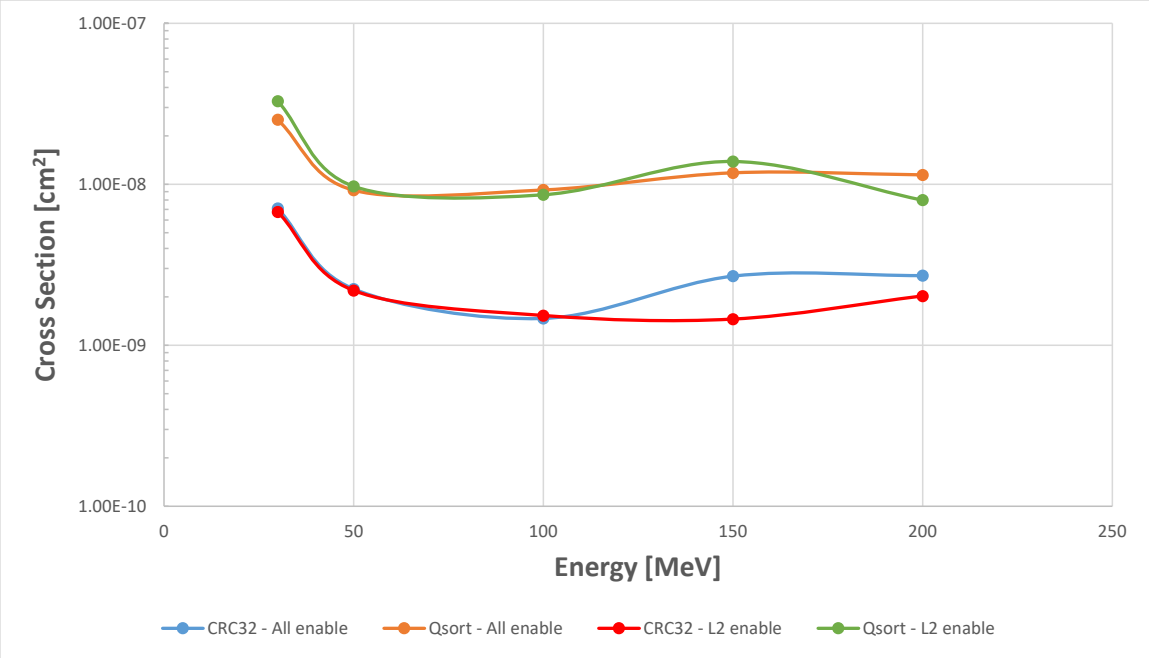


Figure 16: SDC cross section for CRC32 and Qsort

Comments from the SDC analysis:

- Very few SDCs have been observed in cache configurations "both caches disabled" and "only L1 enabled" and are not included in the above table; they will be presented in the following subsection.
- No SDCs in BasicMath and very few SDCs have been observed in FFT, SHA and MatrixMul benchmarks (i.e., much less than CRC32 and QSort). This is due to: a) these benchmarks have a low memory footprint (e.g., small data segment size) and thus occupy a small portion of the caches and b) their execution time is shorter compared to CRC32 and QSort (i.e., less time in the beam).
- CRC32 and Qsort present a higher number of SDCs, while CRC32 has lower cross section than Qsort. This could be explained by the fact that the data segment of CRC32 (see **Table 12**) is larger than the L2 cache size, which means more L2 cache replacements and thus shorter average retention of its data in L2 cache.

7.4.3.2 SDCs per test configuration

Table 19 shows the silent data corruption (SDC) cross section per test configuration for different cache configurations and proton energies.

Table 19: SDCs per test configuration

Test config.	Energy {MeV]	Both caches disabled			L1 enabled, L2 disabled		
		Fluence [p/cm^2]	SDCs	Cross section per device [cm^2]	Fluence [p/cm^2]	SDCs	Cross section per device [cm^2]
Bench 1	30	8.413E+9	0	0.00E+00	3.667E+9	0	0.00E+00
	50	8.043E+9	0	0.00E+00	3.657E+9	0	0.00E+00
	100	7.673E+9	0	0.00E+00	3.643E+9	1	2.74E-10
	150	6.496E+9	0	0.00E+00	4.040E+9	0	0.00E+00
	200	9.699E+9	0	0.00E+00	16.45E+9	2	1.22E-10
Bench 20	30	8.781E+9	0	0.00E+00	5.976E+9	0	0.00E+00
	50	9.997E+9	0	0.00E+00	8.755E+9	0	0.00E+00
	100	8.602E+9	0	0.00E+00	8.482E+9	0	0.00E+00
	150	9.186E+9	0	0.00E+00	5.461E+9	4	7.32E-10
	200	36.30E+9	0	0.00E+00	20.48E+9	26	1.27E-09
Bench cont.	30	6.776E+9	3	4.43E-10	6.556E+9	0	0.00E+00
	50	9.799E+9	0	0.00E+00	6.353E+9	0	0.00E+00
	100	9.748E+9	0	0.00E+00	6.350E+9	0	0.00E+00
	150	9.065E+9	0	0.00E+00	5.028E+9	1	1.99E-10
	200	32.50E+9	0	0.00E+00	29.95E+9	5	1.67E-10
		L1 disabled, L2 enabled			**Both caches enabled**		
Bench 1	30	3.021E+9	28	9.27E-09	2.277E+9	13	5.71E-09
	50	4.514E+9	19	4.21E-09	3.408E+9	2	5.87E-10
	100	5.799E+9	16	2.76E-09	3.687E+9	3	8.14E-10
	150	3.396E+9	13	3.83E-09	3.018E+9	5	1.66E-09
	200	10.55E+9	23	2.18E-09	13.85E+9	27	1.95E-09
Bench 20	30	3.093E+9	38	1.23E-08	2.669E+9	32	1.20E-08
	50	3.177E+9	15	4.72E-09	14.57E+9	52	3.57E-09
	100	8.177E+9	27	3.30E-09	7.205E+9	30	4.16E-09
	150	6.432E+9	25	3.89E-09	8.119E+9	40	4.93E-09
	200	4.440E+9	25	5.63E-09	15.99E+9	81	5.07E-09
Bench cont.	30	3.940E+9	56	1.42E-08	2.664E+9	30	1.13E-08
	50	7.539E+9	25	3.32E-09	5.482E+9	26	4.74E-09
	100	6.991E+9	21	3.00E-09	5.262E+9	14	2.66E-09
	150	6.153E+9	26	4.23E-09	4.134E+9	19	4.60E-09
	200	4.078E+9	14	3.43E-09	11.93E+9	56	4.69E-09

The SDC cross sections for the three test configurations and cache configurations "only L2 enabled" and "both caches enabled" are shown in **Figure 17**.

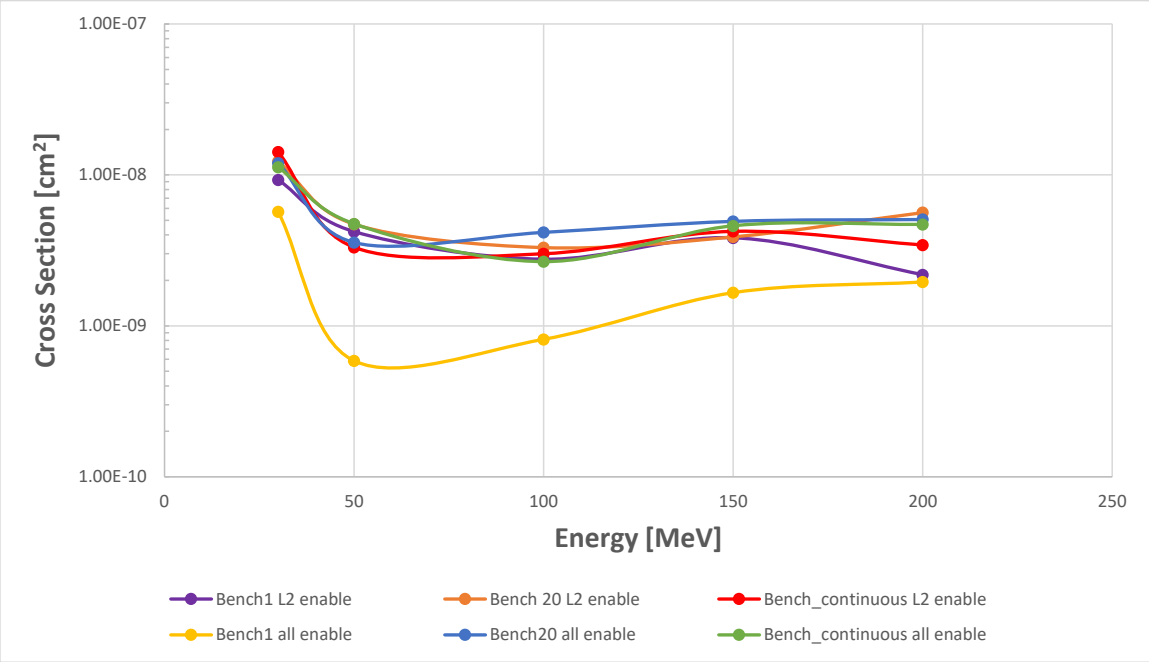


Figure 17: SDC cross section for the three test configurations

Comments from the SDC analysis:

- No differences between the three test configurations (Bench 1, Bench 20, Bench continuous) have been observed. Only the test "Bench 1/all caches enabled" produced a lower cross section; no explanation for this result.
- Very few SDCs have been observed in cache configurations "both caches disabled" and "only L1 enabled", as shown in the table above.
- No differences between the two cache configurations "only L2 enabled" and "both caches enabled" have been observed; it seems that the upsets in the L2 cache dominate the cross section.

7.4.3.3 SDCs per cache configuration

Table 20 shows the SDC cross section per cache configuration (only L1 enabled, only L2 enabled and both caches enabled) for different proton energies. The results were collected from the execution of the six benchmarks for all the different test configurations.

Table 20: SDCs per cache configuration

Cache configuration	Energy [MeV]	Fluence [p/cm^2]	SDCs	Cross section per device [cm^2]	Cross section per bit [cm^2/bit]
L1 enabled, L2 disabled	30	1.620E+10	0	0.00E+00	0.00E+00
	50	1.877E+10	0	0.00E+00	0.00E+00
	100	1.847E+10	1	5.41E-11	2.06E-16
	150	1.453E+10	5	3.44E-10	1.31E-15
	200	6.689E+10	33	4.93E-10	1.88E-15
L1 disabled, L2 enabled	30	1.005E+10	122	1.21E-08	2.89E-15
	50	1.523E+10	59	3.87E-09	9.24E-16
	100	2.097E+10	64	3.05E-09	7.28E-16
	150	1.598E+10	64	4.00E-09	9.55E-16
	200	1.907E+10	62	3.25E-09	7.75E-16
Both caches enabled	30	7.610E+09	75	9.85E-09	n/a
	50	2.346E+10	80	3.41E-09	n/a
	100	1.615E+10	47	2.91E-09	n/a
	150	1.527E+10	64	4.19E-09	n/a
	200	4.176E+10	164	3.93E-09	n/a

Figure 18 shows the SDC cross sections per device for three cache configurations (only L1 enabled, only L2 enabled, both caches enabled), while **Figure 19** shows the SDC cross sections per bit for two cache configurations (only L1 enabled, only L2 enabled). Note that for the calculation of the cross sections per bit the total sizes, and not the active regions, of the caches were considered. The results from the execution of all benchmarks are included in these figures.

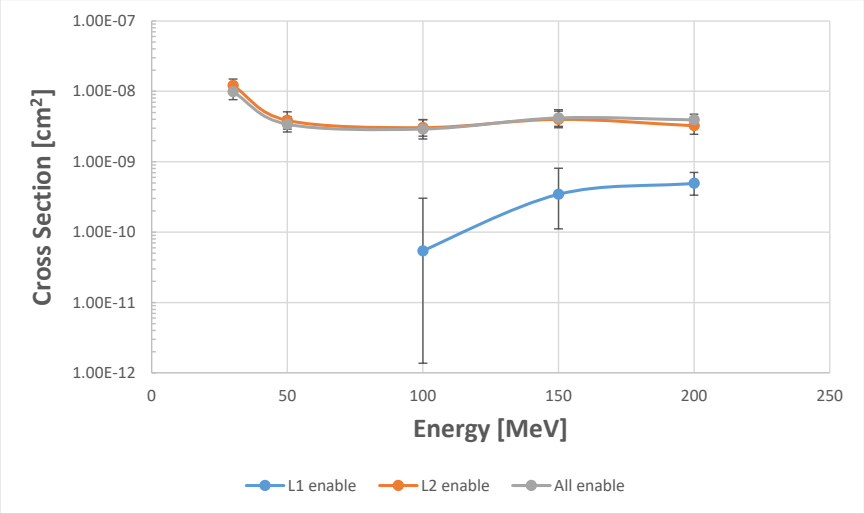


Figure 18: SDC cross section per device for different cache configurations

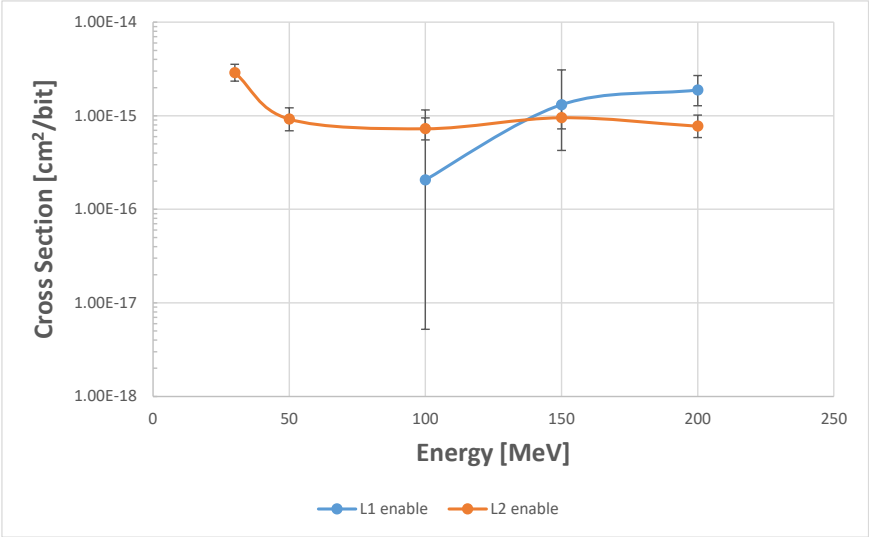


Figure 19: SDC cross section per bit for different cache configurations

Comments for the SDC analysis:

- No differences between the cache configurations "only L2 enabled" and "both caches enabled" have been observed; it seems that the upsets in the L2 cache dominate the cross section.
- The cross section per device is lower when only L1 cache is enabled.
- The cross sections per bit for the L1 and L1 caches are similar.

7.4.3.4 System crashes

System crashes - probably caused by SEFIs in the ARM SoC – have been observed during the execution of the dynamic memory tests and the benchmarks. **Table 21** shows the system crashes per cache configuration (Both caches disabled, only L1 enabled, only L2 enabled, both caches enabled, OCM used & caches disabled) and in total. **Figure 20** shows the total system crashes including all cache configurations.

Table 21: System crashes

Energy [MeV]	Caches disabled			Only L1 enabled			Only L2 enabled		
	Fluence [p/cm^2]	System crashes	Cross section per device [cm^2]	Fluence [p/cm^2]	System crashes	Cross section per device [cm^2]	Fluence [p/cm^2]	System crashes	Cross section per device [cm^2]
30	2.397E+10	0	0.00E+00	2.590E+10	0	0.00E+00	1.587E+10	26	1.64E-09
50	2.784E+10	0	0.00E+00	2.840E+10	0	0.00E+00	2.056E+10	2	9.73E-11
100	2.603E+10	0	0.00E+00	2.558E+10	1	3.91E-11	2.756E+10	2	7.26E-11
150	2.475E+10	0	0.00E+00	2.010E+10	2	9.95E-11	2.513E+10	3	1.19E-10
200	7.848E+10	1	1.27E-11	8.630E+10	6	6.95E-11	5.437E+10	17	3.13E-10

Energy [MeV]	Both caches enabled			OCM used & cached disabled			Total (all cache configurations)		
	Fluence [p/cm^2]	System crashes	Cross section per device [cm^2]	Fluence [p/cm^2]	System crashes	Cross section per device [cm^2]	Fluence [p/cm^2]	System crashes	Cross section per device [cm^2]
30	7.610E+09	0	0.00E+00	8.858E+09	0	0.00E+00	8.221E+10	16	1.95E-10
50	2.346E+10	2	8.53E-11	1.216E+10	1	8.22E-11	1.124E+11	5	4.45E-11
100	1.615E+10	6	3.71E-10	1.218E+10	1	8.21E-11	1.075E+11	10	9.30E-11
150	1.527E+10	4	2.62E-10	6.659E+09	0	0.00E+00	9.190E+10	9	9.79E-11
200	4.176E+10	9	2.16E-10	4.040E+10	1	2.47E-11	3.013E+11	34	1.13E-10

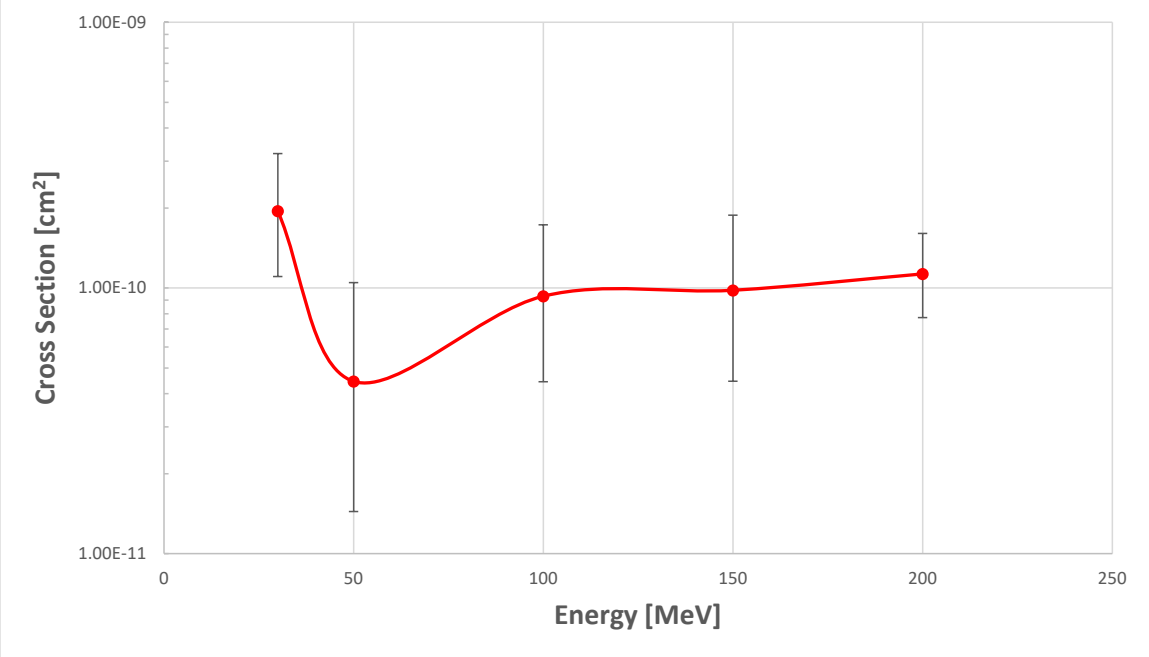


Figure 20: SEFI cross section

8. Error rate prediction

Based on the radiation results, we calculated the error rates for the **Low Earth Orbit (LEO) (800 km, 98.0° inclination)** using TRAD's OMERE software [13].

Table 22 shows the predicted rates for different error categories for the PL (CRAM SEUs, CRAM uncorrectable MBUs) and PS (L2 cache SEUs, SDCs, Crashes) parts. The PS SDCs and crashes cross-sections were calculated for two cache configurations: (a) L1 and L2 caches enabled and (b) L1 only enabled. Note that for the calculation of the PL CRAM error rates, we considered the contribution of both heavy ions and protons (since radiation experimental data for heavy ions are available from [3]), while for the PS failures only protons.

Table 22: Predicted error rates (/device/day)

Category	In-flare rate			Out-of-flare rate		
	Heay ions	Protons	Total	Heay ions	Protons	Total
PL - CRAM SEUs	1.50e+02	1.60e+02	**3.10e+02**	2.19e-01	3.03e+00	**3.24e+00**
PL - Uncorrectable CRAM MBUs	4.97e-04	1.47e+00	**1.47e+00**	5.93e-07	2.98e-02	**2.98e-02**
PS – L2 cache SEUs	-	3.54e+00	**3.54e+00**	-	7.56e-02	**7.56e-02**
PS – SDCs - L1 & L2	-	1.59e+00	**1.59e+00**	-	3.06e-02	**3.06e-02**
PS – Crashes - L1 &2	-	1.16e-01	**1.16e-01**	-	2.47e-03	**2.47e-03**
PS – SDCs- L1 only	-	1.93e-02	**1.93e-02**	-	1.55e-03	**1.55e-03**
PS – Crashes - L1 only	-	5.03e-03	**5.03e-03**	-	3.59e-04	**3.59e-04**