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1 **Executive Summary** ... 3

2 **Component Description** ... 4

3 **Heavy Ion Test Facility** ... 6

4 **Results** ... 7

5 **Shot Log** ... 8

6 **Mitigation** ... 9

7 **Weibull Parameters** ... 10

1 Executive Summary

The Everspin MR4A16BCYS35 is susceptible to SEL and SEFI, but with limits to the current supplied in the fault state, and the duration that the fault state is allowed to persist for, this need not be a hindrance to use in space. For further details see section 6.

Data is available for rate characterisation (see section 7).

To perform the tests an MCU provided the test stimulation and monitored the received data for errors of various types. The test platform included the necessary local voltage regulation components to ensure the supply voltage stayed within data sheet limits (3.3V), and a CSL system was implemented to detect and limit supply current in the event of SEL. For these tests the current limit was set to 200mA. The tests were performed at an ambient temperature of approximately 25 Celsius, however when SEL occurs the temperature is expected to rise (the tests are performed in vacuum so heat transfer only used conduction through the PCB and radiation).

2 Component Description

Manufacturer's designation: MR4A16BCYS35
Manufacturer's name: Everspin Technologies
Manufacturer's address: 5670 W. Chandler Blvd., Suite 130, Chandler, Arizona 85226
Package designation: 54-TSOP2
Component group: CMOS process
Datasheet reference: MR4A16B, rev. 11.7 March 2018

Device Date/Batch codes: H172124

"The MR4A16B is a 16,777,216-bit magnetoresistive random access memory (MRAM) device organized as 1,048,576 words of 16 bits. The MR4A16B offers SRAM compatible 35 ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20 years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. To simplify fault tolerant design, the MR4A16B includes internal single bit error correction code with 7 ECC parity bits for every 64 data bits. The MR4A16B is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.
The MR4A16B is available in a small footprint 48-pin ball grid array (BGA) package and a 54-pin thin small outline package (TSOP Type 2). These packages are compatible with similar low-power SRAM products and other nonvolatile RAM products.
The MR4A16B provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial temperature (0 to +70 °C), and industrial temperature (-40 to +85 °C) operating temperature options."

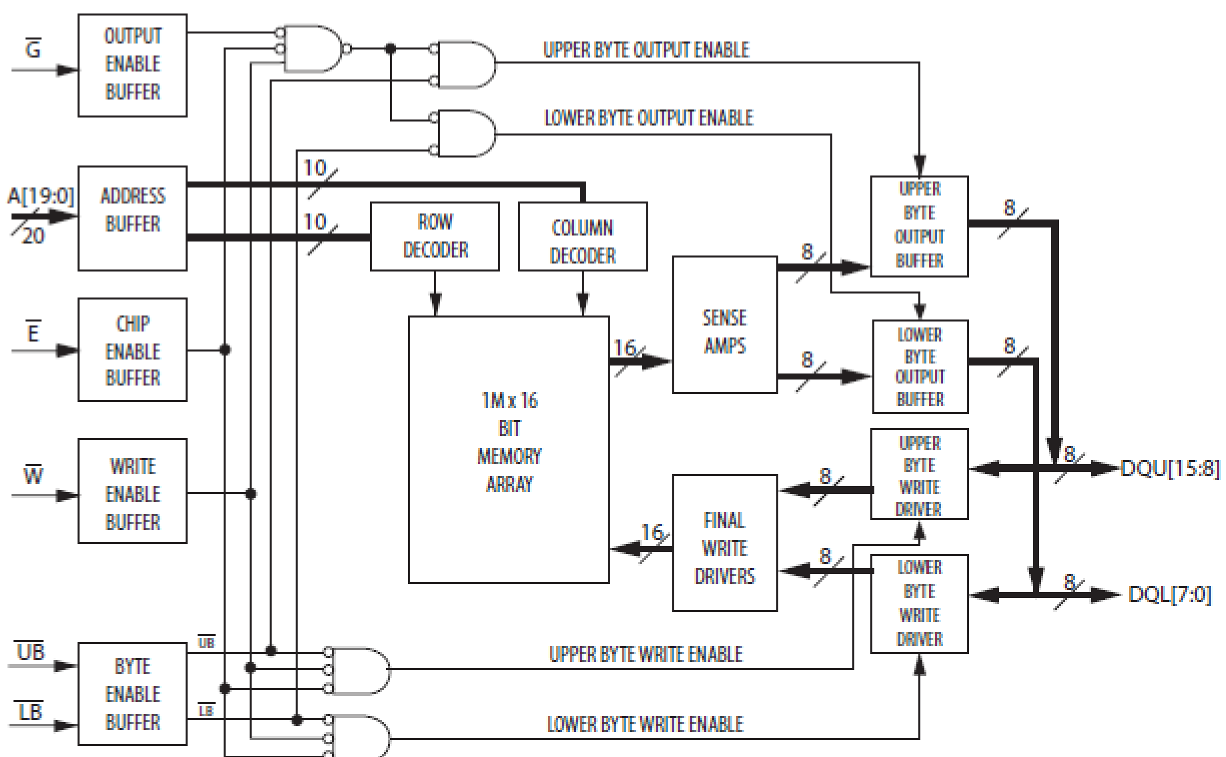


Figure 1. Logic Block Diagram

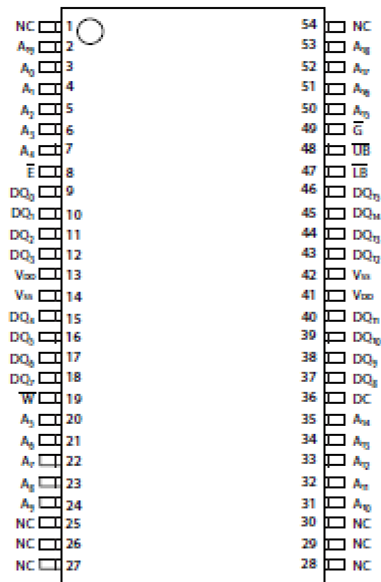


Figure 2. Pin Diagram.

3 Heavy Ion Test Facility

Heavy ion testing was performed at the Université catholique de Louvain (UCL) Heavy Ion Facility (HIF). Exposures are performed in vacuum. The facility provides one beam cocktail at 10 MeV/u. The specific species as well as their range in silicon and LET are shown in the table below.

Available particles inside the cocktail:

M/Q	Ion	DUT energy [MeV]	Range [µm Si]	LET [MeV/(mg/cm²)]
3.25	$^{13}C^{4+}$	131	269.3	1.3
3.14	$^{22}Ne^{7+}$	238	202.0	3.3
3.37	$^{27}Al^{8+}$	250	131.2	5.7
3.27	$^{36}Ar^{11+}$	353	114.0	9.9
3.31	$^{53}Cr^{16+}$	505	105.5	16.1
3.22	$^{58}Ni^{18+}$	582	100.5	20.4
3.35	$^{84}Kr^{25+}$	769	94.2	32.4
3.32	$^{103}Rh^{31+}$	957	87.3	46.1
3.54	$^{124}Xe^{35+}$	995	73.1	62.5

4 Results

The tests showed that both SEL and SEFI occurred in the test samples. The SEL was seen to be non-destructive.

The raw data for rate calculation is shown below.

Run # (UCL #)	Ion	Flux (p/cm^2/s)	Fluence (p/cm^2)	Result	Notes
8 (7)	Rh	500	3.70E+05	SEL = 51 SEFI = 0 (Sample 2)	Partially working device, for Latch-up testing only
9 (8)	Rh	2000	5.88E+05	SEL = 40 SEFI = 0 (Sample 2)	Partially working device, for Latch-up testing only
10 (9)	Rh	200	5.40E+04	SEL = 0 SEFI = 0 (Sample 1)	Fully working device (data is suspect since for this fluence these cannot both be zero – this data from this run is not used below)
11 (11)	Cr	5000	1.00E+06	SEL = 0 SEFI = 0 (Sample 1)	Fully working device
12 (12)	Kr	1000	3.50E+05	SEL = 19 SEFI = 6 (Sample 1)	Fully working device
12 (13)	Kr	1000	1.72E+05	SEL = 16 SEFI = 8 (Sample 1)	Fully working device

Cross-sections have been calculated for the various species used and have been tabulated below. Where multiple data is available (because both boards were tested) the figures have been combined.

Cross-sections (in cm^2) versus LET for SEL

Effect Type	LET = 16.1	LET = 32.4	LET = 46.1
SEL	1e-6	6.70e-5	9.50e-5

(any values shown as <1e-6 are based on an event count of 0).

Cross-sections (in cm^2) versus LET for SEFI

Effect Type	LET = 16.1	LET = 32.4	LET = 46.1
SEL	1e-6	2.68e-5	9.50e-5

(any values shown as <1e-6 are based on an event count of 0).

5 Shot Log

The table below lists all the runs performed.

Ion	Flux ($p/cm^2/s$)	Fluence (p/cm^2)	Sample	Run # (UCL #)	Notes
Rh	500	3.70E+05	2	8 (7)	Partially working device, for Latch-up testing only
Rh	2000	5.88E+05	2	9 (8)	Partially working device, for Latch-up testing only
Rh	200	5.40E+04	1	10 (9)	Fully working device
Cr	5000	1.00E+06	1	11 (11)	Fully working device
Kr	1000	3.50E+05	1	12 (12)	Fully working device
Kr	1000	1.72E+05	1	13 (13)	Fully working device

It is important to note that we operated the shutter for the beam, thus there is not direct correlation between our test runs and those logged by UCL.

6 Mitigation

It is not possible to mitigate against SEL or SEFI directly unless the system is designed for automatic error detection and correction. More precisely, EDC will not be able to correct errors because the scope of the corruption is likely to be too large needing too many bits to be corrected; but if errors are detected by EDC, that can be fixed by power cycling the devices affected.

Thought does need to be given as to how to best determine whether the data should be considered good or not. SEL may be detectable based on current rise, but SEFI cannot use this method. Both issues would be visible to scrubbing or other cell testing strategies, though this would be best done on a range of addresses spread through the device (i.e. not just on one byte). But scrubbing has latencies between tests being performed, during which the data may not be valid.

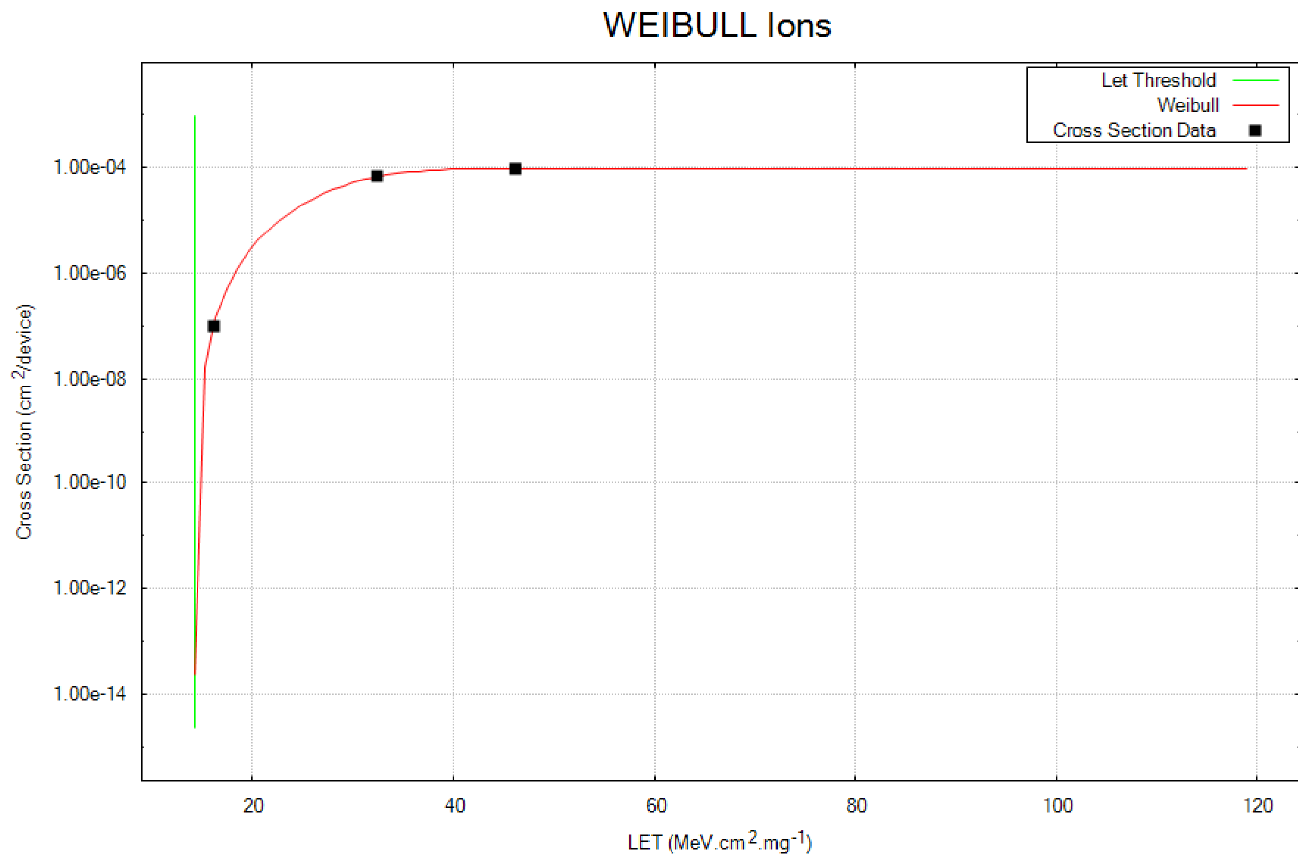
If the MRAM is the source of program information for a CPU, it is possible that code execution could be detected by the CPU crashing. To handle this a watchdog must be used and handlers for any unused vectors must be set. Locations in the device not used for code or data storage should be set to some value that would result in the watchdog being triggered (i.e. a branch to itself instruction). MRAM locations used for storing data are vulnerable to corruption without means of checking what the real contents were meant to be; and are probably undetectable.

One useful feature is that the contents of cells were not seen to be corrupted by SEL or SEFI. So power cycling should restore the contents to their pre-event condition.

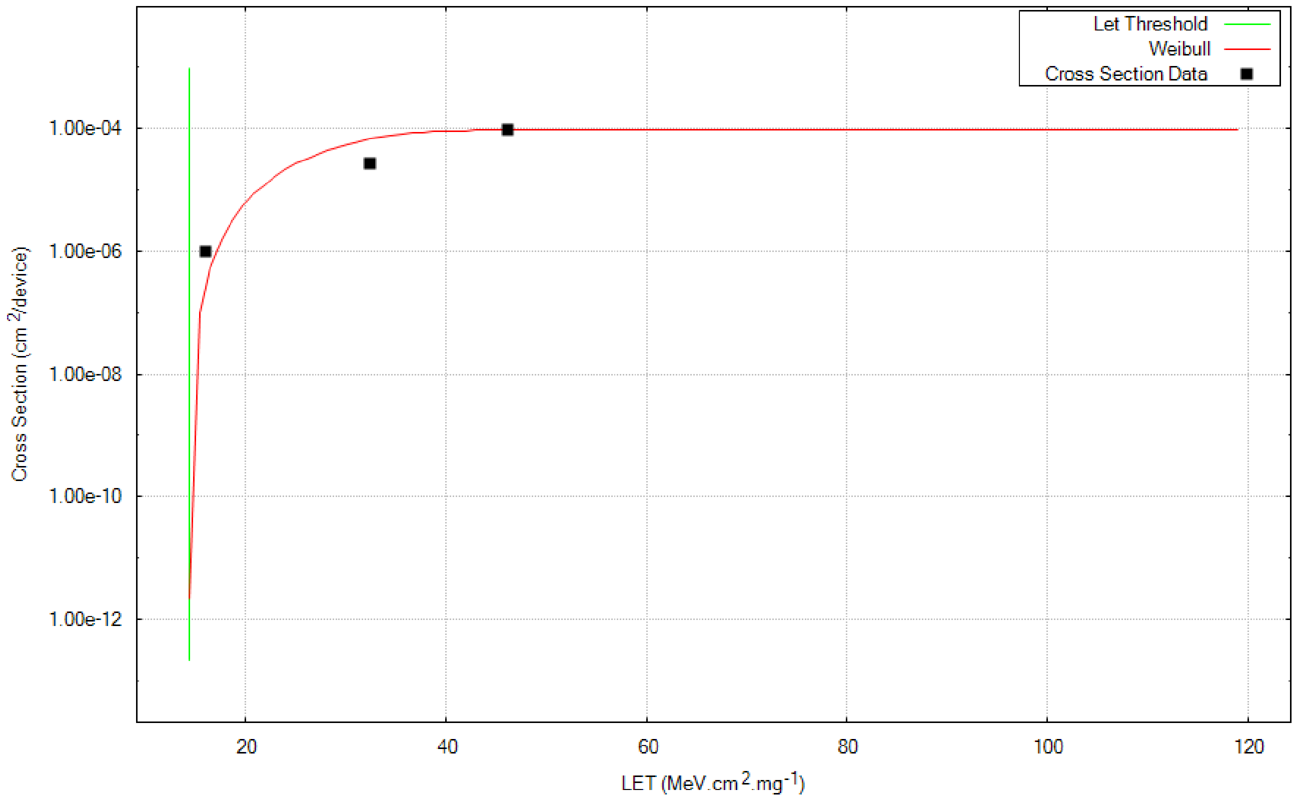
7 Weibull Parameters

The Weibull parameters have been generated using the Omere software.

Function	W	S	Limit Cross Section	LET Threshold
SEL	17.1	3.12	9.51e-5	14.2
SEFI	16.5	2.50	9.51e-5	14.5



SEL Cross Section and LET Threshold



SEFI Cross Section and LET Threshold