Heavy Ion Single Event Effects test report for Xilinx Virtex-5

2018-06-20

Doc. No GR-SEECOO1-TRP-0001

Issue 1.0

Contract 4000113697/15/NL/SW (AO 8022)

CHANGE RECORD

Issue	Date	Section / Page	Description
1.0	2018-06-20	All	First issue

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1 INTRODUCTION

1.1 Scope of the document

This document reports the results of the heavy ion test campaign for Single Event Effects (SEE) sensitivity testing of Xilinx Virtex-5 FPGA. The data presented herein was collected at a test campaign carried out at ESA's UCL(HIF) facility in Belgium on week 22 of 2018. Christian Poivey from ESA was present during the tests.

The work has been performed by Cobham Gaisler AB, Göteborg, Sweden funded by European Space Agency under ESTEC contract 4000113697/15/NL/SW (AO 8022). This document establishes the final delivery of Test plan (D3) and Test report (D4) of COO1.

The heavy ion beam time was funded by the European Space Agency.

1.2 Applicable documents

The following documents, listed in order of precedence, contain requirements applicable to the contents of the document:

[SOW] "Call of Order No. 1: Heavy Ion SEE Characterization of a Commercial SRAM based FPGA," reference TEC-QEC/CP/SOW/2014-3, issue 1, dated 13 August 2014. Published on EMITS under AO/1-8082/14/NLISW.

[ESCC25100] ESCC Basic Specification No. 25100, Issue 2, October 2014.

1.3 Reference documents

The following documents are referred as they contain relevant information:

[D1/D2] "Test Vehicle Definition – D1 and D2," Cobham Gaisler, EEE-TVD-1, issue 1, revision 1, dated 22 December 2016."

[VP] "VERI Place Experimental Validation," Cobham Gaisler, SEECOO1-AN-1, issue 1, revision 1, dated 21 April 2018.

[SEU32] "LEONFT SEU32 Test Software," Cobham Gaisler, Version 1.8, May 2018.

[GRMON] GRMON2 debug monitor for the LEON3 and LEON4 debug support units. http://www.gaisler.com/index.php/products/debug-tools/grmon2, last accessed November 2016.

2 ABBREVIATIONS

CPU	Central Processor Unit
ESA	European Space Agency
LVDS	Low Voltage Differential Signaling
PLL	Phase-looked loop
SEE	Single Event Effects
SEFI	Single Event Functional Interrupt
SEL	Single Event Latch-up
SEU/MBU/MCU	Single Event/Multiple Bit/Multiple Cell Upset
SET	Single Event Transient
TBC	To Be Confirmed
TBD	To Be Defined

3 TEST PLAN

This chapter establish the test plan for the heavy ion test report (delivery D3 of [SOW]).

The plan was to test three design variants all with the same function, but different mitigations schemed.

The designs are described in D2:

PLAIN, no mitigation

XTMR, TMR desoign

VeriPlace, TMR design post processed with the VeriPlace tool.

The FPGA configuration memory are continuously scubbed while the functionality and errors from the design are tested. However, an issue with the VeriPlace design made it in-compatible with the scrubbing engine. Thus, this design was tested without scrubbing.

All designs shall be tested with two different LETs. The LET must be low to allow the ion range reach through the thinned die (backside irradiation).

The flux shall be low to avoid error accumulation during the scrubbing cycle.

The CPU in the DUT design [D1/D2] is tested with the IU test of the SEU32 testware [SEU32]. This is a self-testing algorithm running in the CPU and reports error in the calculation to the host computer. The IU test is design to access the entire L1 cache of the CPU. In the results section of this report this test case is denoted “IU”.

The IO chain test structurs of the DUT design [D1/D2] is tested by the TC-FPGA [D1/D2] continuesly sending data pattern into each IO chain a read-out and check the return data pattern. In the results section of this report this test case is denoted “iotest”.

4 PARTS INFORMATION

4.1 Device description

One Xilinx Virtex-5 FPGA was tested with 3 different designs. The designs are defined in [VP] and [D1/D2].

This is the same device and sample tested by Cobham RAD solution in the “dry-run” performed at UCL in December 2016

5 IRRADIATION FACILITY

The heavy ion irradiation campaign reported in this document was performed at UCL/HIF facility, in Louvain-la-Neuve, Belgium, on week 22, 2018, and according to ESCC25100 specification [AD3].

The Cyclotron of the Catholic University of Louvain-la-Neuve (UCL) can provide heavy ions covering a LET range between 1.3 and 62.5 MeV.cm²/mg (please refer to http://www.cyc.ucl.ac.be/HIF/HIF.php). The HIF facility also consists of a vacuum chamber equipped with motors to allow the placement and rotation of the DUT board (Figure 3). Testing at this facility is only possible under vacuum conditions. The facility also includes several radiation detectors used to control and monitor the beam parameters. The homogeneity of the beam is ± 10% on a 25 mm diameter. The maximum ion flux achievable at this facility is limited to approximately 30,000 ions/cm²/s. The characteristics of the ions used at this facility are shown in Table 3.

Table 2. Characteristics of the used ions at UCL/HIF (vacuum conditions).

Ion	DUT energy (MeV)	Range (µm Si)	LET @ surface (MeV.cm^2/mg)
13 C 4+	131	269.3	1.3
22 Ne 7+	238	202.0	3.3
27 Al 8+	250	131.2	5.7
40 Ar 12+	379	120.5	10.0
53 Cr 16+	513	107.6	16.0
58 Ni 18+	582	100.5	20.4
84 Kr 25+	769	94.2	32.4
124 Xe 35+	995	73.1	62.5

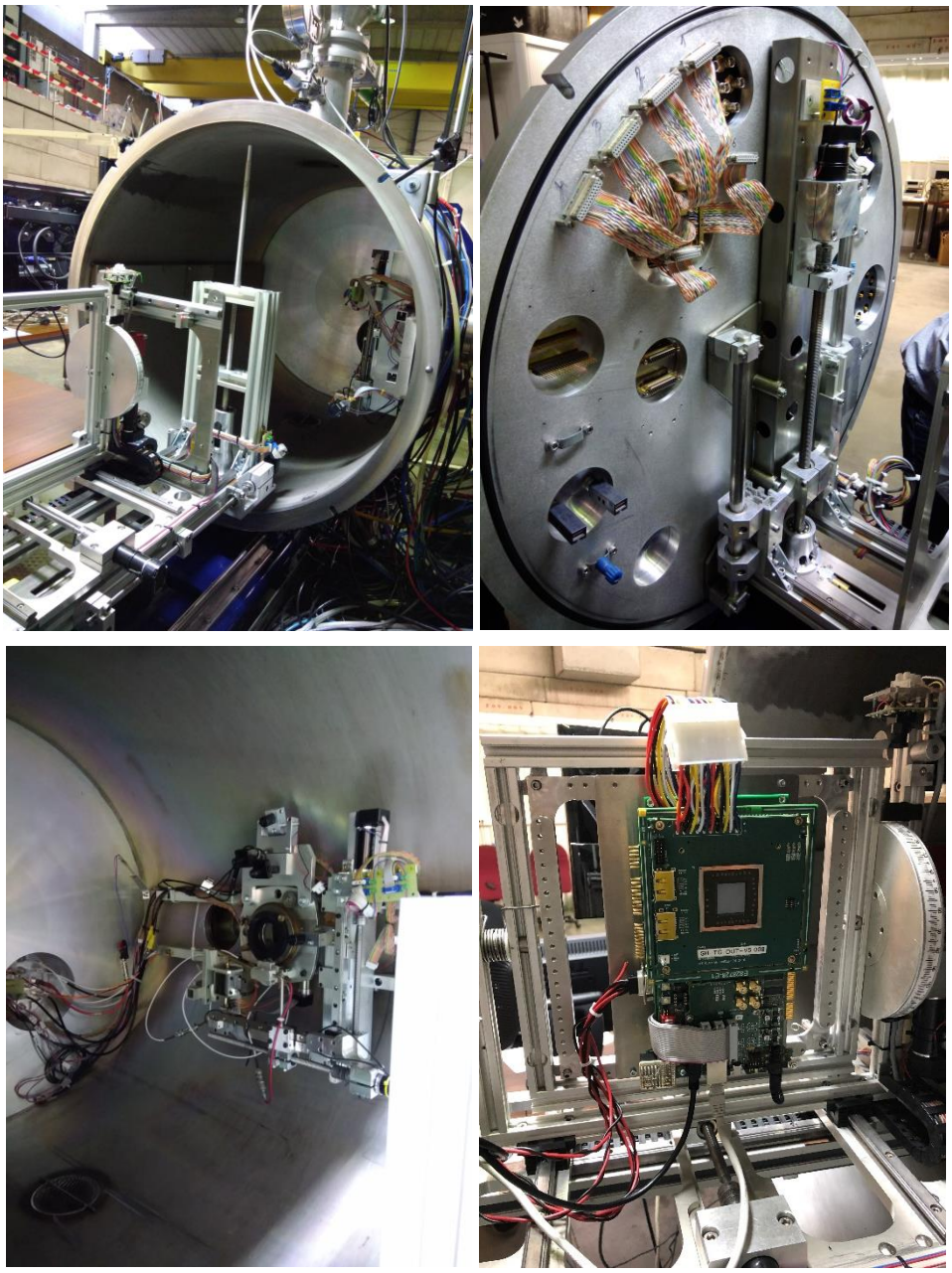


Figure 1. UCL/HIF facility.

6 TEST SETUP AND PROCEDURE

6.1 Test setup

The set-up is the same as reported by Cobham RAD solution used in “dry-run” performed at UCL in December 2016.

6.2 Test conditions

The samples were biased at nominal supply levels.

6.3 Test equipment

External supply available at UCL was used. All other equipment was developed in this project [D1/D2].

6.3.1.1 Test frequency

50 MHz clock supplied from the TC-FPGA.

7 RESULTS

Summary results and test conditions are provided in Annex A.

In total, 23 test runs were performed. All test run ended with a hang of the test system because the DUT had loss its functionality in whole or partly.

7.1 Issues in Testing

7.1.1 Fluence Accuracy

From run#115 up to run#121 each test run was stopped at 1st crash of the DUT. From run#122 the shutter available at UCL was used to temporary stop the beam, re-start the test, and then start the beam again. With this approach the error cross section could be measured more accurately. However, the time until a crash could be concluded varied meaning that the actual fluence with a test running may have been overestimated (fluence is still counting but the test system did not count errors because the DUT was not operational). The reported fluence has not been corrected considering this. However, since the flux was very low in all test runs, the error in fluence shall be rather small.

7.1.2 WDOG Recovery Circuit

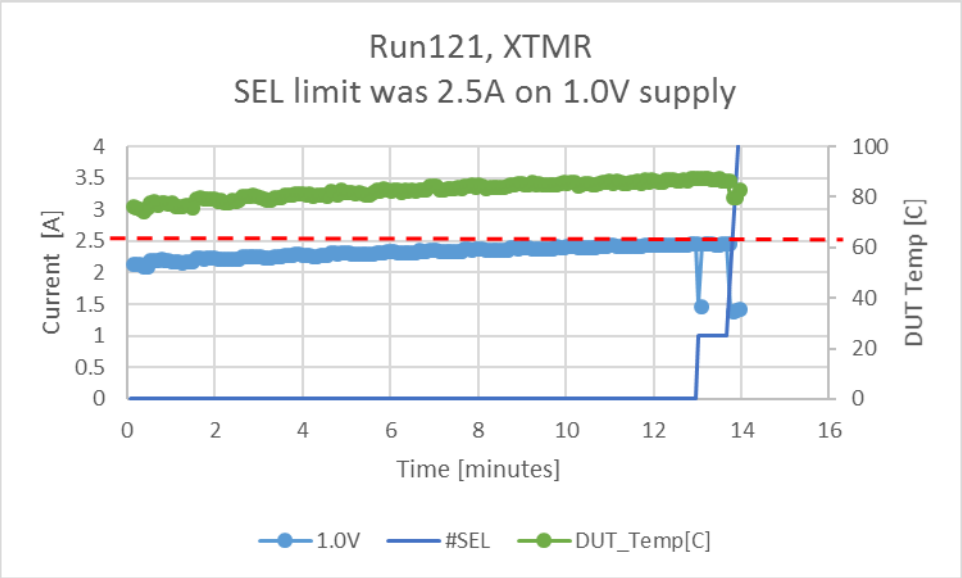
In initial runs the test system did not handle WatchDog events as intended. The WDOG signal from the DUT is monitored by the TC FPGA and the software is supposed to reset the DUT at an WDOG event but it did not.

From test run#123 the reset was handled manually be shutting off the beam and from the terminal reset the DUT and then start the beam and test again.

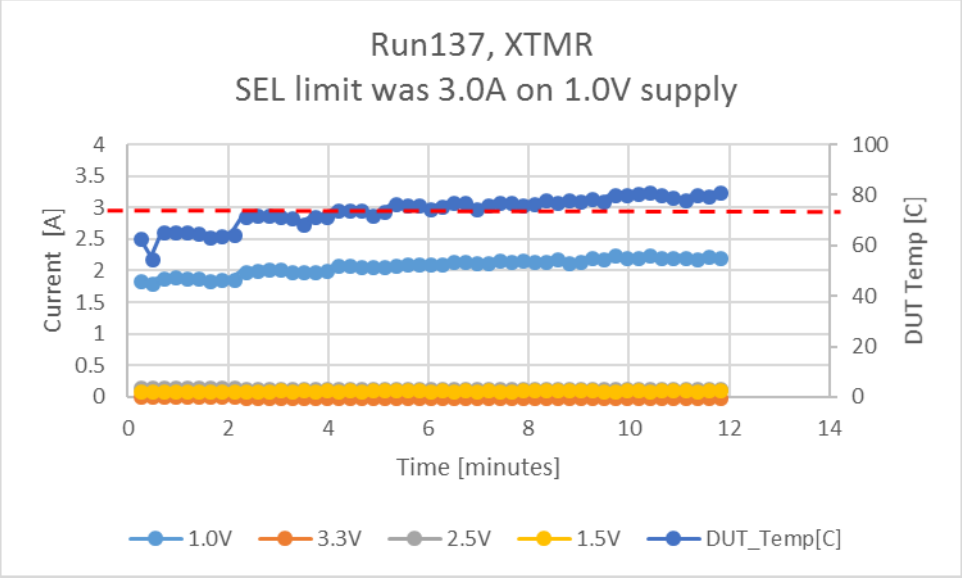
From test run#127 the test software was updated so that the Scrubbing software was monitoring the WDOG signal and automatically resetted the DUT at an WDOG event.

7.1.3 False Triggering of SEL

The test system has a SEL protection system that is configured to default value by the test software. The default value was set for ambient conditions in lab environment. During the test campaign it was not realized that sometimes the SEL triggered due to a limit set too close to the operational supply current during testing in vacuum environment. When DUT temperature increases, the supply current increases towards the SEL limit. This is illustrated with the monitoring data from run#121 below. After 13 minutes the current consumption reaches the SEL limit of 2.5A and the first SEL event is triggered.



From Run#133 and onwards the SEL limit was set to 3.0A on the 1.0V supply. No more SEL events were triggered after that. This is illustrated with the monitoring data from run#137 below.



In-post analysis the number of SEL recorded in each test run has been analysed. In Run#133, 12 false SEL events were recorded. This test run has therefore been disregarded. In other runs, the number of events were between 1 and 3 which is low compared to the number of errors recorded.

UCL RunNo	Design	#False SEL	SEL limit on 1.0V [A]
121	XTMR	2	2.5
127	XTMR	1	2.5
129	XTMR	3	2.5
132	PLAIN	2	2
133	XTMR	12	2.5

Notice that mostly XTMR designs recorded false SEL events, which make sense because this design is the largest and thus has the highest current consumption. Only in one case, the PLAIN design triggered two false SEL events, but in that test run the current limit had been set to 2.0A by mistake.

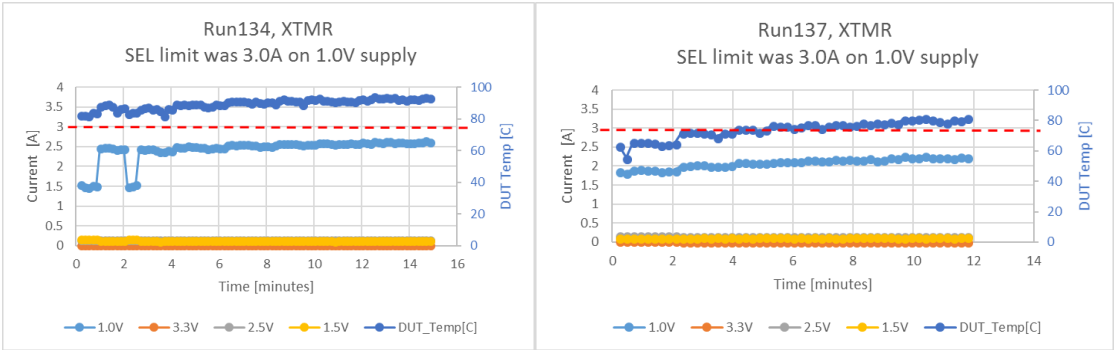
7.1.4 DUT's Temperature Influence on Errors

As illustrated in the figure above the DUT temperature became rather high during the test campaign. No active cooling exists in the test system, so all power loss must be dissipated via the PCBs to the metal structures inside the vacuum chamber.

The DUT temperature varied between 49 degreee Celsius and 94 degreee Celsius with the highest temperature recorded in Run#134.

We suspected that the high temperature could have an influence on the error rates. Thus Run#134 was repeated in Run#137 with the same test conditions but after allowing the system to cooldown before starting the test.

Monitoring data is given below for the two runs giving evidence that both temperature and supply current reduced significantly in Run#137.

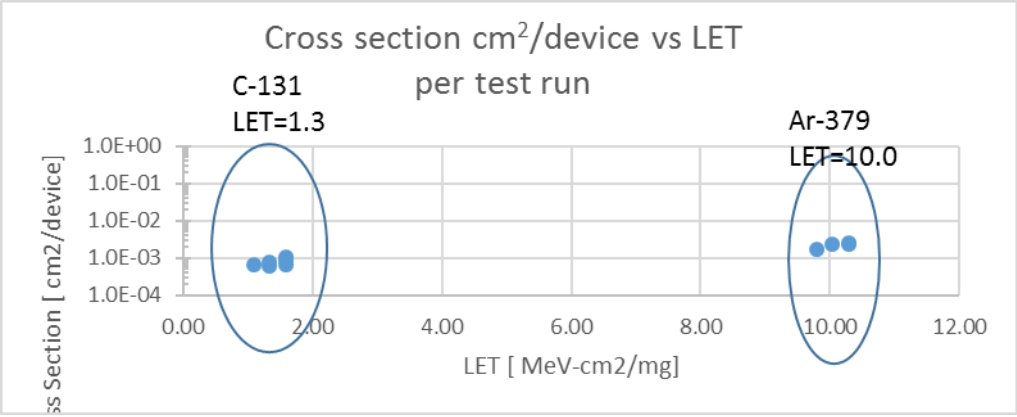


However, it had no impact of the number of errors recorded. E.g the recorded error cross section for fails of the CPU was 2.6e-3 cm2/device and 2.9e-3 cm2/device for run#134 and run#137, respectively. The LET was 10 MeV-cm2/mg in these runs. These error rates are much higher than it can expected for an XTMR design.

7.2 Results of the CPU

In graph below the overall cross section for CPU errors are reported (Traps, WDOG events, hangs). No data errors of the IU test was recorded. The data points are stretched on the x-axis to visualize the results of the three designs. From left is the PLAIN, next the VeriPlace and on the right is the XTMR design.

Notice that the VeriPlace design were tested without the scrubbing of the configuration memory.

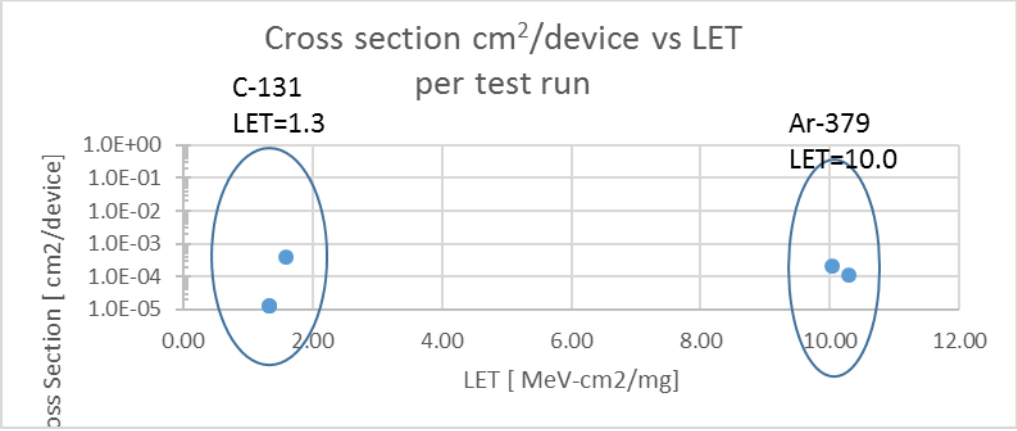


UCL RunNo	TestCase	SCRUB	Design	LET	Errors	Cross section
122	IU	No	VeriPlace	1.30	14	7.73E-04
123	IU		XTMR	1.30	15	7.69E-04
124	IU(mem)		XTMR	1.30	15	1.18E-03
125	IU		PLAIN	1.30	12	8.94E-04
126	IU		PLAIN	1.30	17	6.94E-04
127	IU & iotest		XTMR	1.30	3	1.20E-03
128	IU		XTMR	1.30	15	9.87E-04
134	IU & iotest		XTMR	10.00	10	2.64E-03
135	IU & iotest		PLAIN	10.00	22	2.80E-03
136	IU & iotest	No	VeriPlace	10.00	9	2.00E-03
137	IU & iotest		XTMR	10.00	8	2.90E-03

Run#124 was tested with the L1 cache disabled meaning that the CPU is running with no internal memory but only with the external memory.

7.3 Results of the IO Chain Test Structures

The IOTEST software tested the IO Chain test structures in the DUT design. Most errors were burst of errors meaning that the functionality of one or more IO chains was lost. In some cases, it recovered immediately but sometimes the functionality was lost. It is believed it recovered only after reseting the DUT and the test system. In below grapth results for burst events are presented for PLAIN design (left) and XTMR (right).



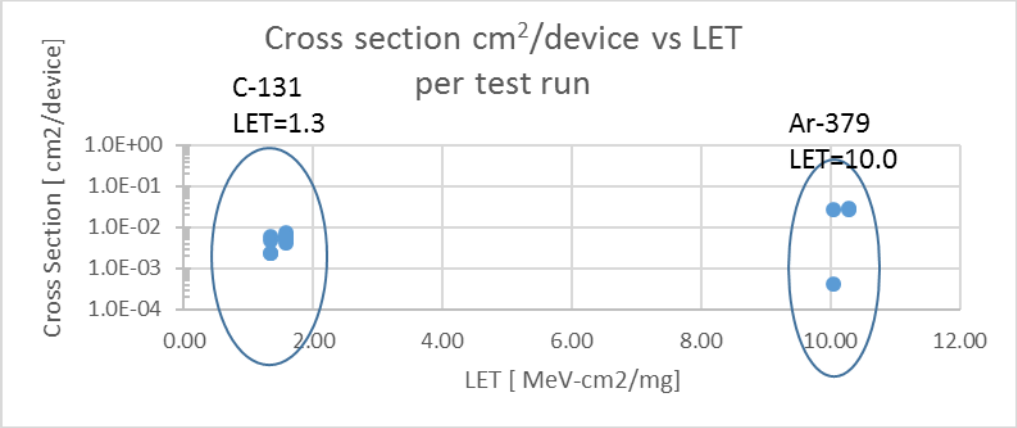
UCL RunNo	TestCase	Design	LET	IOTEST_Burst	Cross section
129	iotest	XTMR	1.30	1	8.06E-05
130	iotest	PLAIN	1.30	4	1.59E-05
131	iotest	PLAIN	1.30	15	1.50E-05
132	iotest	PLAIN	10.00	41	2.05E-04
133	iotest	XTMR	10.00	5	5.00E-05

In the PLAIN desing single bit upsets were recorded (one single bit error in one chain): 1 event in Run#130 and 5 events in Run#132.

The VeriPlace design was tested with the IOTEST in one run (Run#136) with similar results as for the XTMR and VeriPlace design.

7.4 Results of the Configuration Memory

The FPGA configuration memory is continuously scrubbed and then readback and checked for errors. The cycle takes 175ms. All errors were saved to log file. However, the error data is complex to analyse, considering all crashes of the DUT. In a trial to estimate the amount of upsets of the configuration memory the number of events in the readback data has been counted. Only events with separated in time with a complete scrubbing and readback cycle without errors were counted. The event cross section is presented in the graph below for PLAIN design (left) and XTMR (design) on the right.



UCL RunNo	TestCase	Design	LET	CfgMem Events	Cross section	#CfgMem events/CPU Errors
120	IU	XTMR	1.30	8	4.9E-03	8.0
123	IU	XTMR	1.3	115	5.9E-03	7.7
124	IU(mem)	XTMR	1.30	79	6.2E-03	5.3
125	IU	PLAIN	1.3	37	2.8E-03	3.1
126	IU	PLAIN	1.30	172	7.0E-03	10.1
128	IU	XTMR	1.3	103	6.8E-03	6.9
129	IU & iotest	XTMR	1.30	105	8.5E-03	
130	IU & iotest	PLAIN	1.3	1440	5.7E-03	
131	IU & iotest	PLAIN	1.30	2755	2.8E-03	
132	IU & iotest	PLAIN	10	99	5.0E-04	
134	IU & iotest	XTMR	10.00	117	3.1E-02	11.7
135	IU & iotest	PLAIN	10	247	3.1E-02	11.2
137	IU & iotest	XTMR	10.00	95	3.4E-02	11.9

In the right most column in above table, the average number of events recorded in the Configuration Memory per each CPU error (Traps, WDOG events, hangs etc) are reported. This is much higher than expected from simulaton of the designs [VP].

8 CONCLUSIONS

None of the designs tested under radiation performed as expected. The XTMR design is expected to mitigate errors but it seems not to do. Both design blocks (the procesor core and the IO chain test structures) had higher error rates than expected.

It seems that the scrubbing of the configuration memory was not running but it was verified that it did: After a crash the beam was stopped, the CPU was reset while the scrubbing of the configuration memory was running, and the functionality was recovered. Moreover, the burst events in the IOTEST is an evidence that functionality could be automatically recovered.

9 ANNEX A; TABLE WITH ALL TEST RESULTS FROM THE IRRADIATION AT UCL(HIF)

UCL RunNo	TestCase	Scrub	Design	Beam Ctrl	fluence	flux	runTime	Ion	LETeff	CPU Trap/WD/PLL	CPU Hang/burst	CfgMem Events	IOTEST Single	IOTEST Burst	IOTEST Hang
115	IU		PLAIN	F2F	8871	102	87	C-131	1.3	0	1	64	0	1	
116	IU		PLAIN	F2F	3080	18	167	C-131	1.3	1	0	13	0	0	
117	IU		PLAIN	F2F	3674	33	110	C-131	1.3	0	1	22	0	0	
118	IU		PLAIN	F2F	616	14	44	C-131	1.3	0	1	1	0	0	
119	IU		PLAIN	F2F	877	24	36	C-131	1.3	0	1	9	0	0	
120	IU		XTMR	F2F	1616	17	94	C-131	1.3	0	1	8	0	0	0
121	Scrub only		XTMR		75825	93	816	C-131	1.3	0	1	460	0	1	1
122	IU	No	VeriPlace	shutter	18149	24	767	C-131	1.3	3	11	na	na	na	
123	IU		XTMR	shutter	19475	39	505	C-131	1.3	4	11	115	na	na	
124	IU(mem)		XTMR	shutter	12716	32	403	C-131	1.3	2	13	79	na	na	na
125	IU		PLAIN	shutter	13425	5	2889	C-131	1.3	7	5	37	na	na	
126	IU		PLAIN	shutter	24463	20	1215	C-131	1.3	6	11	172	na	na	
127	IU & iotest		XTMR	F2F	2512	19	131	C-131	1.3	2	1	24	0	0	2
128	IU		XTMR	shutter	15182	18	860	C-131	1.3	4	11	103	1	4	0
129	Iotest		XTMR		12438	34	368	C-131	1.3	0	1	105	0	1	5
130	Iotest		PLAIN	shutter	251552	81	3090	C-131	1.3	0	1	1440	1	4	0
131	iotest		PLAIN		1000783	504	1987	C-131	1.3	0	1	2755	0	15	0
132	iotest		PLAIN		200313	314	638	Ar-379	10	0	1	99	5	41	9
133	iotest		XTMR	shutter	100108	60	1670	Ar-379	10	0	1	537	0	5	8
134	IU & iotest		XTMR	shutter	3785	7	517	Ar-379	10	4	6	117	0	0	2
135	IU & iotest		PLAIN	shutter	7856	12	632	Ar-379	10	13	9	247	1	2	
136	IU & iotest	no	VeriPlace	shutter	4510	8	588	Ar-379	10	3	6	na	1	6	1
137	IU & iotest		XTMR	shutter	2756	4	613	Ar-379	10	2	6	95	0	8	0