



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **1/44**

Other reference :	ESTEC/Contract N° 4000102571/10/NL/AF
Type :	
Description :	Radiation Characterization of LAPLACE/TANDEM RH Optocouplers, Sensors and Detectors
Title of document :	HAS2 TID Report

	Names	Dates
Prepared by	VAN AKEN Dirk (ON Semiconductor) HERVE Dominique (Sodern) BEAUMEL MATTHIEU (Sodern)	23/11/2012
Checked by	-	-
Approved by	-	-
Customer approval	-	-



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **2/44**

CHANGE RECORD

Revision	Description of change
A	First issue
B	Added witness part test results



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **3/44**

TABLE OF CONTENTS

1.	SCOPE AND APPLICABILITY	4
1.1.	SCOPE	4
1.2.	PURPOSE	4
2.	REFERENCES	4
2.1.	APPLICABLE DOCUMENTS	4
2.2.	REFERENCE DOCUMENTS	4
3.	ABBREVIATIONS	5
4.	DEVICE INFORMATION	6
4.1.	HAS2 PRESENTATION	6
4.2.	SAMPLES IDENTIFICATION	8
5.	IRRADIATION FACILITY	9
6.	TEST SETUP	10
7.	TEST PLAN	12
8.	EXPERIMENTAL RESULTS	13
8.1.	REPORTED PARAMETERS.....	13
8.2.	OBSERVATIONS	14
8.2.1.	Dark Current	15
8.2.2.	Temporal Noise in DR Mode – hard reset	20
8.2.3.	Temporal Noise in DR Mode – hard to soft reset.....	21
8.2.4.	Temporal Noise in NDR Mode – hard reset.....	22
8.2.5.	Temporal Noise in NDR Mode – hard to soft reset	23
8.2.6.	Global Fixed Pattern Noise – hard reset.....	24
8.2.7.	Global Fixed Pattern Noise – hard to soft reset	25
8.2.8.	Local Fixed Pattern Noise – hard reset	26
8.2.9.	Local Fixed Pattern Noise – hard to soft reset	27
8.2.10.	Global Photo Response Non Uniformity	28
8.2.11.	Local Photo Response Non Uniformity	29
8.2.12.	Operating Current	30
8.2.13.	Standby Current.....	31
8.2.14.	DSNU.....	32
8.2.15.	INL	33
8.2.16.	DNL.....	34
8.2.17.	Electro Optical Measurements	35
8.2.18.	Calibration Parameters.....	40
9.	CONCLUSIONS	44



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **4/44**

1.SCOPE AND APPLICABILITY

1.1.Scope

This test report presents the results of the TID irradiation testing on the HAS2 CMOS image sensor, performed in the frame of the ESTEC contract N° 400 0102571/10/NL/AF "Radiation Characterization of Laplace/Tandem RH optocouplers, sensors and detectors".

The TID irradiations were performed at the ESTEC Co-60 source in October 2011. The annealing steps at room temperature and elevated temperatures were performed at ON Semiconductor.

1.2.Purpose

The effect of TID radiation and annealing is studied on the HAS2 in the ON and OFF state in all different possibilities such as ON during radiation and OFF during annealing etc...

2.REFERENCES

2.1.Applicable documents

[AD 1] ITT 6429 HAS Irradiation Test Plan, PR__00004584, D

2.2.Reference documents

[RD1] Radiation Test Summary

[RD2] HAS Low Dose Rate Radiation Test Report

[RD3] HAS TID Report 2007 Evaluation Campaign



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **5/44**

3.ABBREVIATIONS

AD	Applicable Document
APS	Active Pixel Sensor
CDS	Correlated Double Sampling
CMOS	Complementary Metal-Oxide Semiconductor
DC	DateCode
DDD	Displacement Damage Dose
DR	Destructive Readout
DS	Double Sampling
DSNU	Dark Signal Non Uniformity
ECSS	European Cooperation for Space Standardization
EOL	End Of Life
ESA	European Space Agency
FPN	Fixed Pattern Noise
HAS2	High Accuracy STR 2
LET	Linear Energy Transfer
LSB	Least Significant Bit
N/A	Not Applicable
NDR	Non-Destructive Readout
PCB	Printed Circuit Board
RD	Reference Document
SEE	Single Event Effect
SET	Single Event Transient
SEU	Single Event Upset
SEFI	Single Event Failure interrupt
TID	Total Ionizing Dose



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **6/44**

4.DEVICE INFORMATION

4.1.HAS2 presentation

The Accuracy STR 2 sensor (HAS2) is a 1024 x 1024 pixel rolling shutter Active Pixel Sensor (APS), featuring a programmable (gain and offset) output amplifier (PGA) and an internal 12 bits ADC.

The CMOS image was sensor designed and manufactured by ON Semiconductor¹ under ESA contract 17235/03/NL/FM for star tracker applications.

The block diagram of HAS2 is presented in Figure 4-1.

Pixel design is based on a photodiode coupled with a three transistor readout circuit. The HAS2 is the descendant from a lineage radiation-hardened by design sensors from ON Semiconductor: the photodiodes includes a doped surface protection layer to prevent the depleted area from reaching the field oxide interface, while the CMOS readout circuitry is designed using enclosed geometry transistor layouts.

The wafers are produced by Plessey Semiconductors² on the standard XC035P311 CMOS process (0.35 μ m).

In order to reduce the variation in signal offset from pixel to pixel (known as Fixed Pattern Noise, or FPN) typically seen on APS, the HAS2 implements two different noise reduction techniques: Double Sampling (DS) also called Destructive Readout (DR) and Correlated Double Sampling (CDS) also called Non Destructive Readout (NDR). In DR mode, the pixel is reset at the end of the signal integration time in order to sample the pixel reference level. The reference level is subtracted from the signal level in order to cancel the pixel offset. This internal analog operation is performed before digitization. In NDR mode, two images are sampled and digitized: a reference image at the beginning of the integration time, and a signal image at its end. Offset correction must be performed off-chip by subtracting these two images.

A temperature sensor is also integrated on chip, which can be addressed through an internal multiplexer. This MUX can also address analogue inputs to be digitized by the internal ADC.

¹ Formerly Cypress BVBA and Fillfactory.

² Formerly X-FAB.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012

Séq. : 1

Statut : **Final**

Classification: NC Page : **7/44**

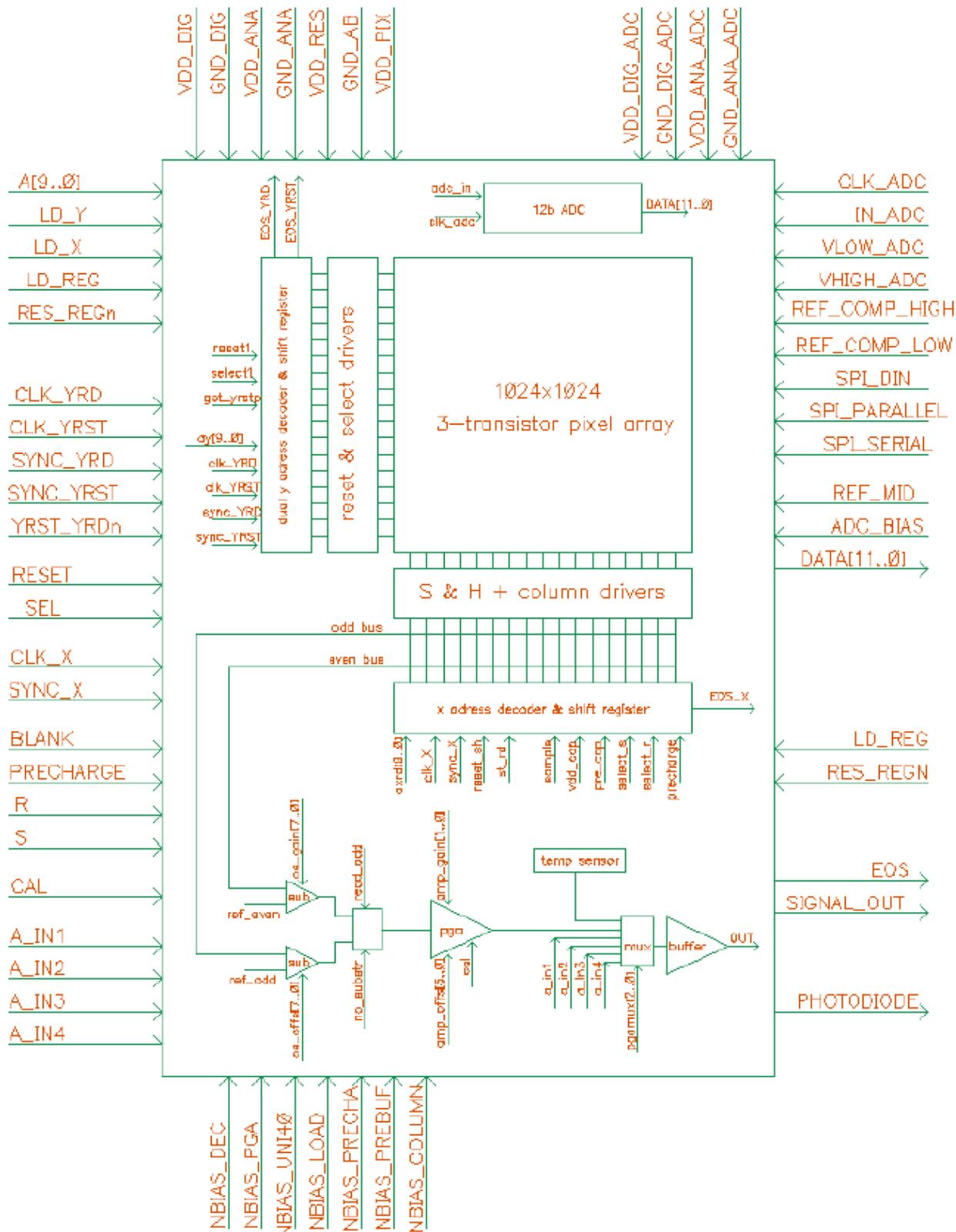


Figure 4-1 : HAS2 block diagram



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **8/44**

4.2.Samples identification

Part type: HAS2
Manufacturer: ON Semiconductor
Package: JLCC84
Tested Samples:

164 Reference sample used during HAS ESCC evaluation campaign
689 Sample from wafer lot P29506.1
572 Sample from wafer lot P20291.1
698 Sample from wafer lot P29506.1
566 Sample from wafer lot P20291.1
713 Sample from wafer lot P29506.1
569 Sample from wafer lot P20291.1
688 Sample from wafer lot P29506.1
705 Sample from wafer lot P29506.1
717 Sample from wafer lot P29506.1
570 Sample from wafer lot P20291.1
679 Sample from wafer lot P29506.1
541 Sample from wafer lot P20291.1
580 Sample from wafer lot P20291.1
723 Sample from wafer lot P29506.1
741 Sample from wafer lot P29506.1
88 Sample from wafer lot P20291.1, 2007 ESCC evaluation lot
687 Sample from wafer lot P29506.1
739 Sample from wafer lot P29506.1
696 Sample from wafer lot P29506.1
576 Sample from wafer lot P20291.1
575 Sample from wafer lot P20291.1
73 Sample from wafer lot P20291.1, 2007 ESCC evaluation lot
731 Sample from wafer lot P29506.1
697 Sample from wafer lot P29506.1

Samples from wafer lot P29506.1:

Backside marking: NOIH2SM1000A HHC (Engineering Models)
Date code: 110414 (April 14, 2011)

Samples from wafer lot P20291.1:

Backside marking: NOIH2SM1000A HHC (Engineering Models)
Date code: 110414 (April 14, 2011)

Samples from wafer lot P29506.1 (2007:

Backside marking: NOIH2SM1000A HHC (Engineering Models)
Date code: 110414 (April 14, 2011)

Sample 679, 713 and 741 were taken out of the beam after 55.1KRad for later use during SEE testing.

All samples have been subjected to an operational burn in step at +125 degC during 168h.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **9/44**

5.IRRADIATION FACILITY

Radiations were performed at the ESTEC CO-60 radiation facility. Detailed information on the dosimetry can be found in the irradiation test campaign details report (ref. RD1).

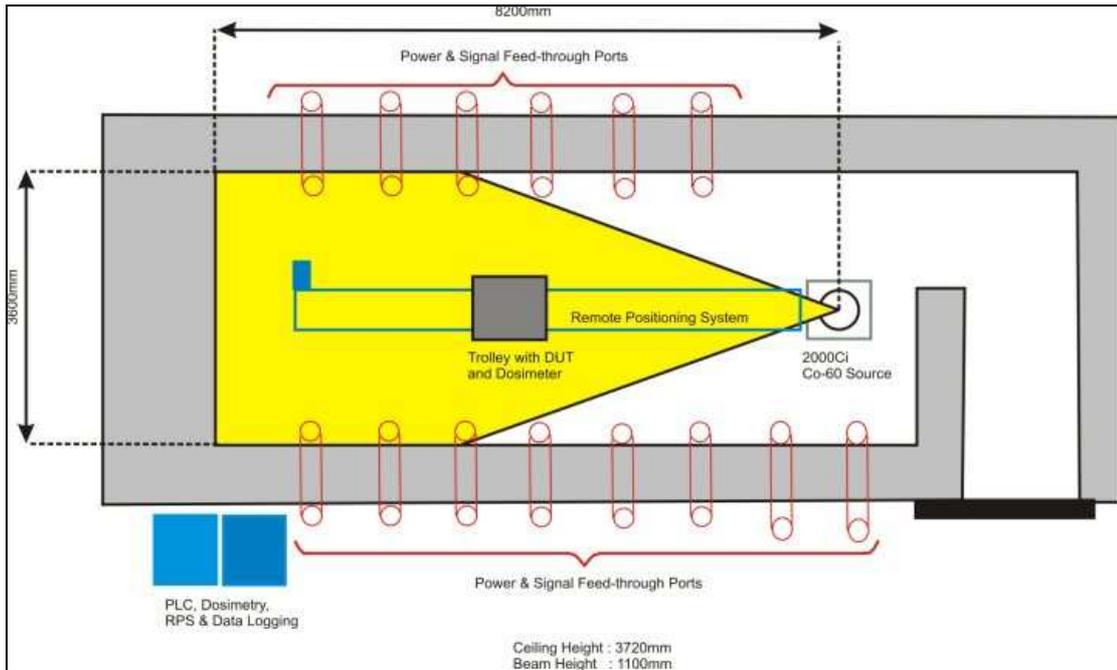


Figure 5-1: ESA-ESTEC Co-60 radiation room layout



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **10/44**

6. TEST SETUP

The irradiations and electrical characterizations have been performed at room temperature. Image acquisition was done using dedicated driving boards and acquisition system.

The figure hereafter presents the geometry of the irradiation setup.

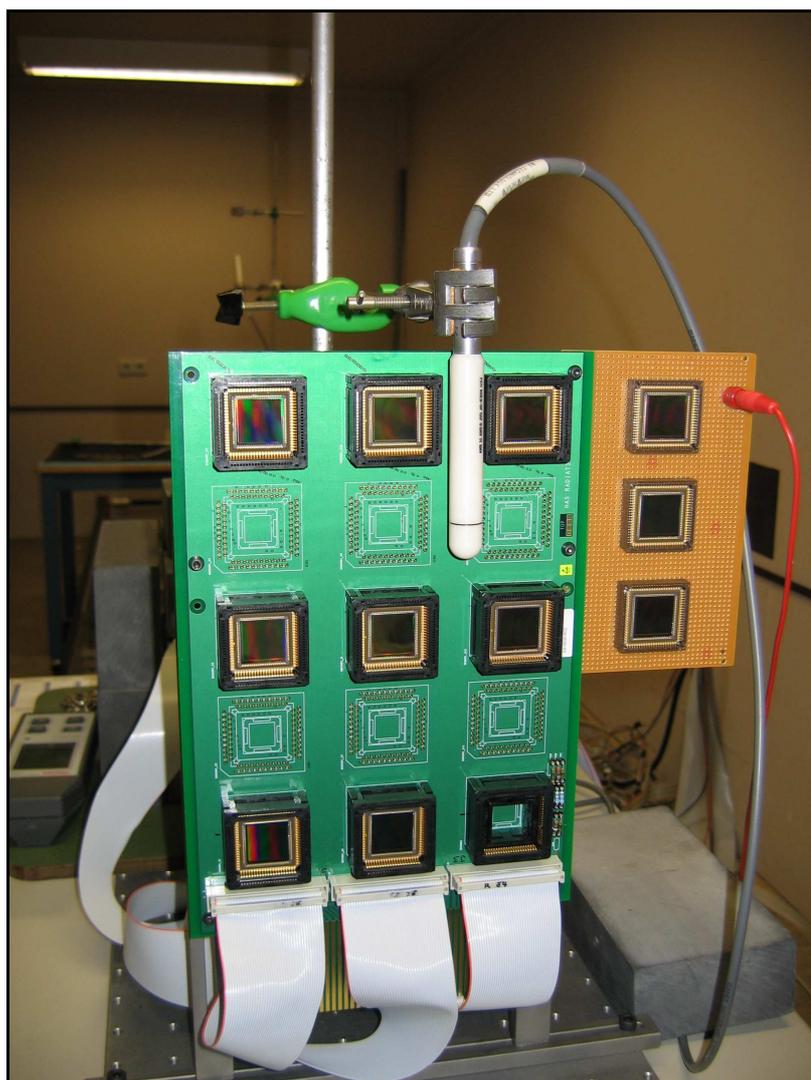


Figure 6-1 : HAS Irradiation Test Setup

The HAS2 is operated under beam in Soft Reset condition.

The camera system consists in 4 main components (Figure 6-2). The boards implemented in the system are detailed hereafter:

- A digital controller runs the image sensor controller, the frame grabber and the communication to a PC.
- A cable interface board contains the controllable power supplies, cable line drivers to drive the control signals to the DUT and receivers that receive the video signal from the DUT.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **11/44**

- A cable receiver board receives the driving signals from the controller and also contains buffers to drive the video signal to the 5 meter long cable.
- A radiation/burn-in board contains the DUT. The DUT returns a video signal to the controller.

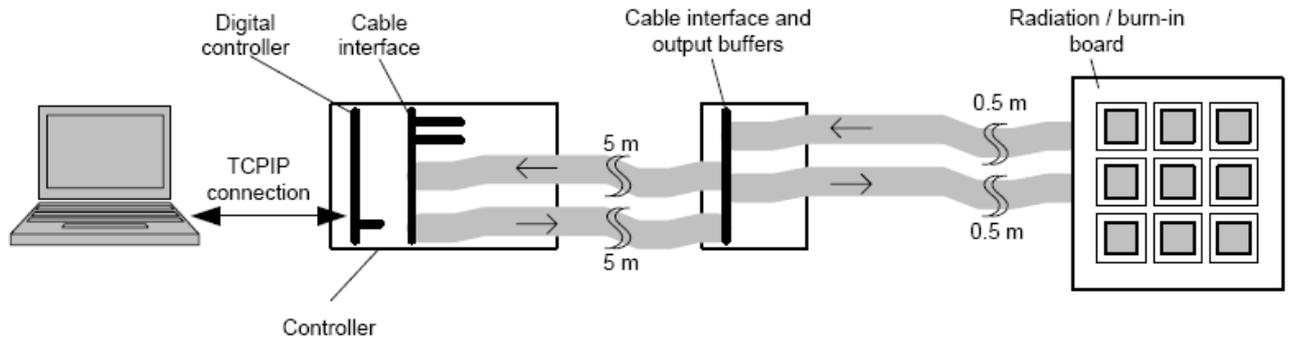


Figure 6-2 : Overview of the HAS2 test setup

During irradiation the device supply currents are monitored separately. In case of abnormal drift or device failure, the following parameters can be logged: power supply where the drift condition occurred, time when the condition occurred, and drift current. In case of latch-up the current supplied to the device is limited to a safe value in order to prevent damage.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **12/44**

7. Test Plan

Electrical measurements are performed at the following steps:

- Initial characterization
- 8.1 KRad
- 31.5 KRad
- 55.1 KRad
- 78.6 KRad
- 144.5 KRad
- 3 months room temperature annealing (measurements on a weekly basis)
- 1 month 50 degC annealing (measurements twice a week)
- 168 hours 1250 degC annealing (measurements every 24h)

Next to the electrical testing, electro optical testing is performed before radiation and after 144.5 KRad. Electro-optical testing is not performed after the two annealing steps.

Devices have been irradiated using the following bias conditions:

Condition Item	Bias State during Irradiation test campaign	Bias state during Post irradiation annealing	Serial Numbers
A	ON	ON	688, 717, 723
A2	ON	ON	541, 566
B	ON	OFF	698, 705,
B2	ON	OFF	569, 570, 572
C	OFF	ON	689, 697, 731
C2	OFF	ON	73, 575, 576
D	OFF	OFF	687, 696, 739
D2	OFF	OFF	88, 580

The samples used for A, B, C and D are issued from the same wafer lot (ref. Section 2.4). The samples used for condition A2, B2, C2 and D2 are issued from the wafer lot used during the ESCC HAS2 evaluation campaign.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **13/44**

8.EXPERIMENTAL RESULTS

8.1.Reported parameters

The following electrical parameters are reported in the next paragraphs:

- Temporal noise in DR mode (hard reset, hard to soft reset)
- Temporal noise in NDR mode (hard reset, hard to soft reset)
- Offsets (in particular DR mode odd/even offset difference and NDR mode offset dispersion – mean, standard deviation, register value)
- Fixed pattern noise (FPN) local and global (hard reset, hard to soft reset)
- Dark current
- Dark current non uniformity local and global
- Photo response non uniformity local and global
- Temperature sensor output
- Supply currents
- ADC Performances (INL, DNL)

The following electro-optical parameters are measured:

- Spectral Response
- FTM
- Linearity and full well capacity
- Conversion factor
- Dark signal temperature dependency
- Lag performance



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **14/44**

8.2.Observations

We have been facing quite some serious issues during the execution of the work. First of all there was the test equipment failure during the irradiation campaign at ESTEC. During the electrical tests in between the irradiation campaigns some strange behavior was observed on the parts: some of the parts were showing high operating current, other parts gave some contact test issues, some parts were showing zero dark current increase, and so on. By retesting the parts until good and expected data was achieved we could minimize the damage. Investigations later on pointed out that the issue was due to a broken contact pin which was probably introduced during the travel of the equipment from Belgium to ESTEC.

The second issue we had was the mix-up of integration time settings for the dark current image. The tester used for this test campaign was also used for the neutron irradiated devices and was also used for production testing. Every type of test required its own integration time setting for the dark current. Unfortunately this issue was only been seen during the 11th week of the room temperature annealing. But, as there was no difference seen between the first and the 11th week of the room temperature annealing, no crucial data have been lost!

The graphs which will be shown in the next paragraphs' needs to be interpreted with care due to the above.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **15/44**

8.2.1. Dark Current

The following graph is displaying the average dark current behavior of the 8 different biasing conditions.

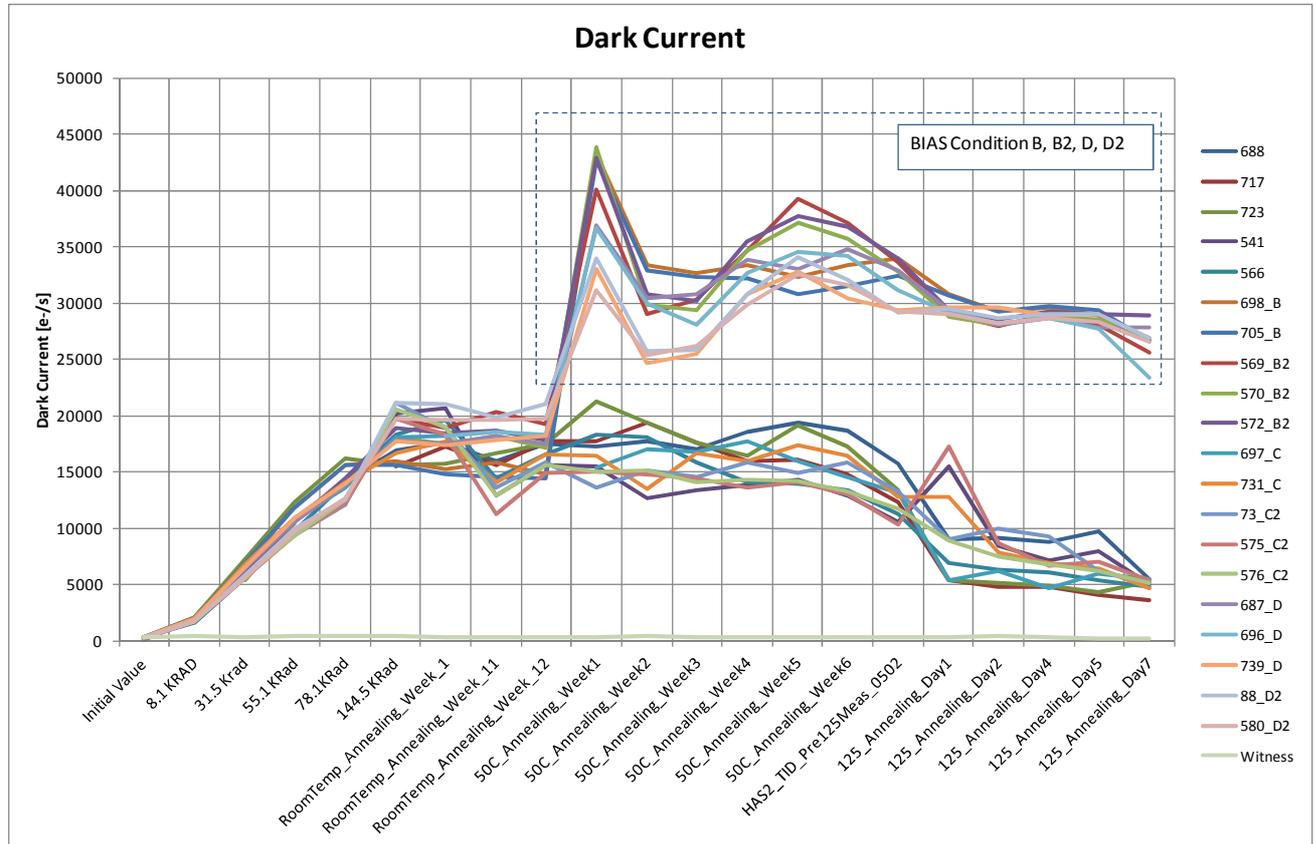


Figure 8-1: Dark Current vs radiation and annealing for different bias conditions

The following observations are made:

- Dark current increases the same for all the samples, independent from the wafer lot, independent from the biasing conditions.
- Dark current does not change significantly during room temperature annealing for the devices in the ON condition.
- Dark current increases significantly for after 1 day of 50 degrees C annealing for the OFF biasing condition (B, B2, D and D2), and is quite unstable during this annealing period.
- Dark current drops during 125degC annealing for both the biased and unbiased condition.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **16/44**

8.2.1.1. Distributions

The graph below is showing the DSNU distributions for device ID 88 which was in the OFF state during radiation and annealing. Please note that the below curves have an integration time of 3 seconds.

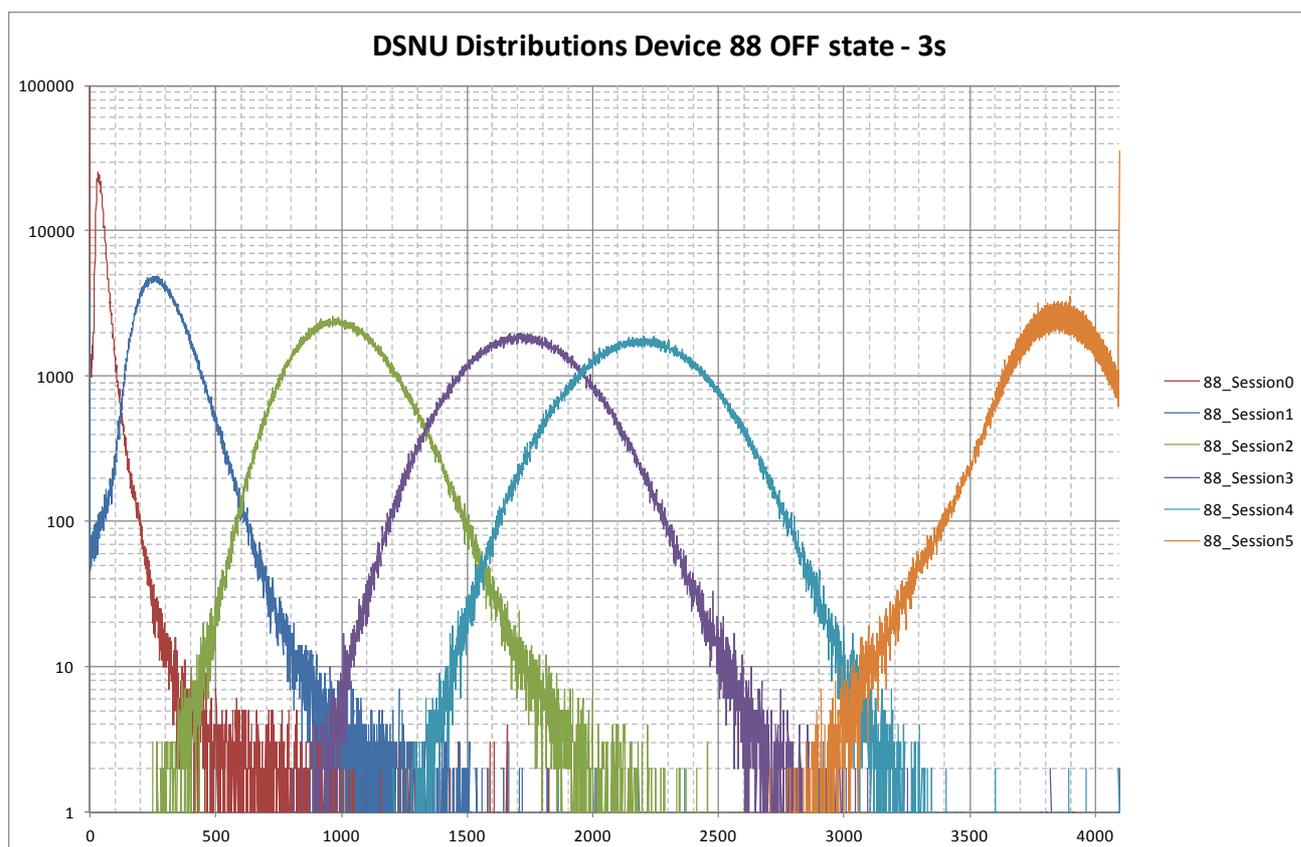


Figure 8-2: DSNU distributions for device 88

The next graph is also showing the DSNU distributions for device 88 but this time after room temperature, 50C and 125C annealing. For these distributions an integration time of 1 second was applied.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **17/44**

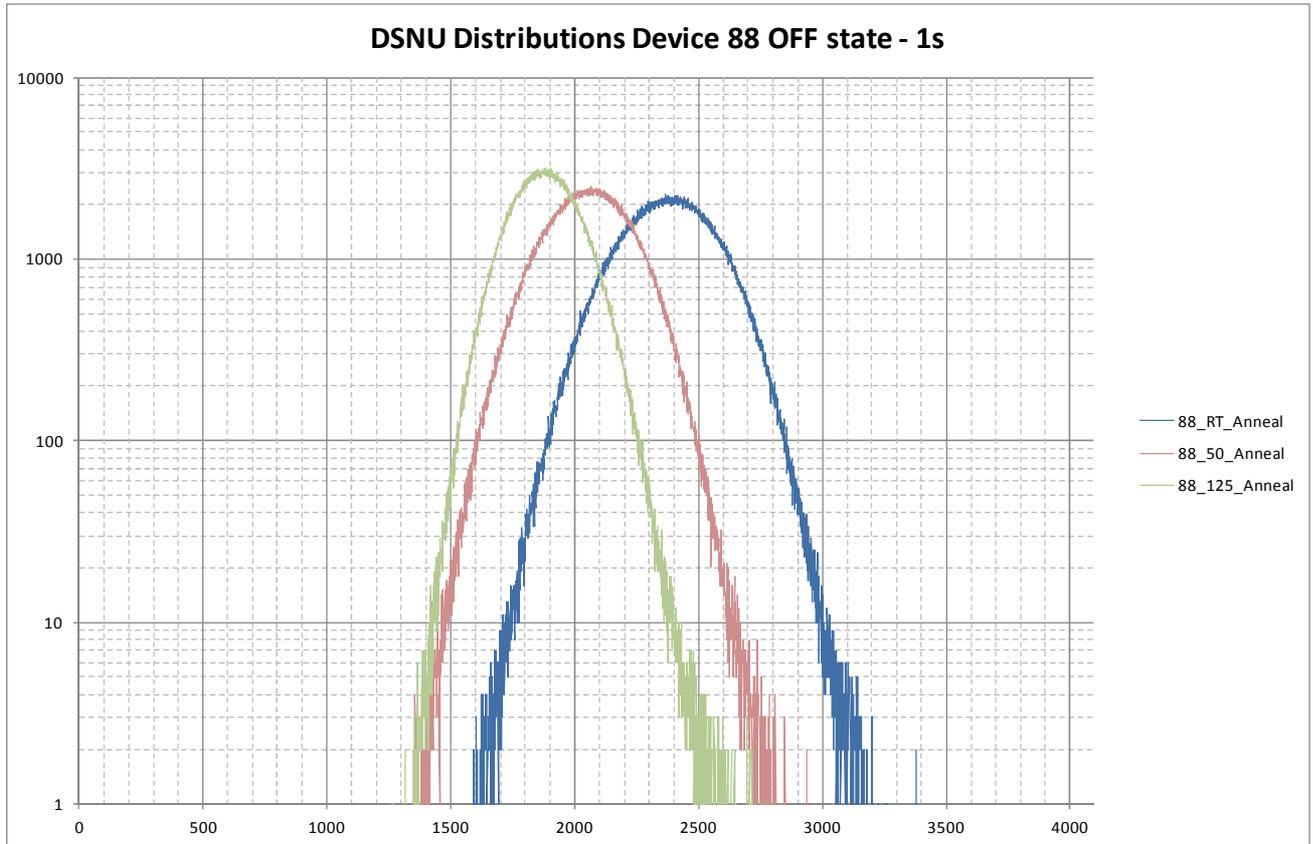


Figure 8-3: DSNU distributions for device 88 after annealing



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **18/44**

The graph below is showing the DSNU distributions for device ID 566 which was in the ON state during radiation and annealing. Please note that the below curves have an integration time of 3 seconds.

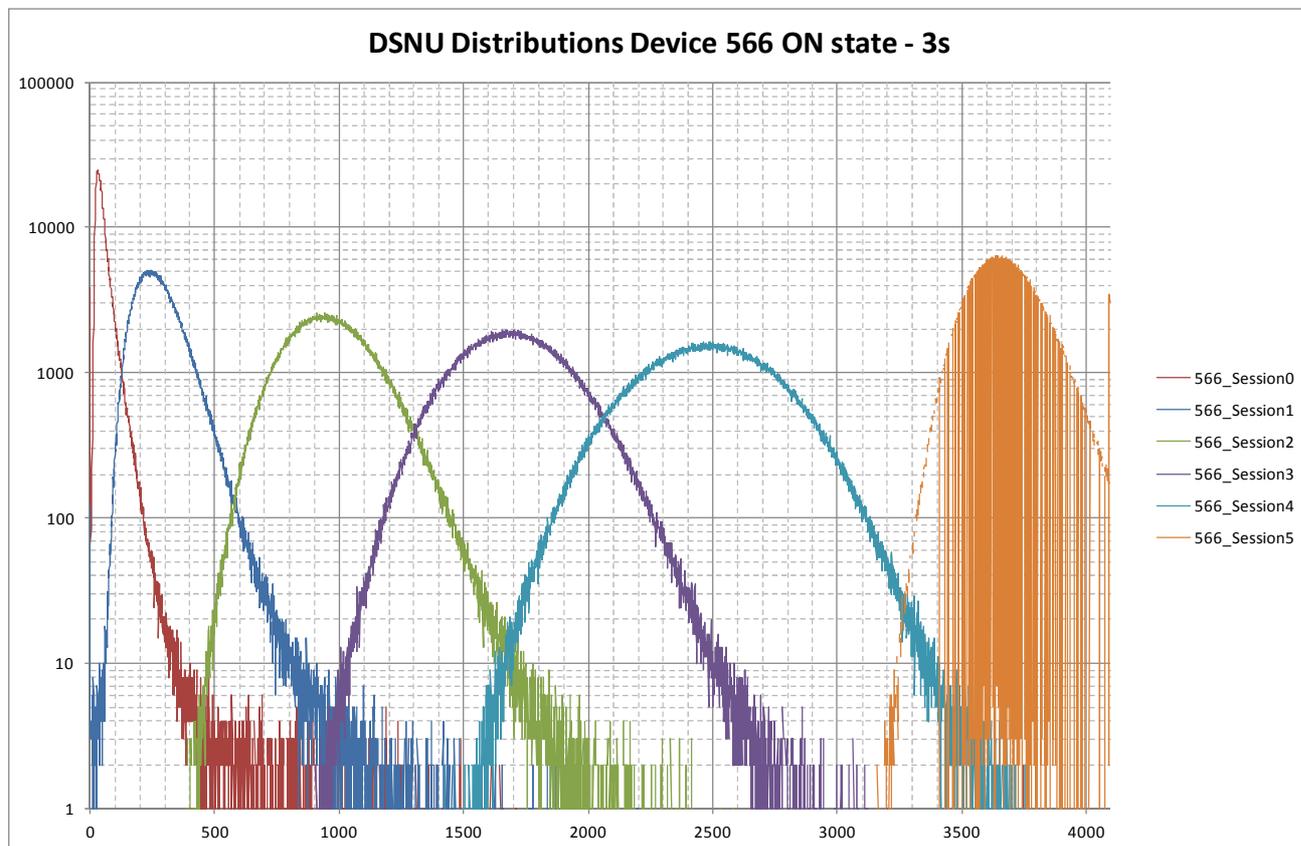


Figure 8-4: DSNU distributions for device 566

Please note that the session 5 distribution has some missing ADC codes due to a testing issue.

The next graph is also showing the DSNU distributions for device 566 but this time after room temperature, 50C and 125C annealing. For these distributions an integration time of 1 second was applied.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **19/44**

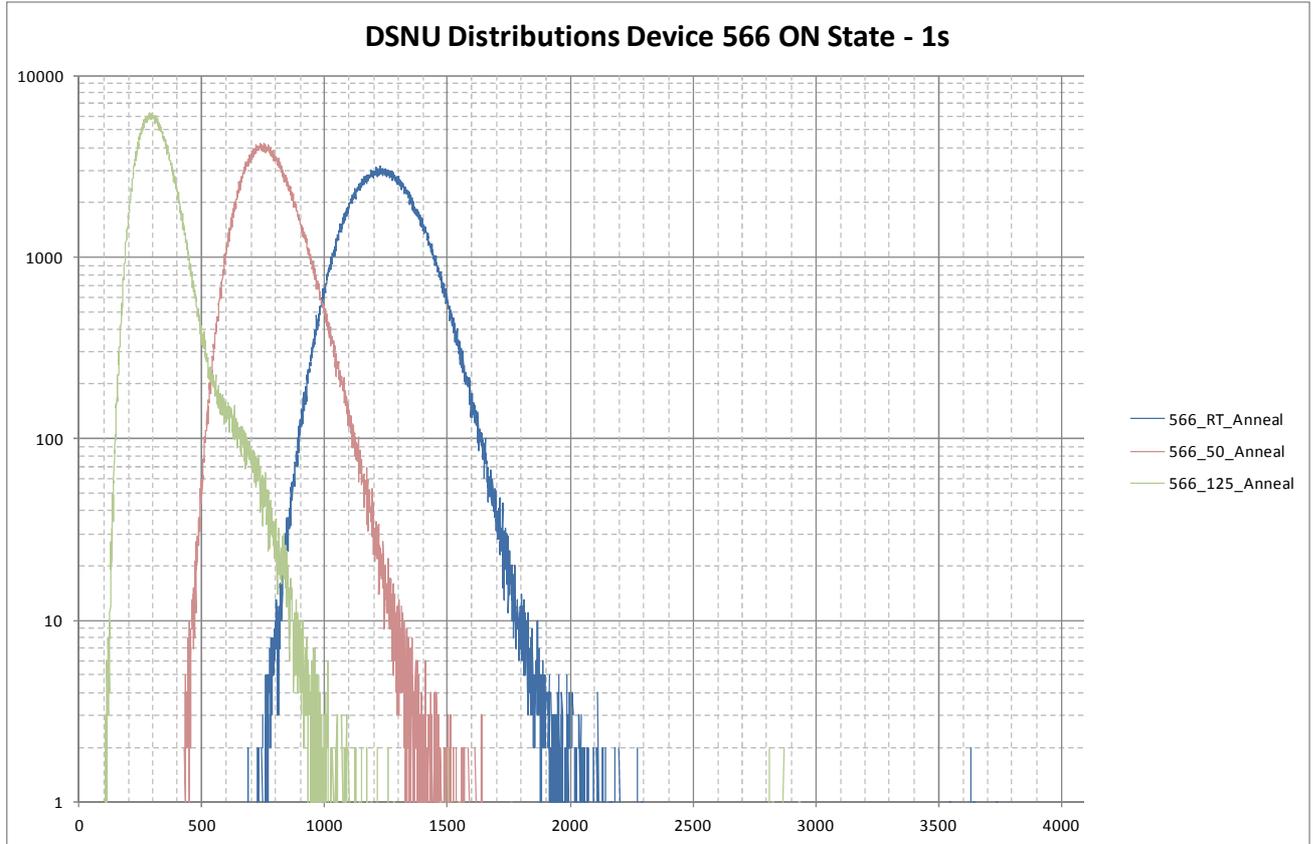


Figure 8-5: DSNU distributions for device 566 after annealing



8.2.2. Temporal Noise in DR Mode – hard reset

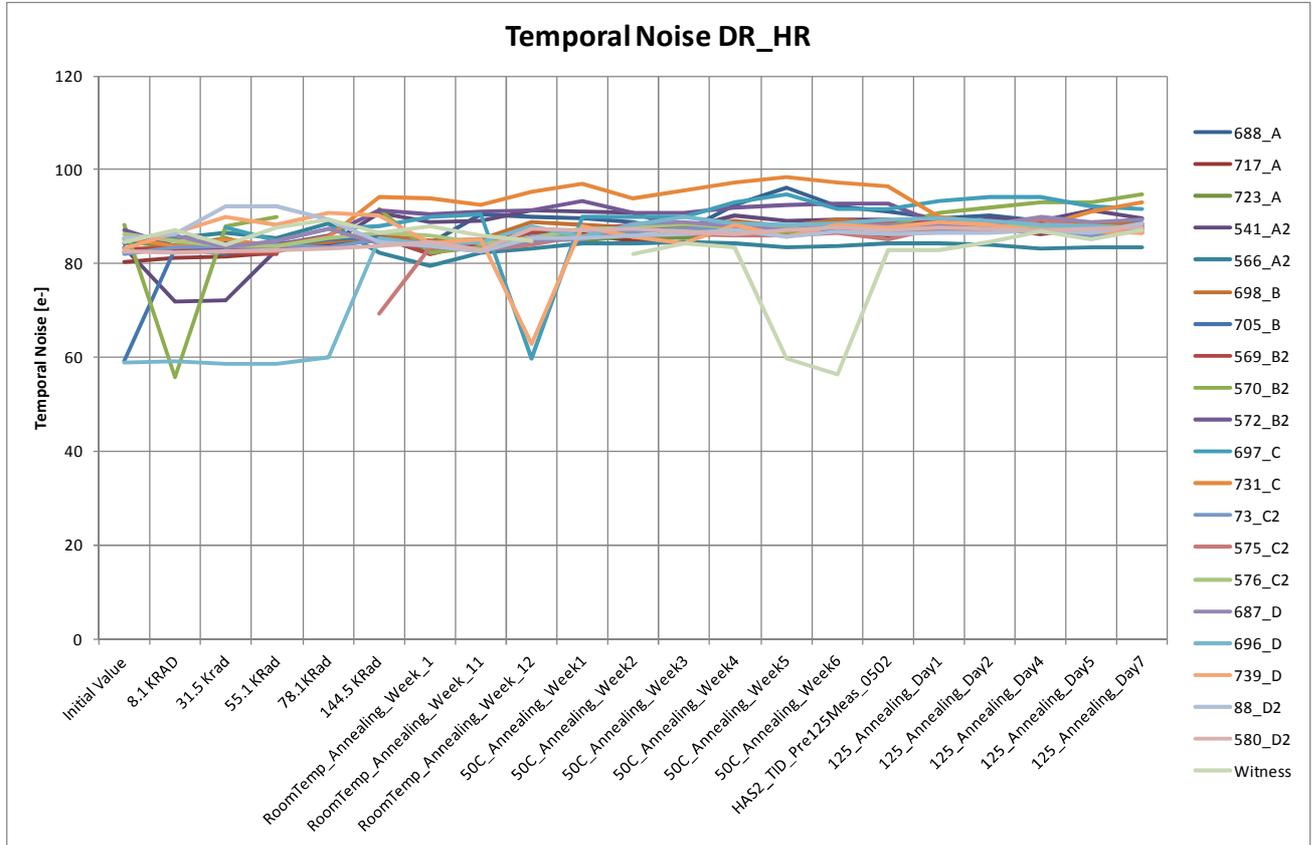


Figure 8-6: Temporal Noise in DR mode – hard reset vs radiation and annealing

The following observations are made:

- Some test points are not reliable due to tester instability during the radiation test.
- Taking an average over the different samples, there's no difference visible between radiation, room temperature annealing and high temperature annealing.
- There is no difference between the different biasing schemes.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **21/44**

8.2.3. Temporal Noise in DR Mode – hard to soft reset

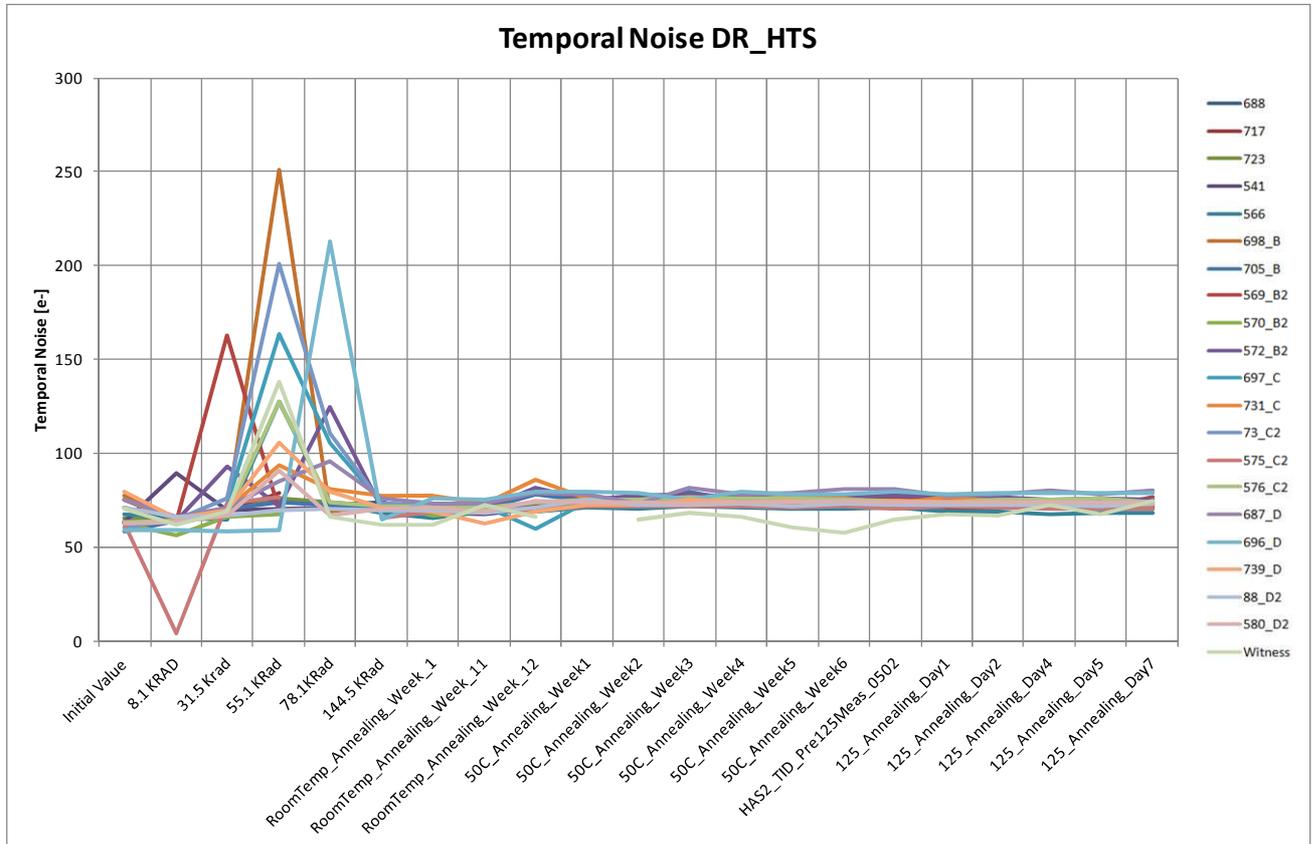


Figure 8-7: Temporal Noise in DR mode – hard to soft reset vs radiation and annealing

The following observations are made:

- Some test points are not reliable due to tester instability during the radiation test.
- Some of the measurement points obtained during irradiation are showing high values. The same effect was observed during the evaluation phase in 2007.
- During room temperature annealing and high temperature annealing there is no change in temporal noise.
- The temporal noise is the same amongst the different biasing schemes.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **22/44**

8.2.4. Temporal Noise in NDR Mode – hard reset

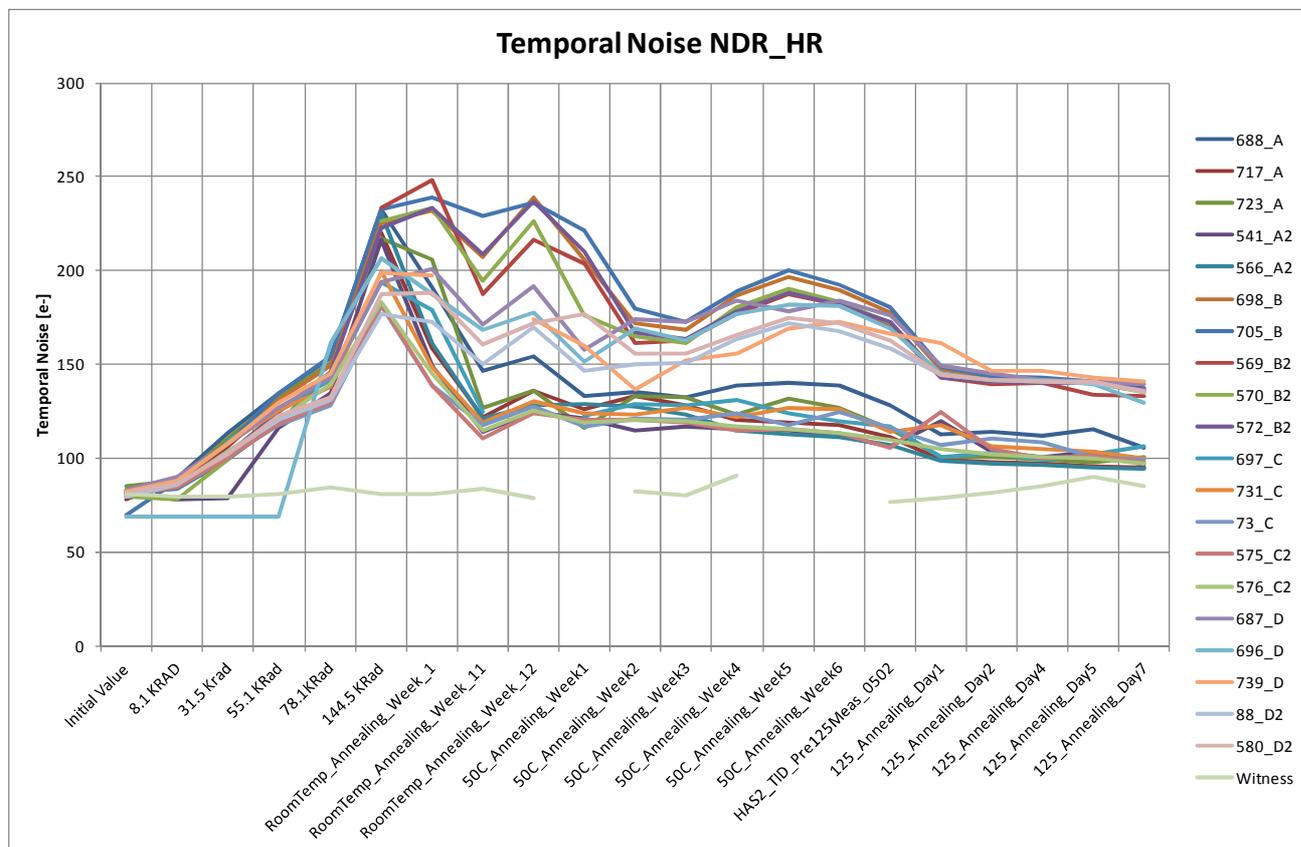


Figure 8-8: Temporal Noise in NDR mode – hard reset vs radiation and annealing

The following observations are made:

- Some test points are not reliable due to tester instability during the radiation test.
- Temporal noise is increasing with radiation. This is probably due to the 200ms minimal integration time on the tester. With increasing radiation a dark current component is added to the temporal noise. There is no difference in biasing scheme.
- Temporal noise is decreasing during room temperature annealing, though the parts which were in the 'ON' state are decreasing much faster and more homogenous than the ones which are annealed in the 'OFF' state. The same effect has been seen for the dark current.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **23/44**

8.2.5. Temporal Noise in NDR Mode – hard to soft reset

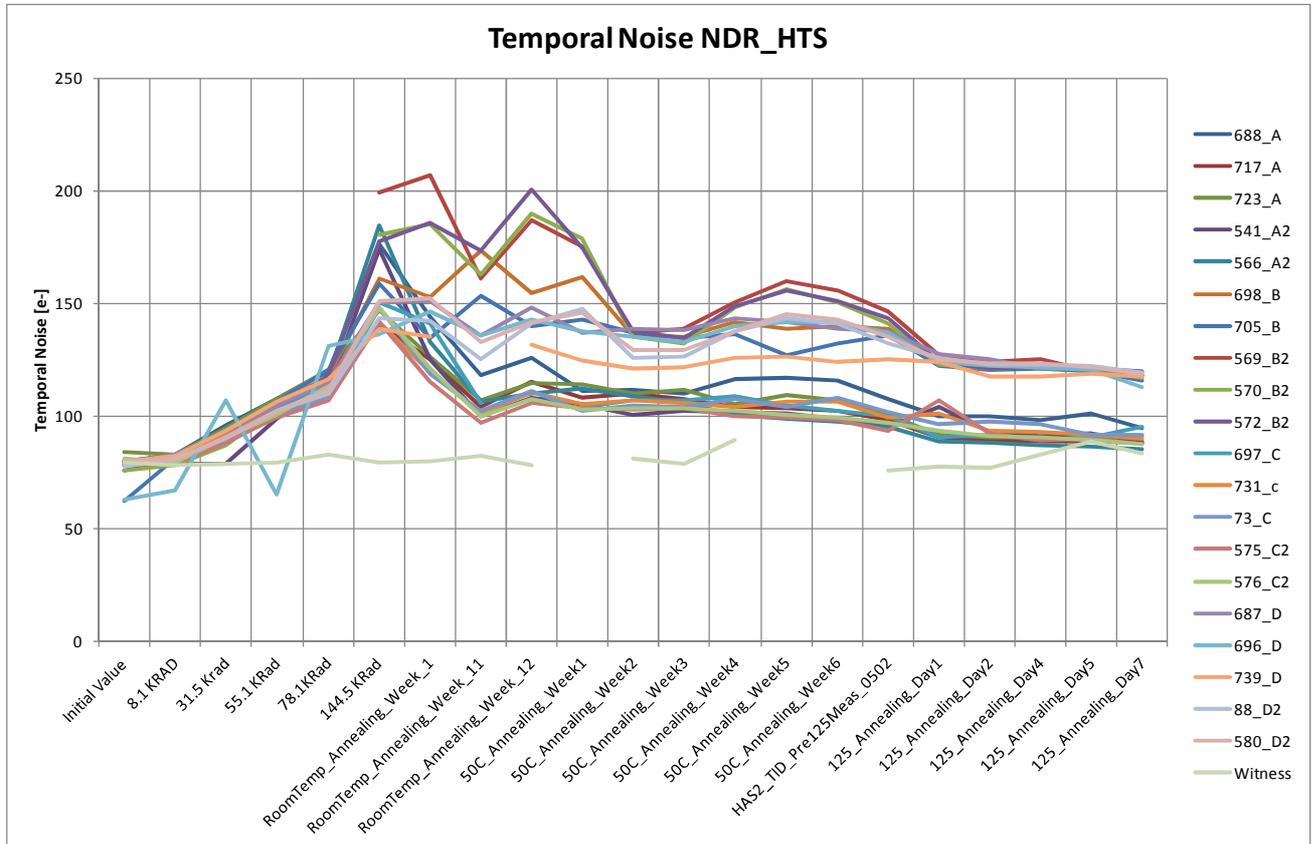


Figure 8-9: Temporal Noise in NDR mode – hard to soft reset vs radiation and annealing

The following observations are made:

- Some test points are not reliable due to tester instability during the radiation test.
- Temporal noise is increasing with radiation. This is probably due to the 200ms minimal integration time on the tester. With increasing radiation a dark current component is added to the temporal noise. There is no difference in biasing scheme.
- Temporal noise is decreasing during room temperature annealing, though the parts which were in the 'ON' state are decreasing much faster and more homogenous than the ones which are annealed in the 'OFF' state. The same effect has been seen for the dark current.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **24/44**

8.2.6. Global Fixed Pattern Noise – hard reset

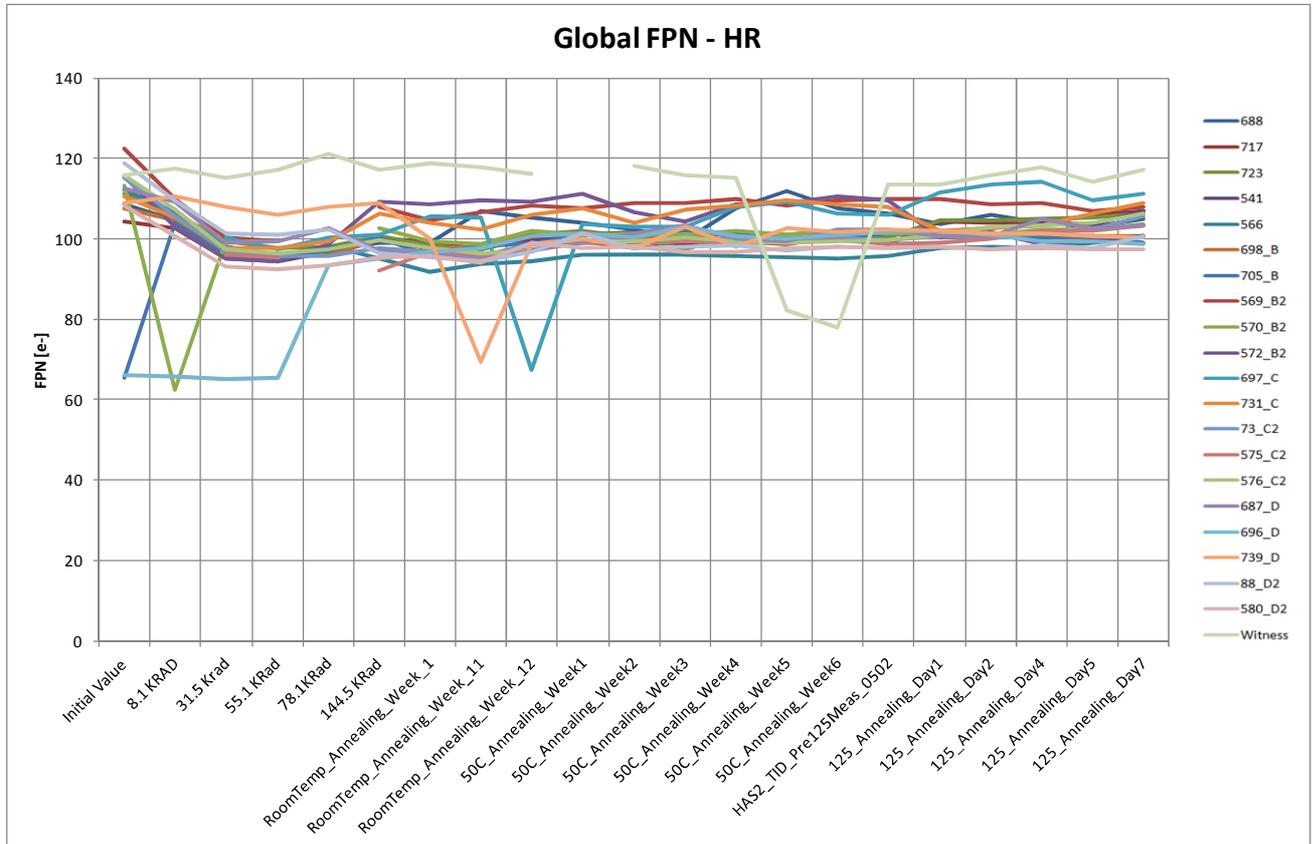


Figure 8-10: Global FPN – hard reset vs radiation and annealing

The following observations are made:

- Some test points are not reliable due to tester instability.
- Taking an average over the different samples, there's no difference visible between radiation, room temperature annealing and high temperature annealing.
- There is no clear difference between the different biasing schemes.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **25/44**

8.2.7. Global Fixed Pattern Noise – hard to soft reset

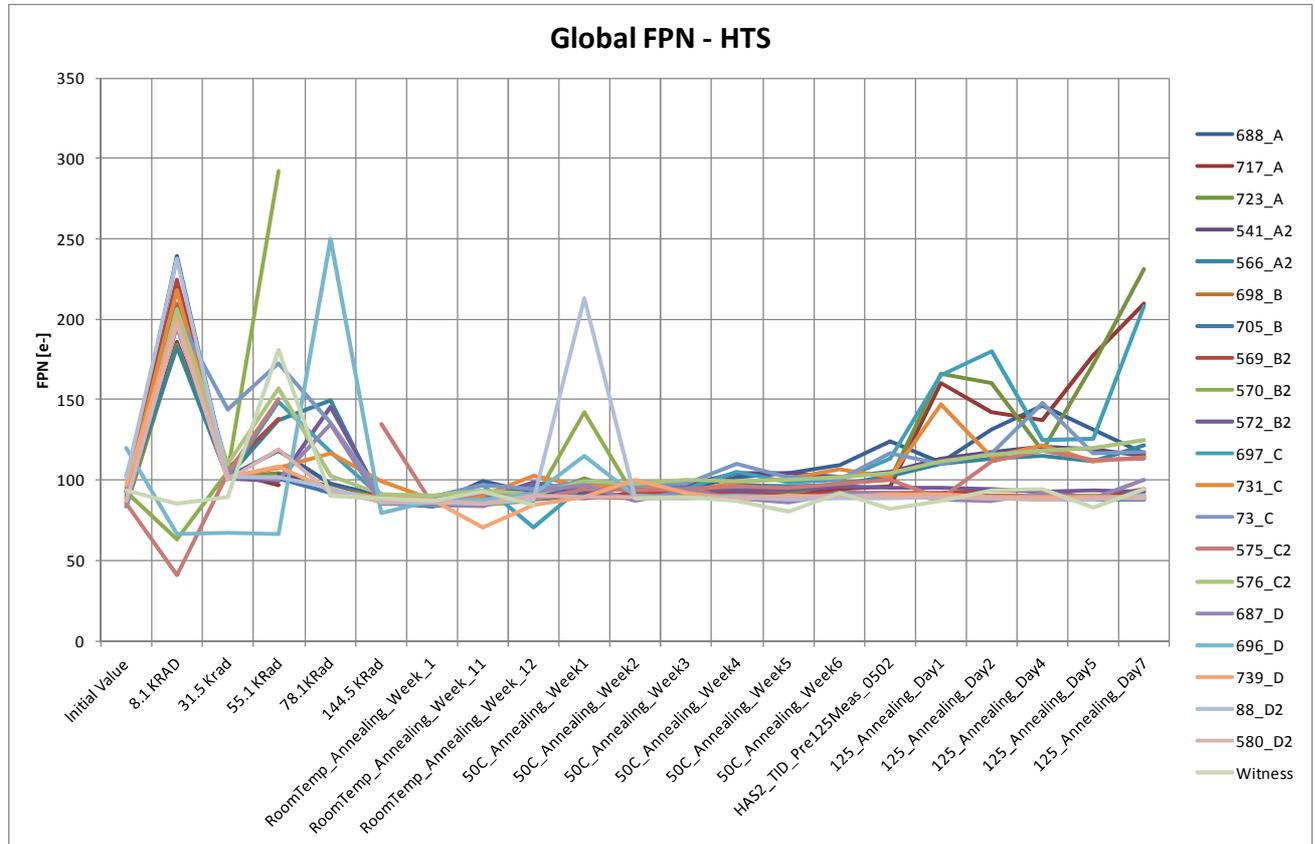


Figure 8-11 Global FPN – hard to soft reset vs radiation and annealing

The following observations are made:

- Some test points are not reliable due to tester instability, especially during radiation.
- The FPN, measured during high temperature annealing for the parts in the 'ON' condition, increases. This is the opposite effect of what has been observed with the dark current. Re-measurement of the parts 7 months later showed initial values again.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: B

Date : 23/11/2012 Séq. : 1

Statut : Final

Classification: NC Page : 26/44

8.2.8. Local Fixed Pattern Noise – hard reset

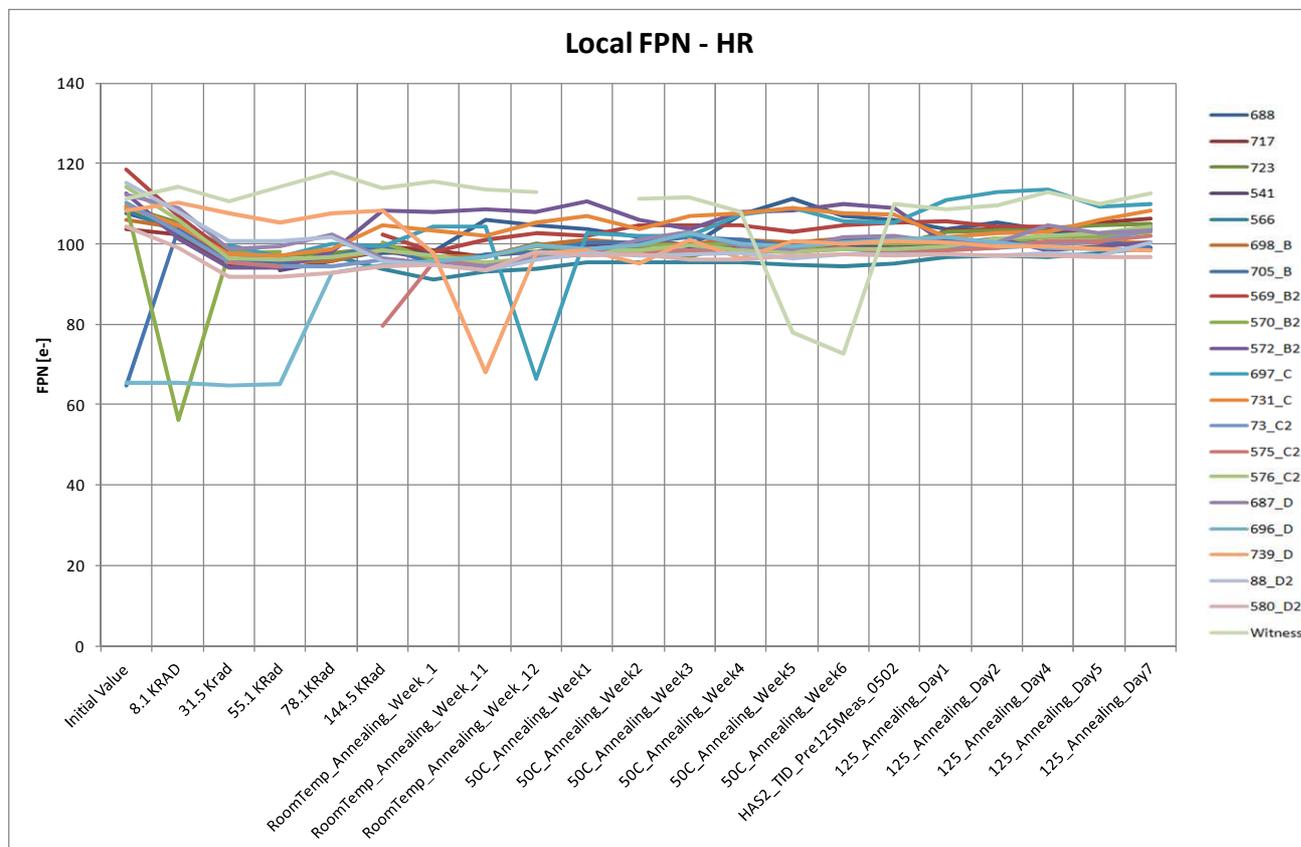


Figure 8-12 Local FPN – hard reset vs radiation and annealing

- Some test points are not reliable due to tester instability.
- Taking an average over the different samples, there's no difference visible between radiation, room temperature annealing and high temperature annealing.
- There is no clear difference between the different biasing schemes.
- FPN is decreasing with increasing radiation. The same observation was made during the evaluation campaign in 2007.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **27/44**

8.2.9. Local Fixed Pattern Noise – hard to soft reset

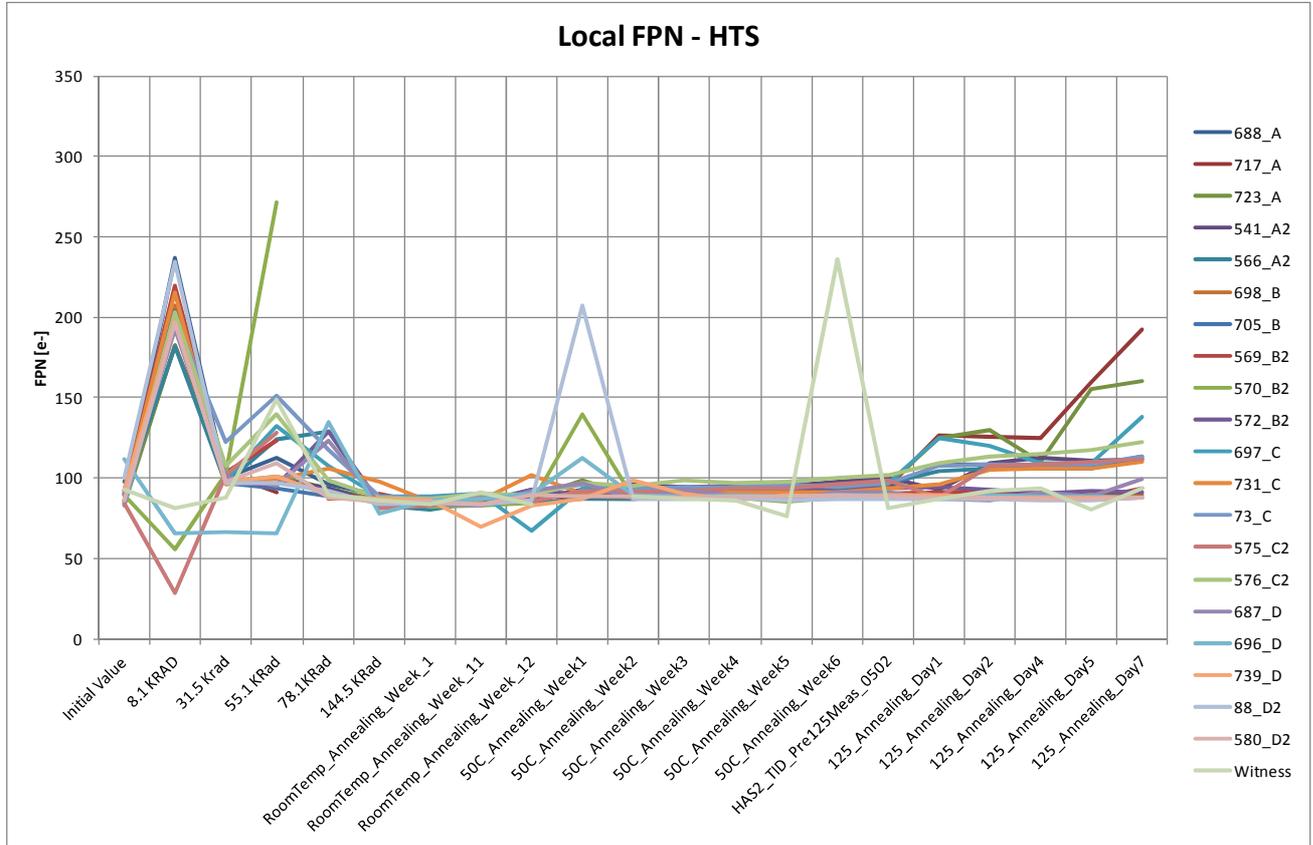


Figure 8-13: Local FPN – hard to soft reset vs radiation and annealing

- Some test points are not reliable due to tester instability, especially during radiation.
- The FPN, measured during high temperature annealing for the parts in the 'ON' condition, increases. This is the opposite effect of what has been observed with the dark current. Re-measurement of the parts 7 months later showed normal values again.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **28/44**

8.2.10. Global Photo Response Non Uniformity

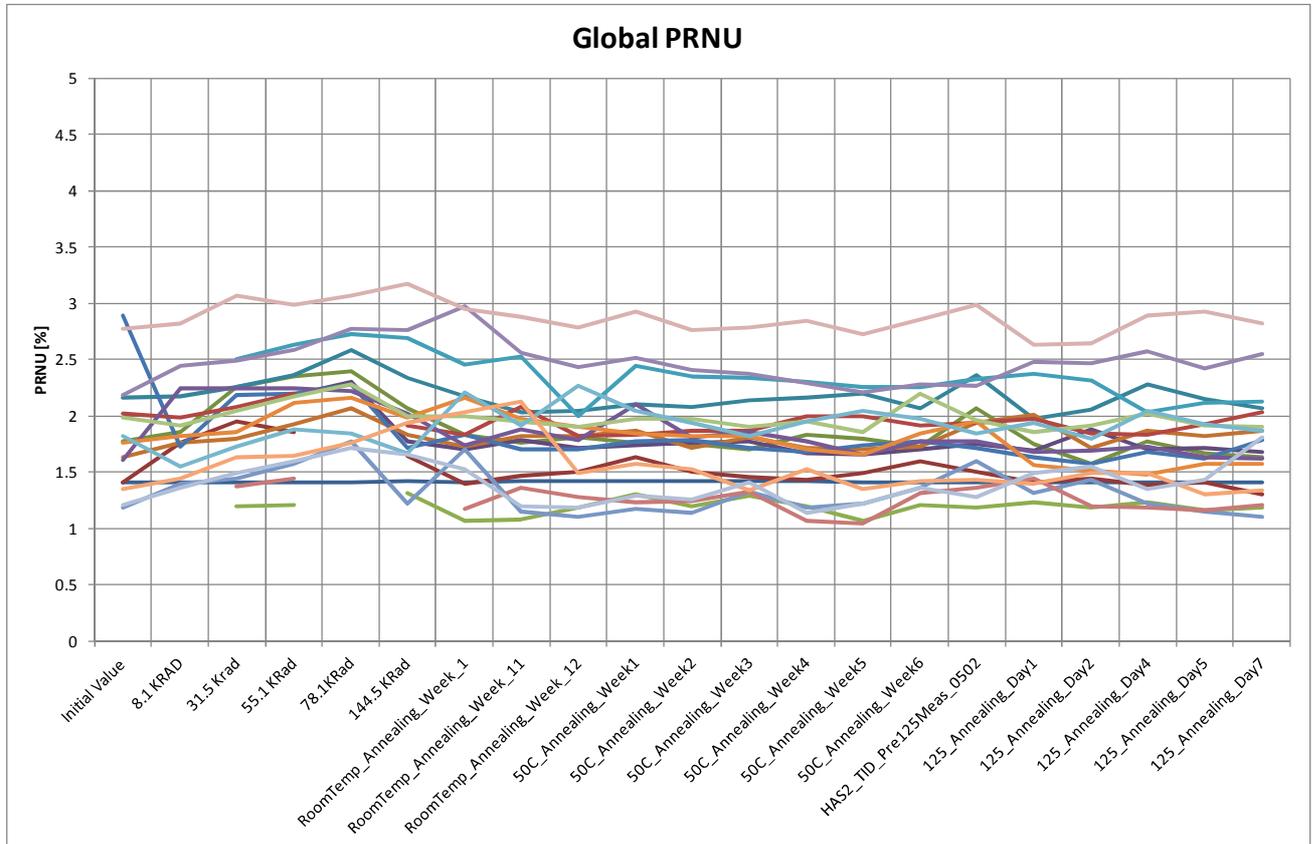


Figure 8-14: Global PRNU vs radiation and annealing

- There's no drift visible during radiation or during room temperature and high temperature annealing.
- The fluctuations visible are probably due to some influence of particle and handling contamination as the tests were performed in non clean room environment.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **29/44**

8.2.11. Local Photo Response Non Uniformity

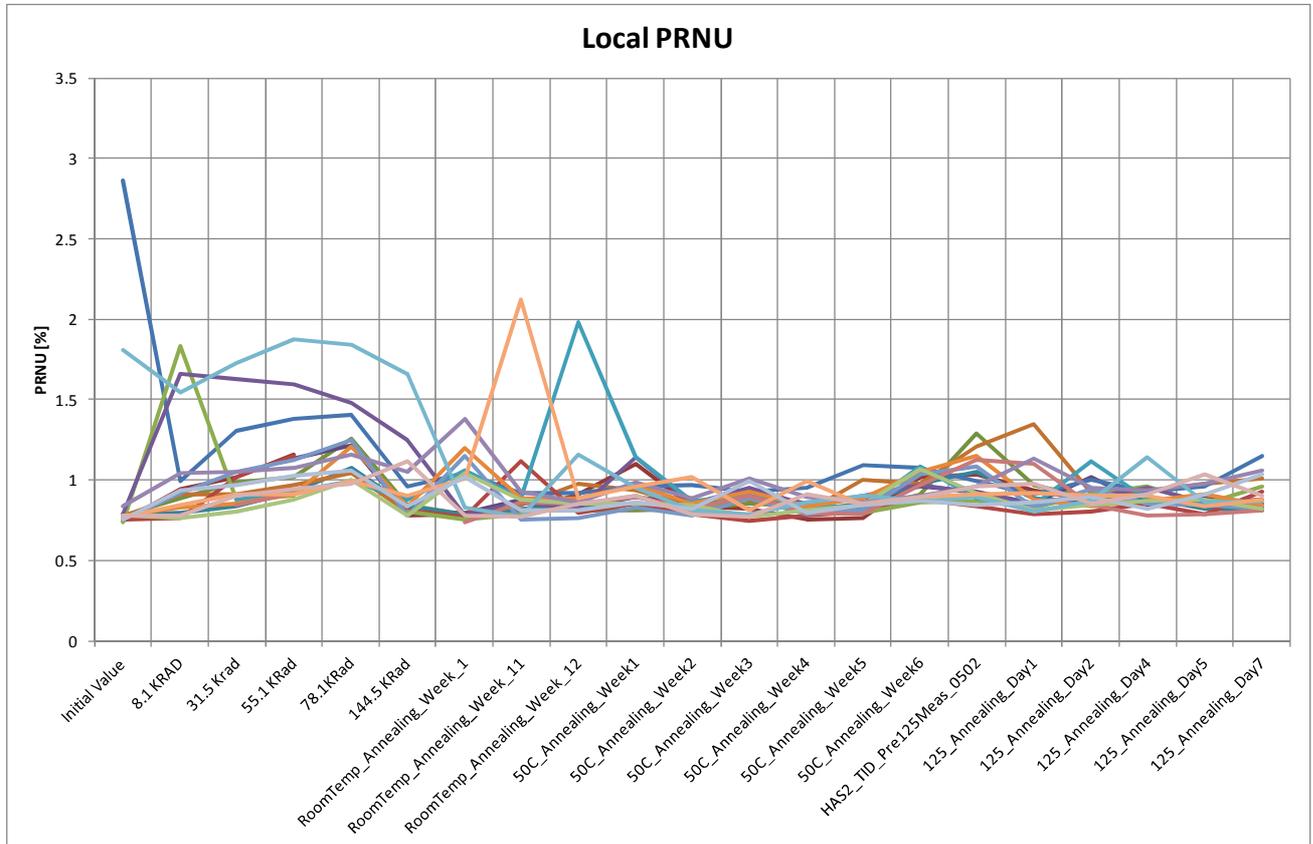


Figure 8-15: Local PRNU vs radiation and annealing

- There's some fluctuation visible during radiation. This is probably due to the instability of the tester.
- There's no drift visible during room temperature and high temperature annealing.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **30/44**

8.2.12. Operating Current

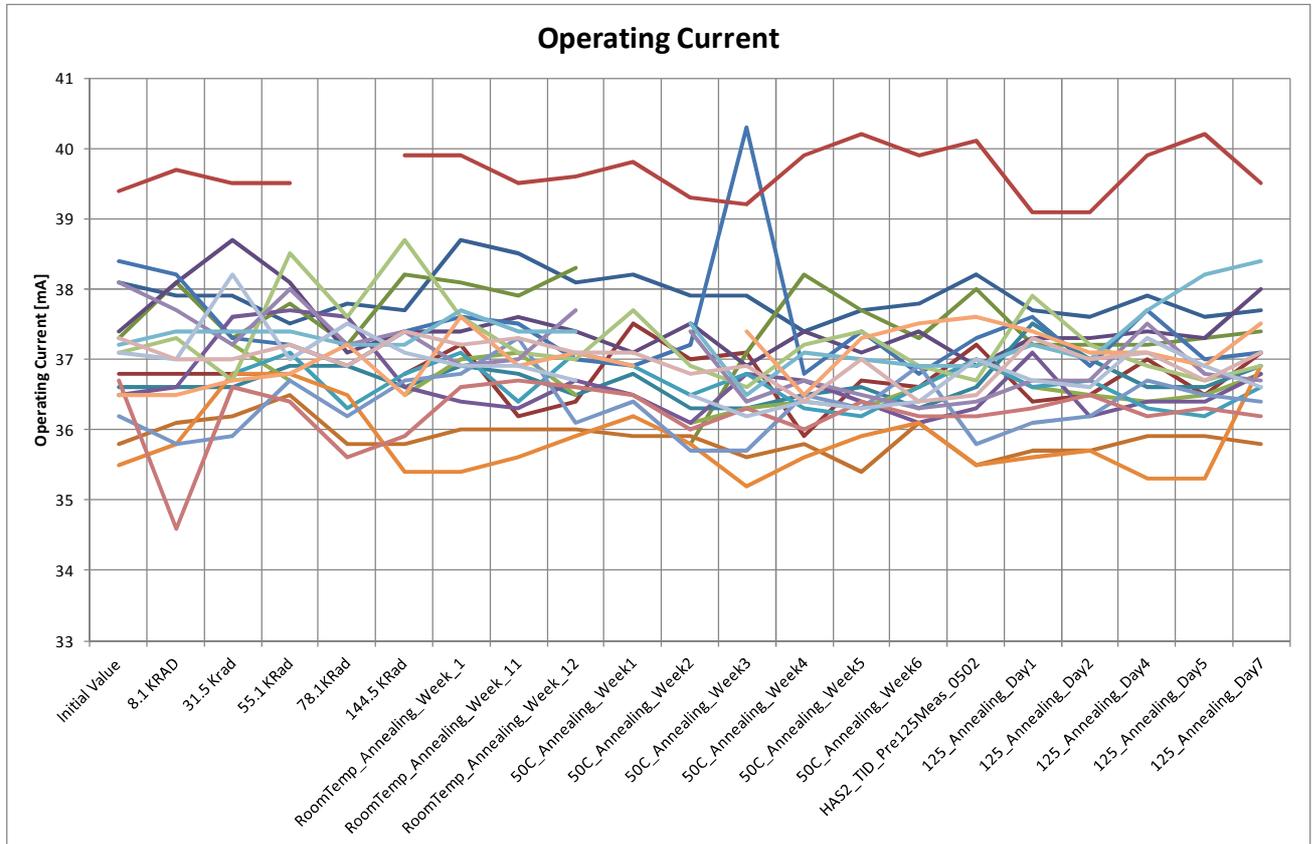


Figure 8-16: Operating Current vs radiation and annealing

- The operation current does not change over radiation, room temperature annealing and high temperature annealing. Also the different biasing schemes have no influence.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **31/44**

8.2.13. Standby Current

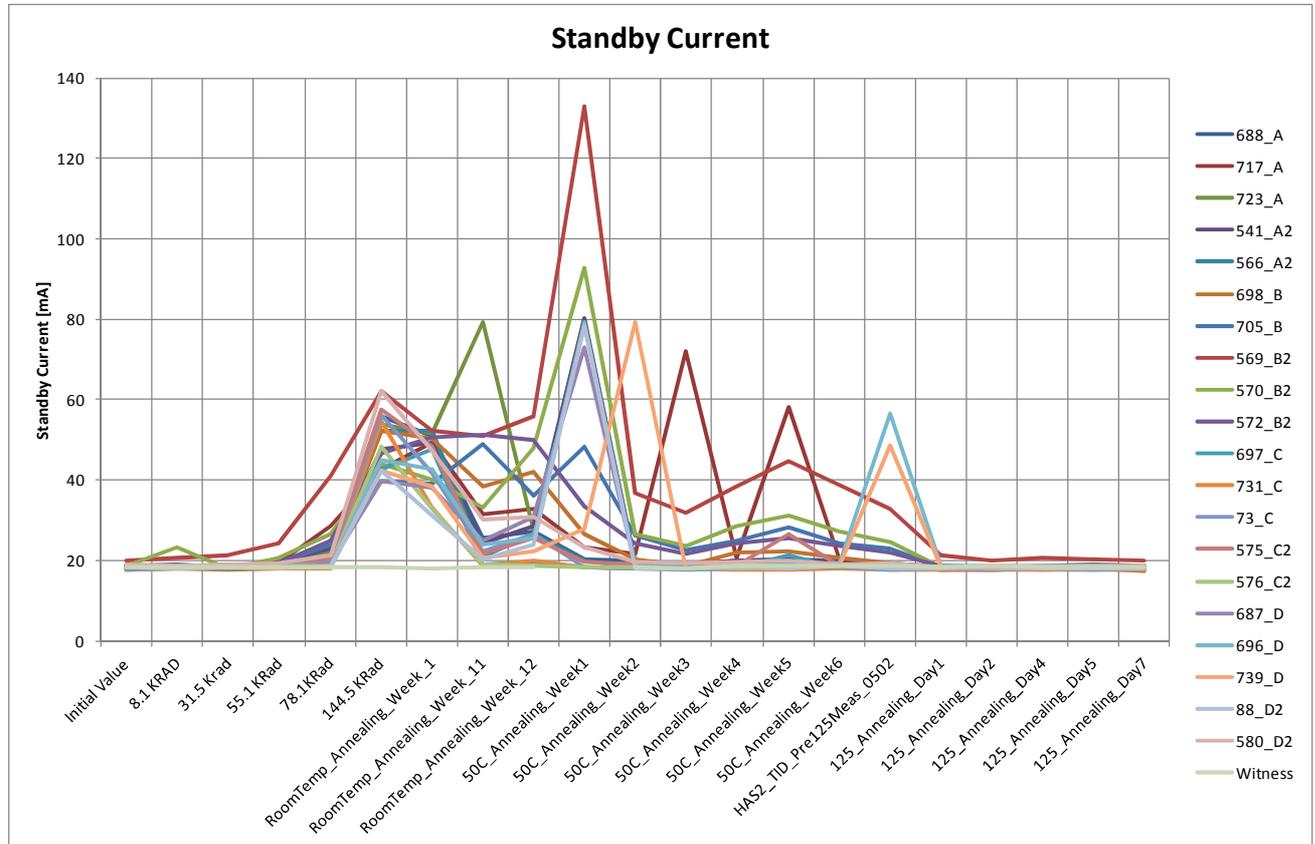


Figure 8-17: Standby Current vs radiation and annealing

- Standby current is getting unstable after the 78.1KRad measurement point. The same observation was made during the evaluation phase in 2007, though the effect was only seen at elevated temperature (85 degC).
- Standby current keeps unstable during room temperature annealing and 50 degrees annealing. The majority of the devices showing unstable behavior are annealed in the 'OFF' state.
- Standby current gets back to normal during high temperature annealing.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **32/44**

8.2.14.DSNU

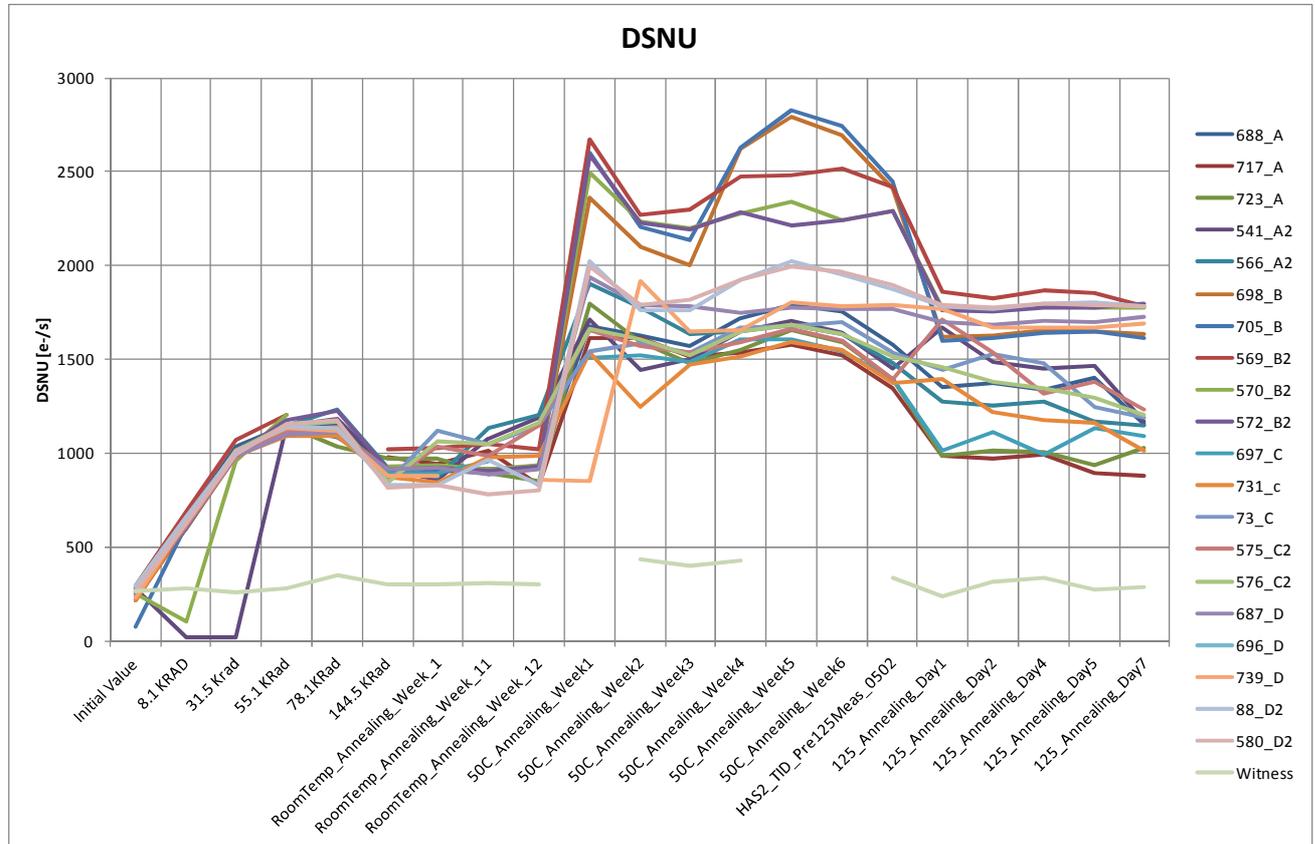


Figure 8-18: DSNU vs radiation and annealing

- DSNU increases the same for all the samples, independent from the wafer lot, independent from the biasing conditions
- DSNU does not change significantly during room temperature annealing. No influence from the bias condition.
- DSNU increases significantly after 1 day of 50 degrees C annealing for the OFF biasing condition (B, B2, D and D2).
- DSNU drops during 125degC annealing for both the biased and unbiased condition.
- Some measurement points are unreliable due to tester instability.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **33/44**

8.2.15. INL

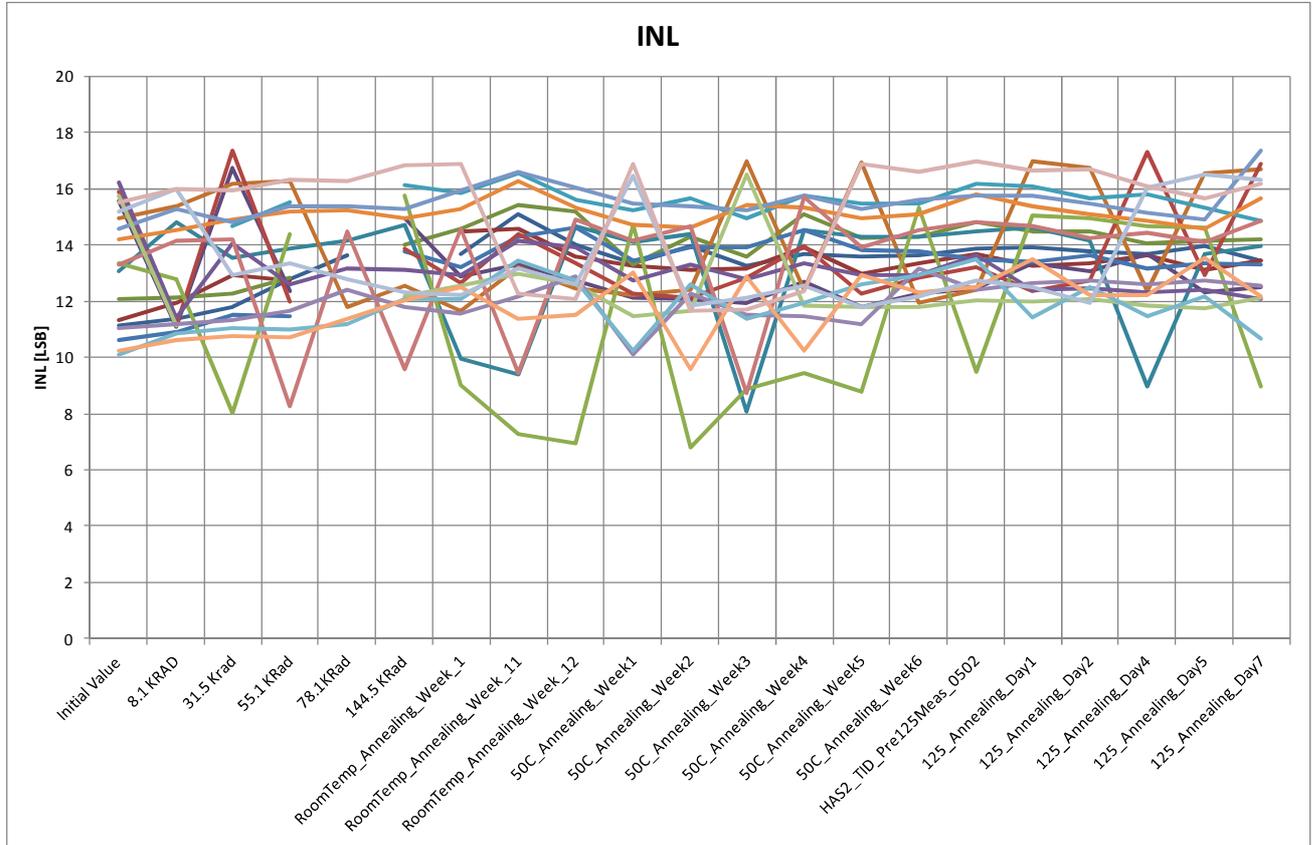


Figure 8-19: INL vs radiation and annealing

- INL is a very unstable measurement due to the behavior of the HAS2 ADC.
- There's no increase or decrease visible during radiation or annealing.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **34/44**

8.2.16.DNL

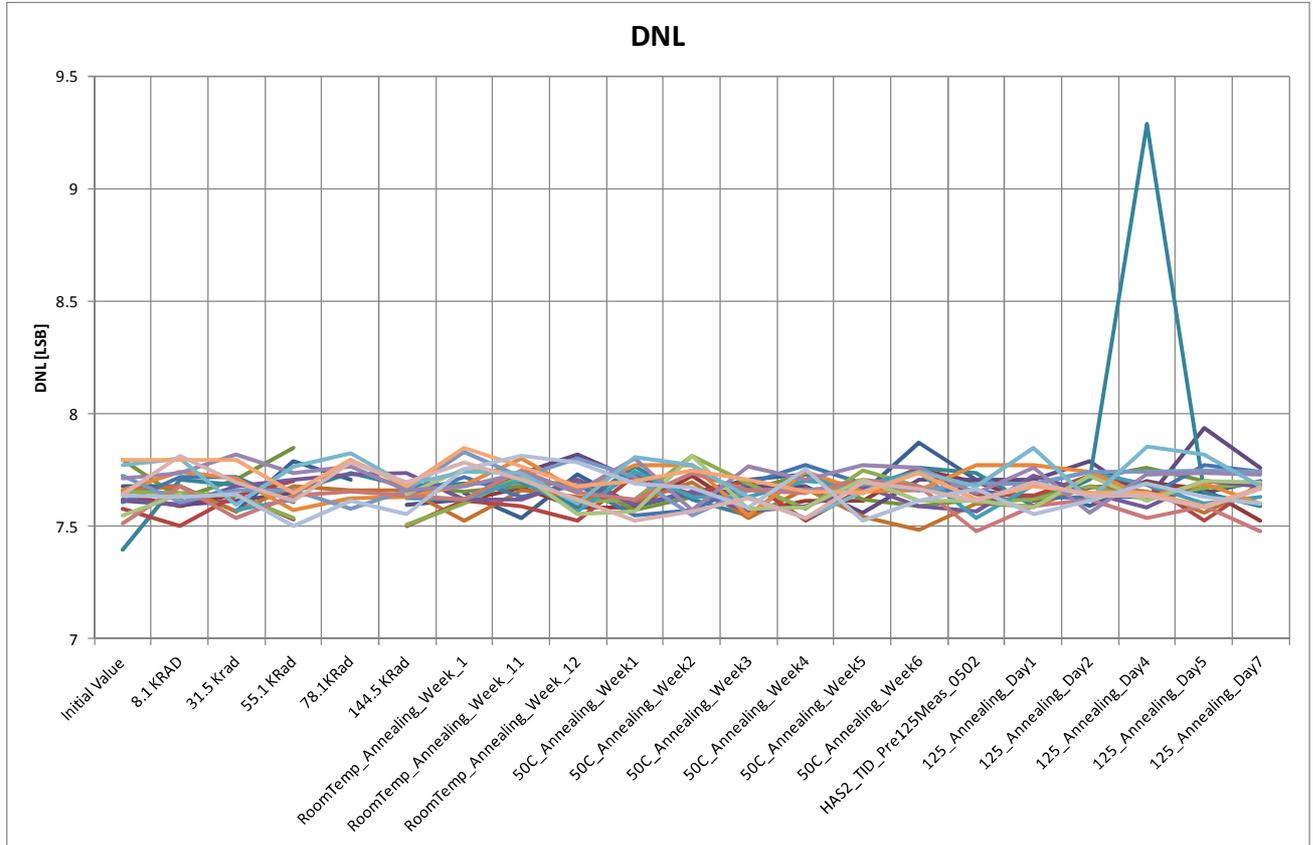


Figure 8-20: DNL vs radiation and annealing

- There's no increase or decrease visible during radiation or annealing.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **35/44**

8.2.17. Electro Optical Measurements

Electro optical measurements were performed on 5 devices. 2 Devices were selected from the new wafer lot; another 2 devices were selected from the same lot that was used for the evaluation campaign in 2007. Finally one device was used as a reference device.

Device ID	Silicon Wafer Lot	Assembly Lot
689	P29506.1	11-002
688	P29506.1	11-002
073	P20291.1	ESA-QUAL-LOT
088	P20291.1	ESA-QUAL-LOT
164	Reference Device	ESA-QUAL-LOT

Observations:

- After radiation we were unable to retrieve data from device nr. 689. Also during the radiation campaign this device was not working properly. Analysis has shown that there was a broken lead on the device. This probably happened when inserting and taking out the device from its test socket.
- Device nr.88 was drawing a very high leakage current in the test pixel array and as such was not usable anymore for measuring spectral and optical response.
- Only device 688 and 73 could be measured after radiation.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **36/44**

8.2.17.1. Spectral Response

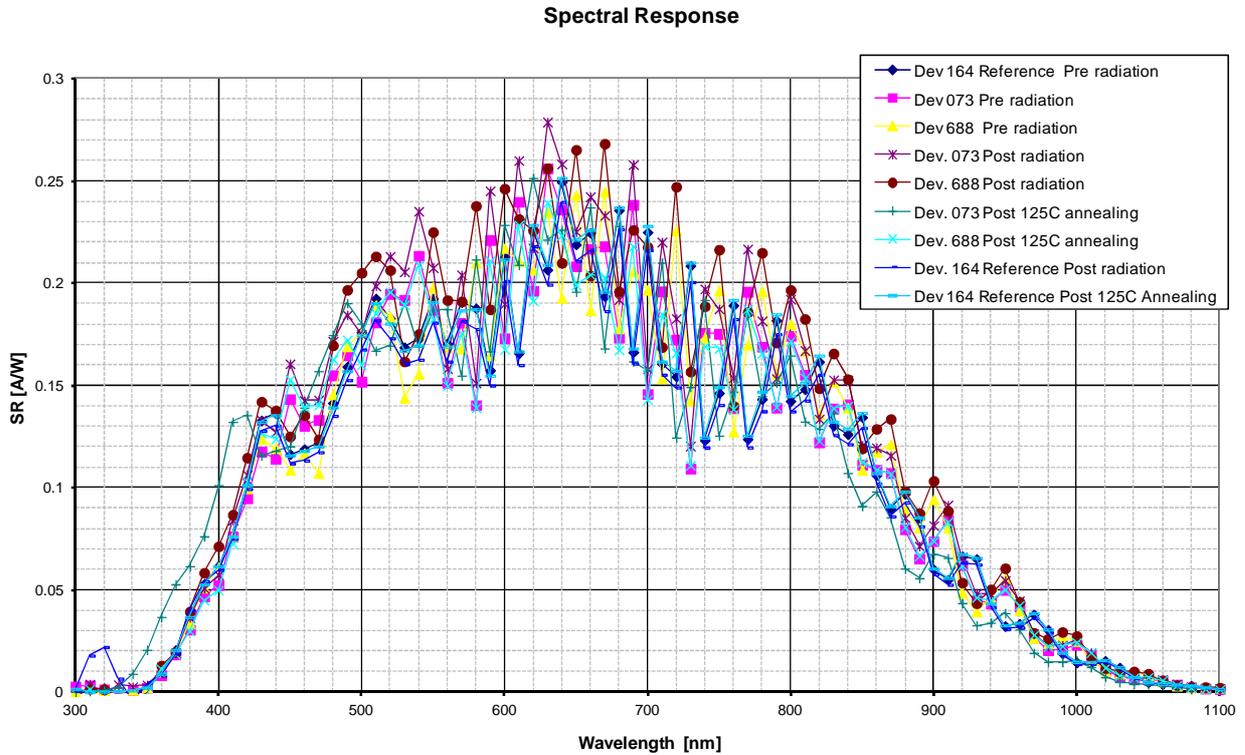


Figure 8-21: Spectral Response before and after radiation and annealing

No degradation is visible after 144KRad TID. The minor deviations that are visible are due to setup-to-setup variations.

Response Data			
Device	Average Value 400-900 nm [A/W] Pre Radiation	Average Value 400-900 nm [A/W] Post Radiation	Average Value 400-900 nm [A/W] Post 125C Annealing
073	0.158	0.173	0.155
688	0.159	0.177	0.162
164	0.157	0.150	0.157



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **37/44**

8.2.17.2. Optical Response

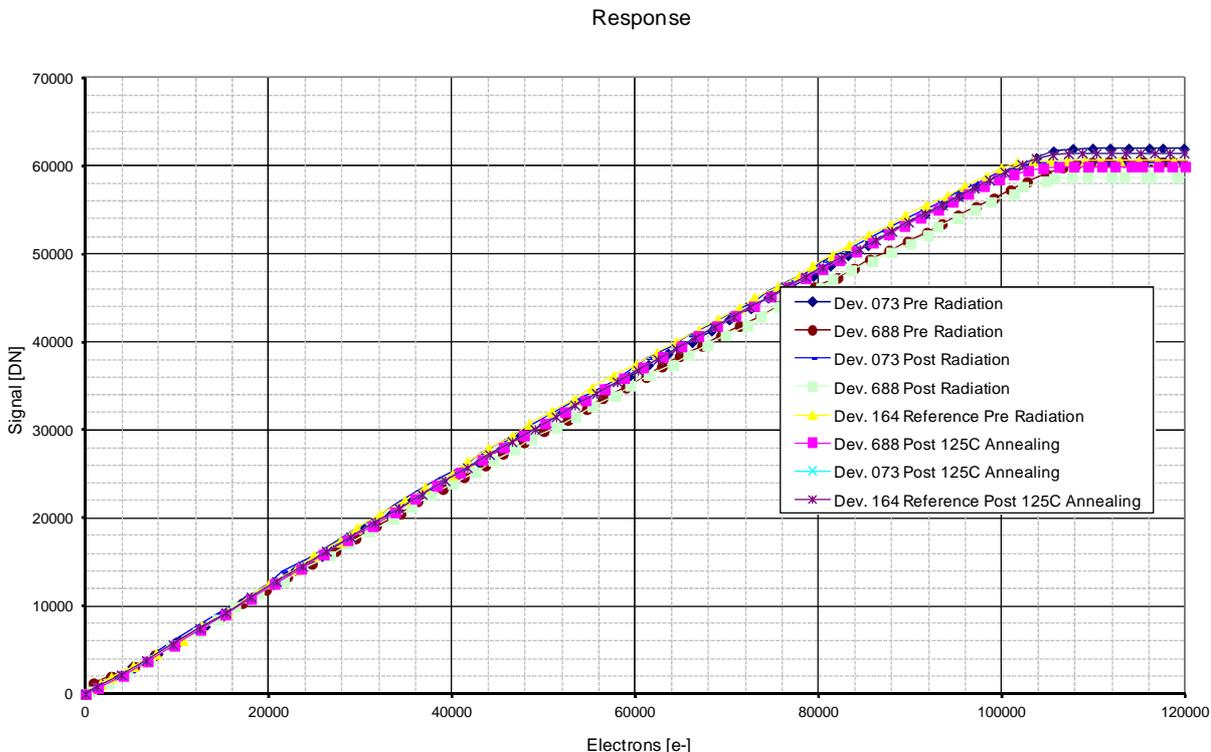


Figure 8-22: Optical Response before and after radiation and annealing

No degradation is visible after 144KRad TID. The minor deviations that are visible are due to setup-to-setup variations.

Conversion Factor (CF) Data			
Device	CF [$\mu\text{V}/\text{e}^-$] Pre Radiation	CF [$\mu\text{V}/\text{e}^-$] Post Radiation	CF [$\mu\text{V}/\text{e}^-$] Post 125C Annealing
073	13.6	14.1	13.7
688	13.2	13.3	13.8
164	14.1	13.8	13.7



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **38/44**

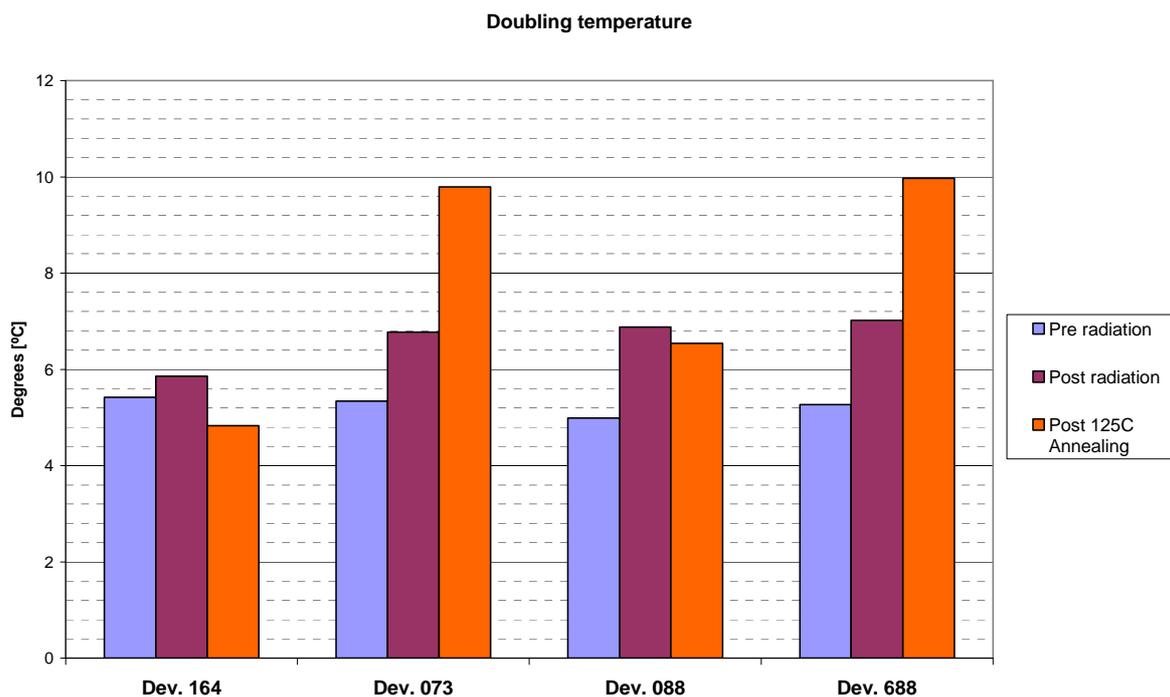
8.2.17.3.MTF

MTF Data			
Device	MTF [%] Pre Radiation	MTF [%] Post Radiation	MTF [%] Post 125C Annealing
073	43.9	39.3	39.8
088	37.7	40.7	38.2
688	41.7	37.9	36.8
164	42.9	40.24	42.8

The deviations are due to setup-to-setup variation.

8.2.17.4.Dark Signal Doubling Temperature

The dark signal doubling temperature was measured by placing the devices under a thermo stream. Temperatures used were 10°C, 25°C and 40°C.



Doubling Temperature			
Device	DT [°C] Pre Radiation	DT [°C] Post Radiation	DT [°C] Post 125C Annealing
073	5.34	6.78	9.79
088	4.99	6.88	6.54
688	5.27	6.88	9.97
164	5.42	5.86	4.93



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **39/44**

Observations :

- Device. 088 behaves different compared to device 073 and 688. This might be related to the biasing state of the device during annealing. Device 088 is annealed in the 'OFF' state whereas device 73 and 688 are annealed in the 'ON' state.
- It is remarkable that the doubling temperature of device 688 and 073 is increasing even after high temperature annealing. At the moment of writing this test report no explanation can be given for this behavior.

8.2.17.5. Image Lag

Image Lag

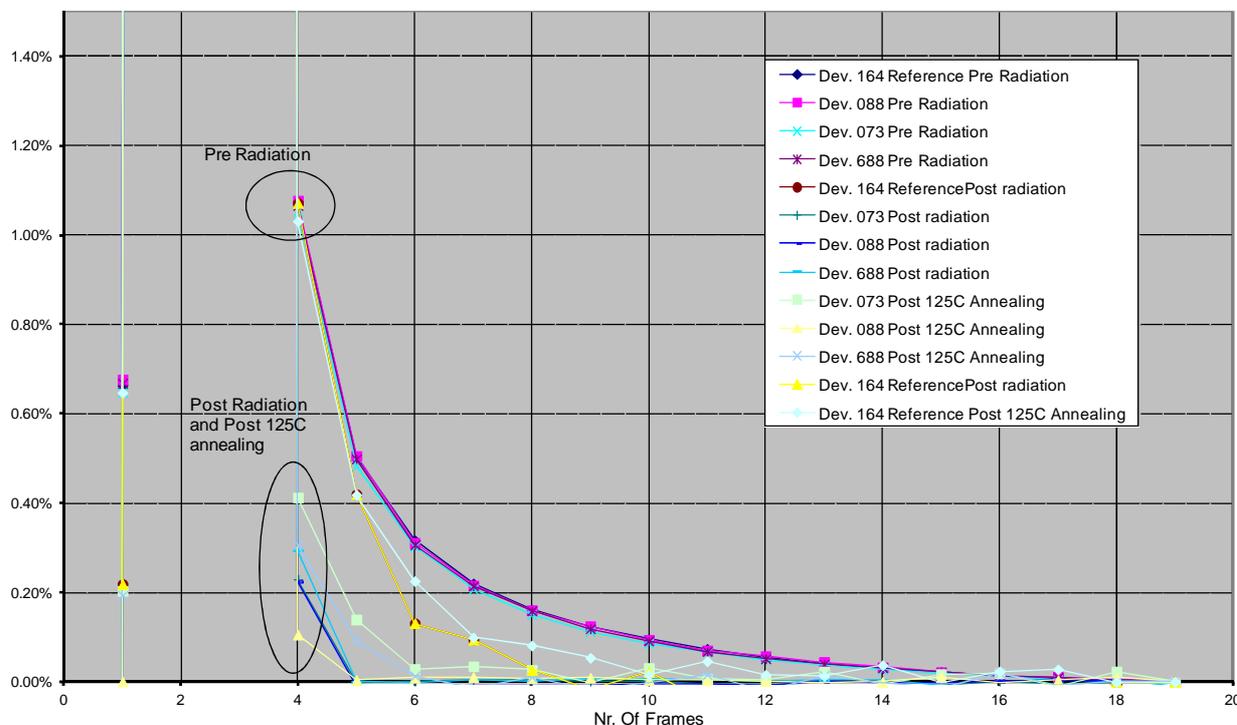


Image Lag Data			
Device	Image Lag [%] Pre Radiation	Image Lag [%] Post Radiation	Image Lag [%] Post 125C Annealing
073	1.05	0.23	0.41
088	1.08	0.22	0.11
688	1.07	0.30	0.31
164	1.07	1.07	1.03

The image lag for the reference device is stable for each measurement, confirming a proper setup. It is unknown why the image lag drops after radiation.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**Classification: NC Page : **40/44**

8.2.18. Calibration Parameters

Odd/even offset matching, NDR black level offset and temperature sensor curve calibration parameters were measured before and after radiation.

Test	ID	Matchable	Value		Black Offset/ Reg	Temp Calib	Voltage
PRE	723	1	85	23.07	26	85	1.156
			84	11.51		-40	1.6844
			86	29.88		25	1.4327
POST	723	1	89	4.51	24	85	1.1503
			88	11.85		-40	1.6931
			90	5.197		25	1.4326
PRE	741	Not Matchable		29	85	1.1423	
					-40	1.6637	
					25	1.4144	
POST	741	Not Matchable		27	85	1.1538	
					-40	1.6682	
					25	1.4186	
PRE	713	Not Matchable		25	85	1.1101	
					-40	1.6613	
					25	1.4007	
POST	713	Not Matchable		23	85	1.1219	
					-40	1.665	
					25	1.4055	
PRE	717	1	85	11.14	28	85	1.1449
			84	18.38		-40	1.6744
			86	0.8134		25	1.4225
POST	717	1	94	17.08	26	85	1.1108
			93	24.36		-40	1.6421
			95	9.302		25	1.3815
PRE	705	Not Matchable		26	85	1.1327	
					-40	1.6703	
					25	1.4155	
POST	705	Not Matchable		24	85	1.1195	
					-40	1.7078	
					25	1.4357	
PRE	679	1	54	11.35	26	85	1.1331
			53	17.28		-40	1.6726
			55	2.815		25	1.4158
POST	679	1	58	13.77	24	85	1.1377
			57	24.03		-40	1.6751
			59	8.682		25	1.4174
PRE	698	1	49	1.434	29	85	1.1626
			48	8.9		-40	1.6849
			50	8.575		25	1.4335
POST	698	1	39	4.927	27	85	1.1388
			38	4.396		-40	1.6856
			40	13.21		25	1.3664



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**Classification: NC Page : **41/44**

Test	ID	Matchable	Value		Black Offset/ Reg	Temp Calib	Voltage
PRE	697	1	88	18.86	34	85	1.1315
			87	28.15		-40	1.6645
			89	9.744		25	1.4107
POST	697	1	93	6.417	31	85	1.1305
			92	15.77		-40	1.6642
			94	0.9434		25	1.4126
PRE	731	1	102	11.08	29	85	1.1315
			101	19.15		-40	1.6673
			103	0.1161		25	1.4111
POST	731	1	114	3.779	26	85	1.1138
			113	7.943		-40	1.6227
			115	8.253		25	1.3674
PRE	739	Not Matchable		33	85	1.1272	
					-40	1.6566	
					25	1.4047	
POST	739	Not Matchable		29	85	1.0927	
					-40	1.6444	
					25	1.3961	
PRE	687	Not Matchable		33	85	1.1181	
					-40	1.6605	
					25	1.4031	
POST	687	Not Matchable		30	85	1.1107	
					-40	1.6437	
					25	1.3844	
PRE	696	1	203	0.07455	35	85	1.1369
			202	10.04		-40	1.6693
			204	6.391		25	1.4164
POST	696	1	227	7.355	33	85	1.1122
			226	0.1672		-40	1.6526
			228	16.89		25	1.3959
PRE	689	Not Matchable		28	85	1.1435	
					-40	1.6678	
					25	1.4345	
POST	689	Not Matchable		26	85	1.1674	
					-40	1.682	
					25	1.4358	
PRE	688	Not Matchable		35	85	1.1324	
					-40	1.6605	
					25	1.4097	
POST	688	Not Matchable		30	85	1.1429	
					-40	1.6639	
					25	1.4129	
PRE	541	1	26	2.807	47	85	1.1544
			25	11.15		-40	1.667
			27	5.185		25	1.4138
POST	541	1	40	15.83	44	85	1.1262
			39	5.005		-40	1.6532



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **42/44**

Test	ID	Matchable	Value		Black Offset/ Reg	Temp Calib	Voltage
			41	24.45		25	1.4031
PRE	566	1	208	4.874	41	85	1.1565
			207	0.3598		-40	1.6575
			209	10.29		25	1.4019
			189	22		85	1.1134
POST	566	1	188	31.2	38	-40	1.6466
			190	17.02		25	1.3853
			108	15.63		85	1.1549
PRE	569	1	107	4.461	48	-40	1.6512
			109	23.8		25	1.4061
			89	5.104		85	1.1208
POST	569	1	88	13	46	-40	1.6451
			90	0.5822		25	1.4022
			67	46.58		85	1.1555
PRE	570	1	66	36.25	38	-40	1.6639
			68	54.74		25	1.4142
			56	18.55		85	1.1259
POST	570	1	55	29.92	36	-40	1.6711
			57	9.716		25	1.4188
			162	15.72		85	1.1614
PRE	572	1	161	20.59	43	-40	1.6785
			163	7.177		25	1.4298
			160	63.16		85	1.1138
POST	572	1	159	72.19	41	-40	1.6421
			161	53.41		25	1.4012
			64	16.95		85	1.1556
PRE	576	1	63	25.67	44	-40	1.6598
			65	6.791		25	1.4079
			45	42.53		85	1.1125
POST	576	1	44	51.26	42	-40	1.66
			46	33.25		25	1.4012
			23	0.697		85	1.1552
PRE	580	1	22	8.515	41	-40	1.6714
			24	7.288		25	1.4218
			19	2.93		85	1.1021
POST	580	1	18	10.23	38	-40	1.6417
			20	6.576		25	1.3957
			118	0.6458		85	1.1163
PRE	73	1	117	9.812	48	-40	1.653
			119	10.52		25	1.3965
			118	0.6458		85	1.1163
POST	73	1	117	9.812	48	-40	1.653
			119	10.52		25	1.3965
			Not Matchable			85	1.1256
PRE	88	Not Matchable		48	-40	1.6565	
POST	88	Not Matchable		46	25	1.4035	
					85	1.1178	



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **43/44**

Test	ID	Matchable	Value	Black Offset/ Reg	Temp Calib	Voltage
					-40	1.6211
					25	1.3829

Observations:

- There is a difference in register setting for the odd/even column matching in DR mode before and after radiation. The same observation was already made during the evaluation campaign in 2007. (ref. HAS Low Dose Rate radiation Test Report ESA/ESTEC/TEC-ECC/09.07/LS). The same variations were measured after annealing.
- There is a small difference noticeable for the NDR black offset parameter. As this test is done manually the small difference is probably due to test-to-test variation.
- The on-chip temperature diode is unaffected after radiation.



ON Semiconductor

HYDRA_LAPLACE

Réf.:ESA_6429_TID_001 Rév.: **B**

Date : 23/11/2012 Séq. : 1

Statut : **Final**

Classification: NC Page : **44/44**

9.CONCLUSIONS

The HAS2 image sensor has been irradiated till 144 KRad using different biasing schemes. After radiation the devices were annealed for 3 months at room temperature, 1 month at 50 degC and 1 week at 125 degC. Annealing was also done using different biasing schemes.

From the observations the main conclusions are:

- There is no difference observed in dark current increase between sensors that are being biased (operational) and sensors that are in the off state (all pins grounded).
- During 50degC annealing, dark current is increasing on those sensors which are in the off state.
- During 125degC annealing, dark current is decreasing on all the parts.
- The dark current doubling temperature is increasing on those parts which are annealed in the ON state. The ones annealed in the off state do not show an increase.
- There is no difference between devices from different diffusion lots.