RHM

Intelligent Memory heavy-ion SEE test report

RHM-IDA-TN3-5

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1 Overview

On September 20, 2017, a test was performed at RADEF to determine the sensitivity of Intelligent Memory DDR3 SDRAM devices to single-event effects (SEUs and SEFIs) caused by heavy-ion irradiation.

Intelligent Memory devices are supposed to be more radiation tolerant than standard devices due to cell twinning and integrated error correction (ECC).

2 Test facility

The test was performed at RADEF, Jyväskylä, Finland, using the 9.3 MeV/u ion cocktail:

Ion	Energy [MeV]	Range [µm]	LET (surface) [MeV cm² / mg]	LET (60 µm) [MeV cm² / mg]	Comments
$^{15}N^{4+}$	139	202	1.8	2.2	
$^{20}Ne^{6+}$	186	146	3.6	4.7	
$^{40}Ar^{12+}$	372	118	10.2	13.4	
$^{56}Fe^{15+}$	523	97	18.5	26.4	
$^{82}Kr^{22+}$	768	94	32.1	40.6	
$^{131}Xe^{35+}$	1217	89	60.0	67.2	

3 Samples

One device type was tested:

Part ID	Manufacturer	Part number	Capacity	Feature size	Date code
Im5	Intelligent Memory	IMX5108D3EEBG-15EI	512 Mbit	Unknown	1537

All samples are housed in a flip-chip BGA package, as per the DDR3 SDRAM standard. All samples had been prepared for backside irradiation by thinning them to a die thickness of ≈ 60 µm. Thinning has been performed by Fraunhofer IOF, Jena.

Figure 1: Im5 sample photo

Normally, the integrated error correction is enabled. The procedure for disabling the error correction has been provided to IDA under NDA and has been implemented in the test equipment.

4 Test procedure and test results

Devices have been tested in read mode, both with the internal error correction enabled and disabled.

Before every run, the DUT was power-cycled (which enables the error correction). For runs without error correction, the procedure to disable error correction was applied. A pseudo-random pattern was written to the DUT.

The DUT was then irradiated while repeatedly reading the whole address space; errors were not corrected during irradiation. Error data from all read operations was displayed for preliminary analysis and stored on disk. In case of a device SEFI, the irradiation run was terminated manually.

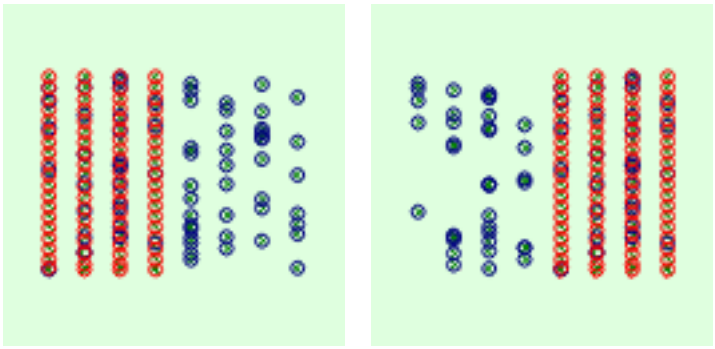
4.1 Error classification

The following error classes have been observed:

- SEUs: isolated single-bit errors
- Stuck bits: isolated single-bit errors that are still present after power-cycling the device and rewriting the affected cell
- Row errors: many errors in a single row of logical address space
- Column errors: many errors in a single column of logical address space
- Device SEFIs: extended erroneous regions of errors in logical address space
- Block errors: regions of 8 or 4 columns and 256 rows, as described in more detail below

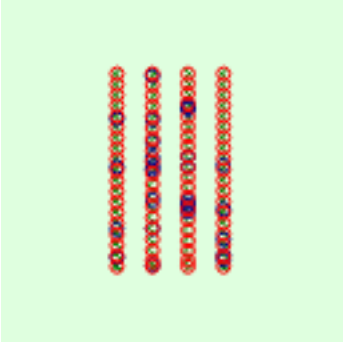
Note that unlike the other error classes, block errors have not been observed for other types of DDR3 SDRAM.

There are two types of block errors, type A and type B, both of which extend across 256 consecutive rows, starting at a whole multiple of 256. Type-A block errors extend across eight columns, starting at a whole multiple of eight, and follow one of two typical patterns:



Here, a blue circle indicates a word with a single erroneous bit, and a red circle indicates a word with more than one erroneous bit. In the columns with the higher error density (red), almost all words have an error. In the columns with the lower error density (blue), typically fewer than 20 words (out of 256) contain an error.

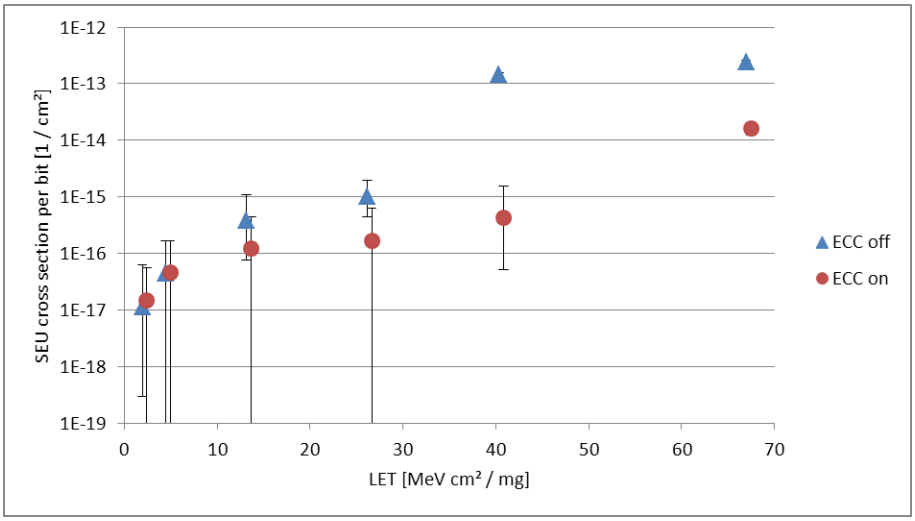
Type B block errors follow a similar pattern, but without the low-density part. Thus, they extend across four columns, starting a whole multiple of four:

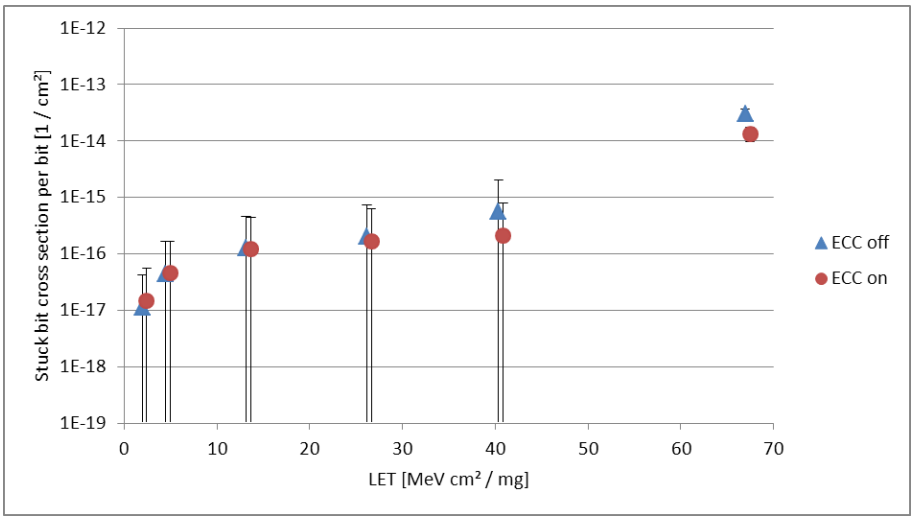


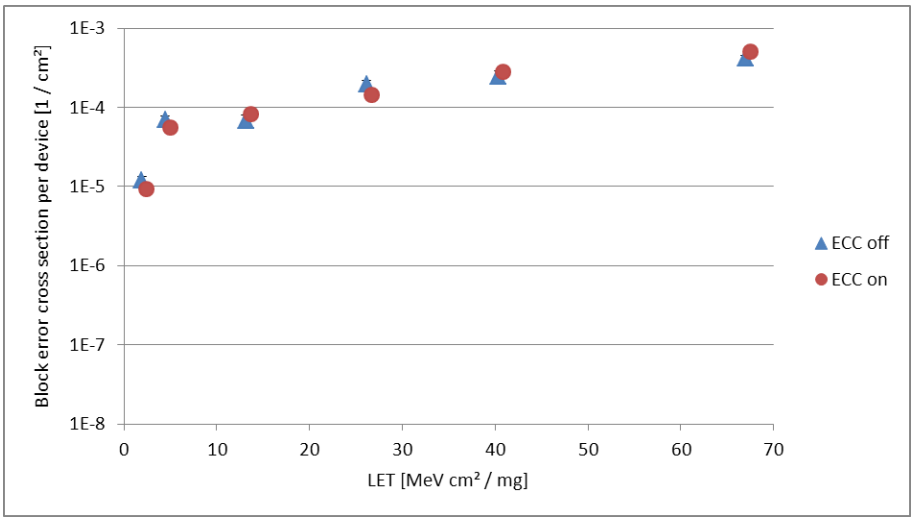
4.2 Error cross sections

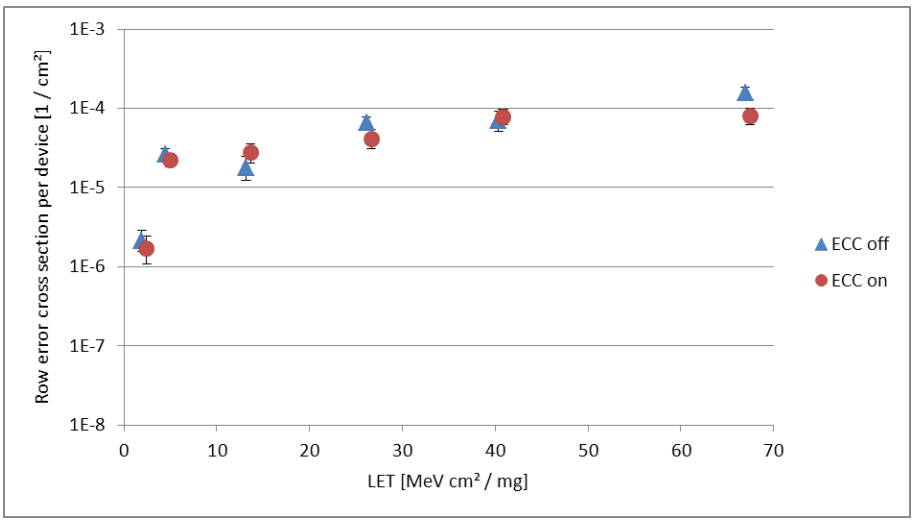
The error cross sections with ECC on and ECC off are shown in the following figures. In cases where the number of errors was zero, the shown value is the cross section that would have resulted from one error; this case can be recognized by the lower error bar which extends all the way to 0 ($-\infty$ in the logarithmic plot). The values are slightly shifted in the horizontal (LET) direction to make them more visually distinct; this does not correspond to an actual change in LET.

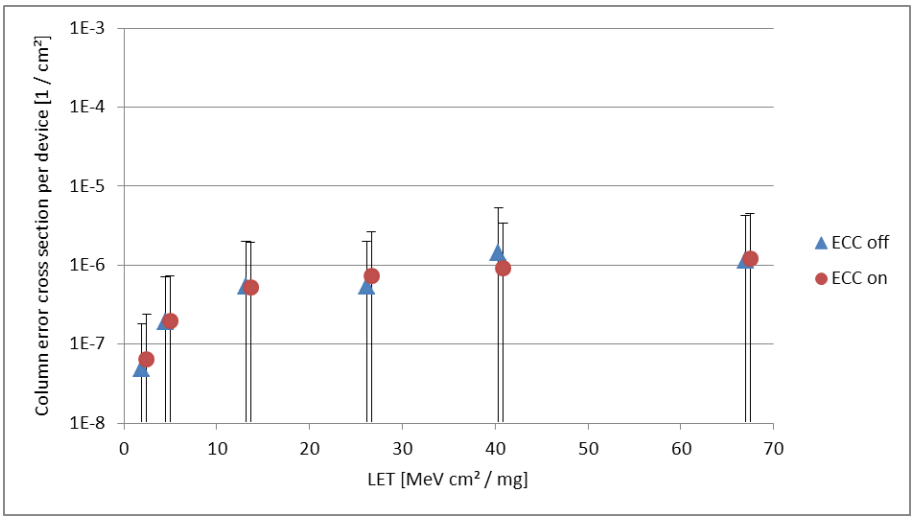
With error correction on, almost all runs had exclusively type-A block errors; with error correction off, almost all runs had exclusively type-B block errors (note that block errors are more severe with error-correction enabled). A few runs (3 with error correction off and 1 with error correction on, out of 92 total) had both types of block errors.

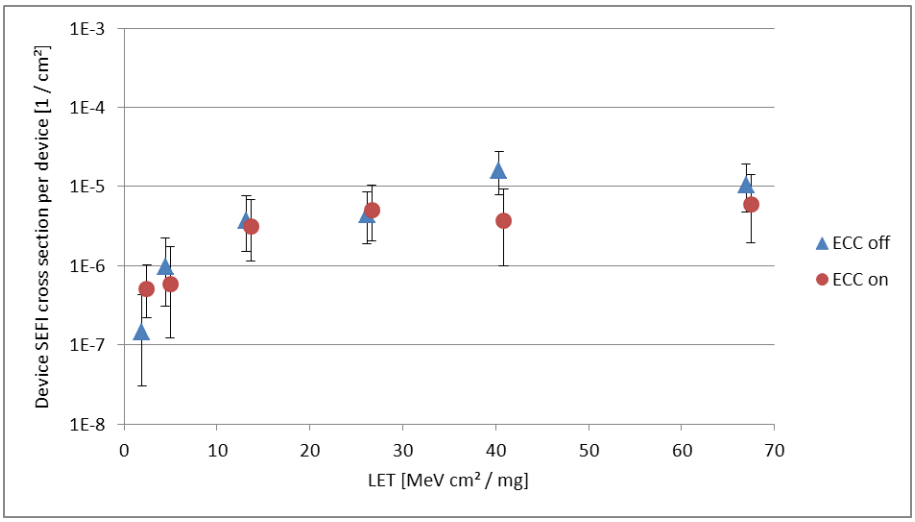



Stuck bit cross section per bit [1 / cm²]
1E-12
1E-13
1E-14
1E-15
1E-16
1E-17
1E-18
1E-19
0
10
20
30
40
50
60
70
LET [MeV cm² / mg]
ECC off
ECC on


Block error cross section per device [1 / cm²]
1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
0
10
20
30
40
50
60
70
LET [MeV cm² / mg]
ECC off
ECC on


Row error cross section per device [1 / cm²]
1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
0
10
20
30
40
50
60
70
LET [MeV cm² / mg]
ECC off
ECC on


Column error cross section per device [1 / cm²]
1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
0
10
20
30
40
50
60
70
LET [MeV cm² / mg]
ECC off
ECC on


Device SEFI cross section per device [1 / cm²]
1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
0
10
20
30
40
50
60
70
LET [MeV cm² / mg]
ECC off
ECC on