RHM

DDR3 SDRAM stuck bit test report

RHM-IDA-TN3-3

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1 Overview

On September 19, 2017, a test was performed at RADEF to determine the sensitivity of DDR3 SDRAM devices to stuck bits caused by heavy ion irradiation, as well as long-term annealing of these stuck bits. Stuck bits are memory cells that are always read as the same value, regardless of the value previously written to that cell.

2 Test facility

The test was performed at RADEF, Jyväskylä, Finland, using the 9.3 MeV/u ion cocktail:

Ion	Energy [MeV]	Range [µm]	LET (surface) [MeV cm² / mg]	LET (60 µm) [MeV cm² / mg]
$^{15}N^{4+}$	139	202	1.8	2.2
$^{20}Ne^{6+}$	186	146	3.6	4.7
$^{40}Ar^{12+}$	372	118	10.2	13.4
$^{56}Fe^{15+}$	523	97	18.5	26.4
$^{82}Kr^{22+}$	768	94	32.1	40.6
$^{131}Xe^{35+}$	1217	89	60.0	67.2

3 Samples

Two device types were tested:

Part ID	Manufacturer	Part number	Capacity	Feature size	Date code
Hyn4	Hynix	H5TQ4G83MFR-H9C	4 Gbit	Unknown	1223
Sam4	Samsung	K4B4G0846B-HCH9	4 Gbit	35 nm	1216

Hyn4 Sam4

Figure 1: Package photos

All samples are housed in a flip-chip BGA package, as per the DDR3 SDRAM standard. All samples have been prepared for backside irradiation by thinning them to a die thickness of ≈ 60 µm. Thinning has been performed by Fraunhofer IOF, Jena.

4 Test procedure

Devices were tested in (a) unbiased mode and (b) storage mode. All irradiation runs were performed in vacuum.

In unbiased mode, the device was irradiated while powered off. After the end of the irradiation, the vacuum chamber was vented, the device powered on, initialized, and written with a pseudo-random data pattern (containing an equal number of ones and zeros). The device was then read and the data compared to the original pattern; any discrepancies constitute a stuck bit.

In storage mode, the device was powered on, initialized, and written with the same pseudo-random pattern as used in unbiased mode. The device was then irradiated while performing periodic refresh operations with the standard refresh interval of $t_{\mathrm{REFI}} = 7.8\ \mu\mathrm{s}$. After the end of the irradiation, the device was power-cycled in order to clear any SEFIs that might have occurred during the irradiation and to establish the same conditions as for unbiased mode. The vacuum chamber was vented and the device was written and read as described above in order to determine the stuck bits.

Each sample was only used for either biased or unbiased irradiation with a single ion species. In any case, irradiation was repeated until at least 1000 stuck bits had been observed or until a fluence of $10^7/\mathrm{cm}^2$ had been reached.

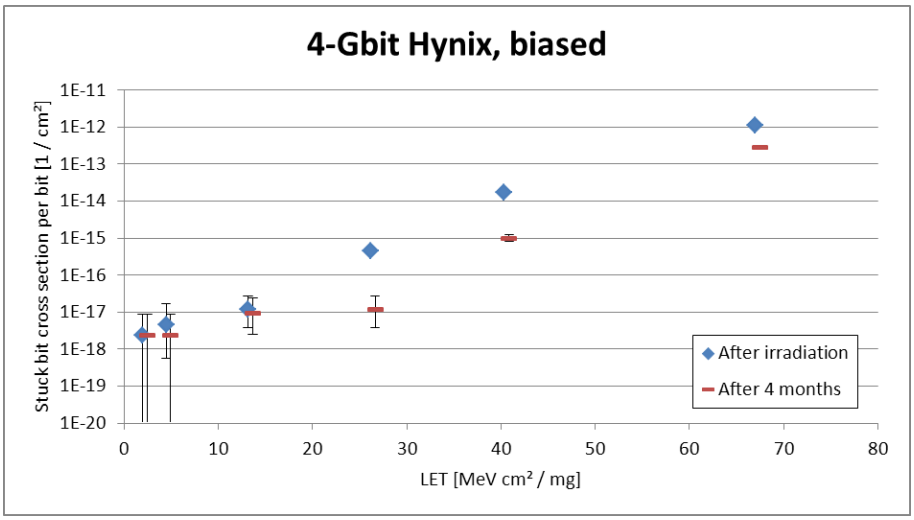
After the end of the test campaign, the samples were stored unbiased at room temperature. Four months after irradiation, the remaining number of stuck bits was determined. The same pseudo-random pattern was used for all test runs. All tests were performed with the standard refresh interval of $t_{\mathrm{REFI}} = 7.8\ \mu\mathrm{s}$.

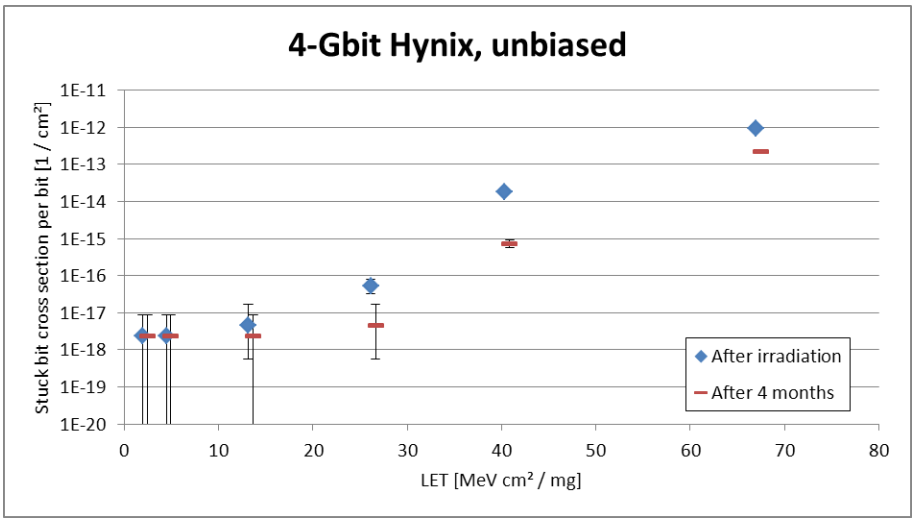
5 Test results

The following figures show the stuck-bit cross sections immediately after the end of the irradiation (blue diamonds) and after four months (red lines). The error bars represent the 95% confidence interval. All observed stuck bits were errors in the 1 → 0 direction for both tested device types. This is consistent with previous test results for Samsung and Hynix types (for other device types, 1 → 0 and 1 → 0 stuck bits have been found to be equally likely).

Note that a stuck bit will only cause an error if the value written to the cell is different from the value that the cell is stuck at. The indicated cross section refers to the *observed* number of stuck bits, i. e. the number of errors caused by stuck bits. Since the pseudo-random pattern has an equal number of ones and zeros, only half of the total stuck bits are observed (this is independent of the preferred polarity of stuck bits). The total number of stuck bits is therefore twice the reported value. However, in a typical application that stores an equal number of ones and zeros, only half of the stuck bits will cause an error. The expected number of errors in such an application therefore corresponds to the values reported here; the worst-case number of errors is twice that value.

In cases where the number of stuck bits was zero, the shown value is the cross section that would have resulted from one stuck bit; this case can be recognized by the lower error bar which extends all the way to 0 ($-\infty$ in the logarithmic plot). The values after four months (red lines) have been slightly shifted to the right so the error bars can be distinguished.


4-Gbit Hynix, biased
Stuck bit cross section per bit [1 / cm²]
1E-11
1E-12
1E-13
1E-14
1E-15
1E-16
1E-17
1E-18
1E-19
1E-20
0
10
20
30
40
50
60
70
80
LET [MeV cm² / mg]
After irradiation
After 4 months


4-Gbit Hynix, unbiased
Stuck bit cross section per bit [1 / cm²]
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1E-12
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1E-17
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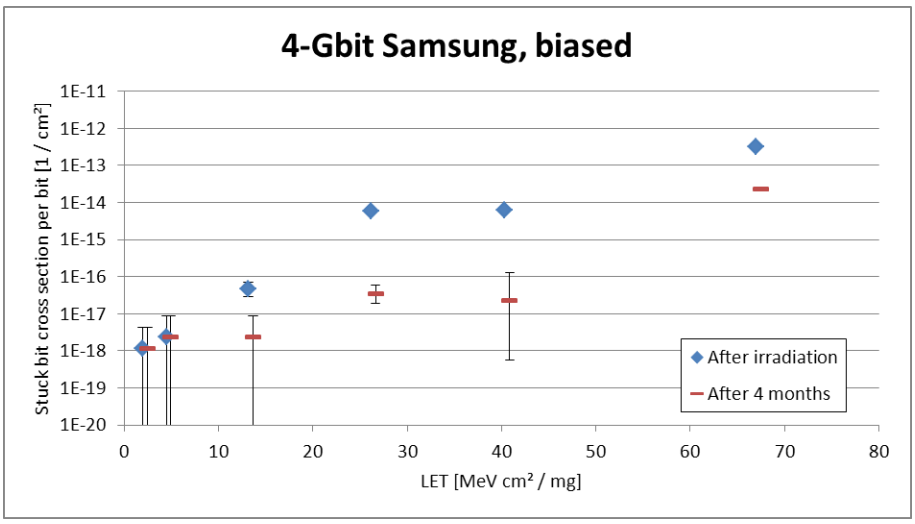
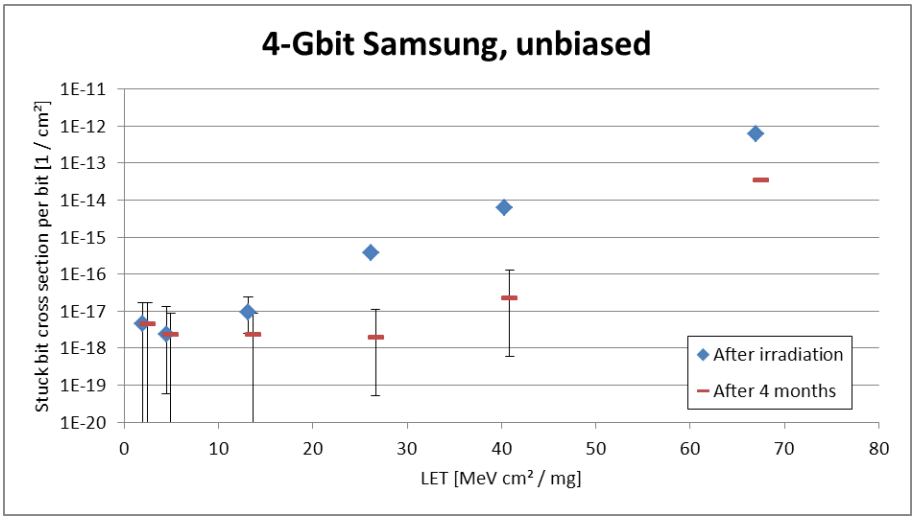
LET [MeV cm² / mg]
After irradiation
After 4 months


4-Gbit Samsung, biased
Stuck bit cross section per bit [1 / cm²]
1E-11
1E-12
1E-13
1E-14
1E-15
1E-16
1E-17
1E-18
1E-19
1E-20
0
10
20
30
40
50
60
70
80
LET [MeV cm² / mg]
After irradiation
After 4 months


4-Gbit Samsung, unbiased
Stuck bit cross section per bit [1 / cm²]
1E-11
1E-12
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1E-14
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1E-16
1E-17
1E-18
1E-19
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LET [MeV cm² / mg]
After irradiation
After 4 months