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SY10x7A_ESCC9000 ASIC Evaluation

Radiation Test Report – Total Dose Steady State

High and Low Dose Rates

	NAME	**FUNCTION**	**SIGNATURE**	**DATE**
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1 Introduction

1.1 Scope

Ionizing radiation can cause parametric degradation and ultimately functional failure in electronic devices. In BiCMOS processes the damage occurs via electron-hole pair production, transport and trapping in the dielectric (silicon dioxide) regions, as well as a reduction in the gain or breakdown voltage of the bipolar devices. Bipolar devices may also exhibit an enhanced low dose rate sensitivity (ELDRS). Since there is no way to predict ELDRS, low dose rate testing is also necessary.

The purpose of this test session is to assess the radiation hardness of the SY1007A RF front-end [1] and the SY1017A AD/DA-converter and PLL frequency synthesizer [2] ASICs up to a total dose $>$2kGy(Si) ($>$200krad(Si)). These devices are improved versions of the SY1007 and SY1017C chip-set [3, 4], which were redesigned to improve both electrical performances and radiation hardness.

The tests were performed in July 2020 at the *ESTEC Co-60 irradiation laboratory, Keplerlaan 1, 2201 AZ Noordwijk, the Netherlands*. As ionizing radiation source a Co-60 gamma source is used. The test session was prepared by Saphyrion and carried out by ESA personnel.

1.2 Acronyms

AD	Applicable Documents
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
ASIC	Application Specific IC
BGA	Ball Grid Array
BJT	Bipolar Junction Transistor
BOM	Bill Of Materials
CBGA	Ceramic Ball Grid Array
CoB	Chip on Board
CP	Compression Point (1dB)
DAC	Digital to Analogue Converter
DBM	Double Balanced Mixer
DUT	Device Under Test
ECC	Error Correction Code
ELDRS	Enhanced Low Dose Rate Sensitivity
ESA	European Space Agency
ESCC	European Space Components Coordination
GAL	Galileo
GLO	GLONASS
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GUI	Graphical User Interface
HI	Heavy Ion
HBT	Heterojunction Bipolar Transistor
IB	Interface Board
IC	Integrated Circuit
iCP	CP referred to the input
IF	Intermediate Frequency
iIP3	IP3 referred to the input
IP3	3rd Order Intercept Point
LNA	Low Noise Amplifier
LET	Linear Energy Transfer
LO	Local Oscillator
LOCOS	LOCal Oxidation of Silicon
MOS	Metal Oxide Semiconductor
MPW	Multi-Project Wafer
N/A	Not Applicable
NF	Noise Figure
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PTAT	Proportional to Absolute Temperature
PWM	Pulse Width Modulation
RD	Reference Document
RF	Radio Frequency
RT	Radiation Test
RTHI	Heavy Ions Radiation Test
RTTD	Total Dose Radiation Test
SAW	Surface Acoustic Wave
SEE	Single Event Effects
SEL	Single Event Latch-up
SET	Single Event Transient
SEU	Single Event Upset
SiGe	Silicon Germanium (HBT)
TB	Test Board
TBC	To Be Confirmed
TBD	To Be Defined
TCXO	Temp. Comp. Crystal Oscillator
TD	Total Dose
VCA	Voltage Controlled Amplifier
VCO	Voltage Controlled Oscillator

2 Tested Items

Two devices, i.e. the SY1007AS RF front-end and the SY1017AS AD-DA converter, have been tested in this session [6]. Both devices were designed using the AMS S35 0.35μm SiGe process [8, 9]. The two designs were taped out on the *same gdsII file*, called SY10x7A_Wafer_2019r1, and produced together on the *same engineering lot*, thus each wafer contains both SY1007AS and SY1017AS designs.

Twelve wafers, with the lot ID G46284.1 were produced in September 2019. Eleven samples per type – 6 biased and 5 unbiased – were tested in compliance with the recommended sample size given in ESCC 22900 [11] guidelines, while one sample per type was kept as a non-irradiated spare. The devices for the TID tests were taken from wafer number 7.

2.1 SY1007AS DUTs

The SY1007A test items (DUTs) used for this total dose irradiation test session are the following:

- **Top cell name (SPH database) :** SY10x7A_Wafer_2019r1
- **Part manufacturer :** Saphyrion Sagl
- **Part number :** SY1007AS [1]
- **Die marking :** SY1007A, SPH-REV 2, ©11 2017
- **AMS revision block :** 40412_A
- **Wafer lot ID :** G46284.1
- **Wafer number :** 7
- **Test fixture (PCB) :** TB-1007A-COB V1.0
- **Process :** AMS S35D4H5 [8, 9]
- **DUTs biased :** 6x – SY1007A_W7_40412A_01 to SY1007A_W7_40412A_06
- **DUTs unbiased :** 5x – SY1007A_W7_40412A_07 to SY1007A_W7_40412A_11
- **DUTs spare :** 1x – SY1007A_W7_40412A_12 – *See Table 4 for details*

The SY1007AS DUTs, which were picked at random from wafer 7, have a size of 1570μm x 1390μm (without scribe line), use SiGe Heterojunction Bipolar Transistors (HBT) in all RF/IF blocks and a combination of HBT and CMOS transistors in the analogue circuits. The digital section is implemented using only CMOS transistors. The active zone is approximately 3.5μm deep (N-well junction depth).

2.2 SY1017AS DUTs

The SY1017A test items (DUTs) used for this total dose irradiation test session are the following:

- **Top cell name (SPH database) :** SY10x7A_Wafer_2019r1.
- **Part manufacturer :** Saphyrion Sagl
- **Part number :** SY1017AS [2]
- **Die marking :** SY1017A, SPH-REV 3, ©11 2017
- **AMS revision block :** 40412_B.
- **Wafer lot ID :** G46284.1
- **Wafer number :** 7
- **Test fixture (PCB) :** TB-ADULA V1.1
- **Process :** AMS S35D4H5 [8, 9]
- **DUTs biased :** 6x – SY1017A_W7_40412B_01 to SY1017A_W7_40412B_06
- **DUTs unbiased :** 5x – SY1017A_W7_40412B_07 to SY1017A_W7_40412B_11
- **DUTs spare :** 1x – SY1017A_W7_40412B_12 – *See Table 12 for details*

The SY1017AS DUTs, which were picked at random from wafer 7, have a size of 1170μm x 1120μm (without scribe line), use a combination of SiGe Heterojunction Bipolar Transistors (HBT) and CMOS in the analogue circuits. The digital section is implemented using only CMOS transistors. The active zone is approximately 3.5μm deep (N-well junction depth).

2.3 Die Drawings and Photographs

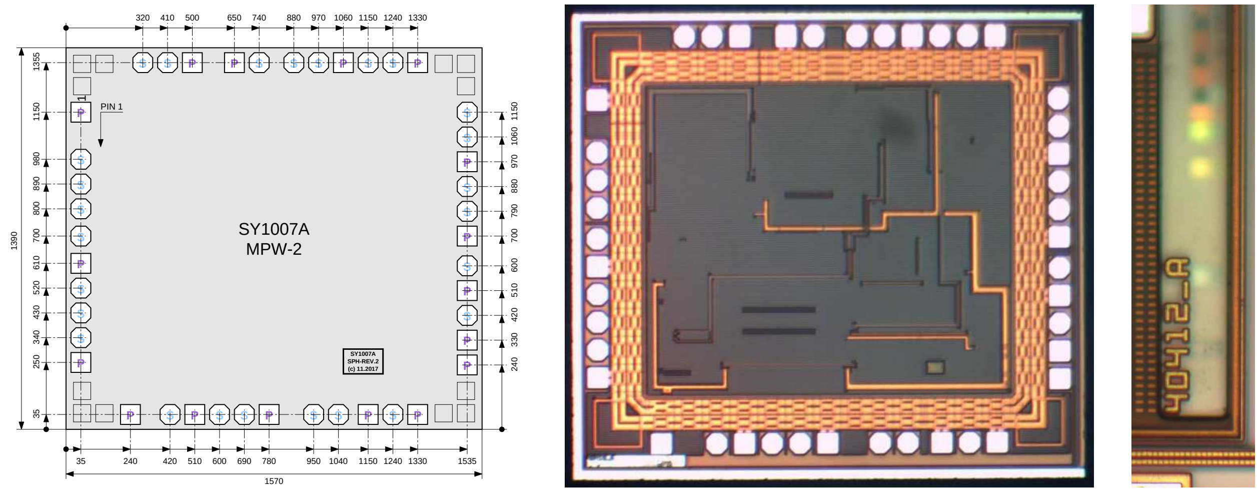


Figure 1: SY1007AS die drawing (left), photograph (center) and marking (right).

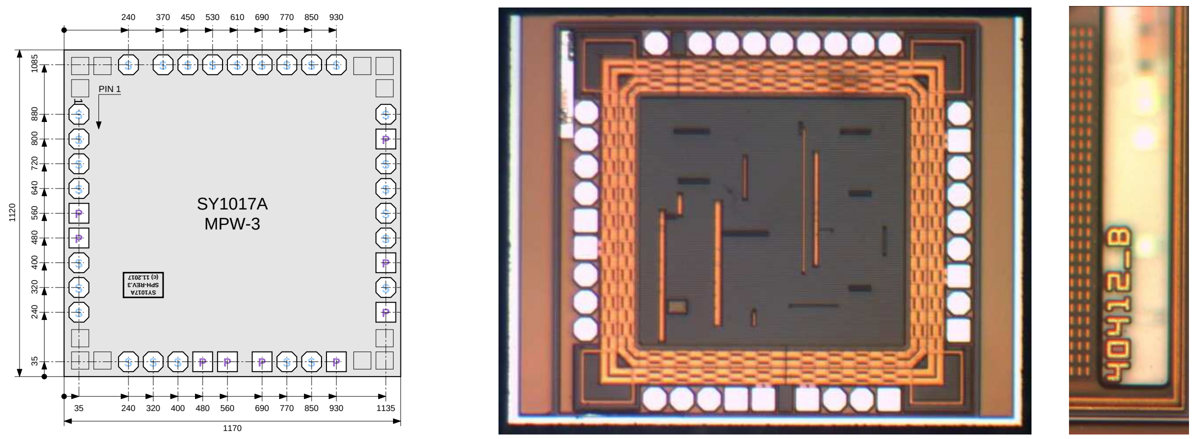


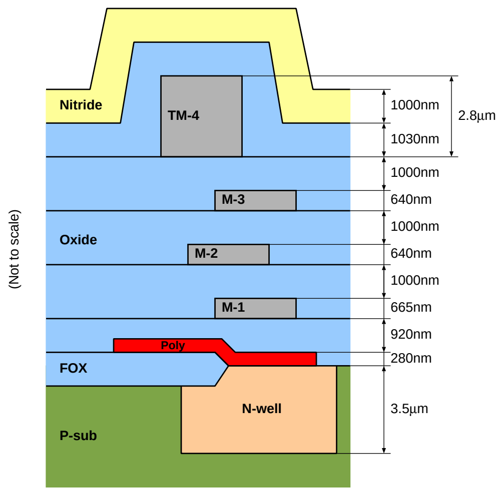
Figure 2: SY1017AS die drawing (left), photograph (center) and marking (right).

2.4 DUT Physical Characteristics

The DUTs are manufactured in the AMS S35 SiGe 350nm process. The main characteristics and dimensions of this process are:

- **Metal layers:** 4x aluminum, 2.8μm top metal.
- **Field oxide thickness:** 290nm SiO_2.
- **Gate oxide thickness:** 7.6nm SiO_2.
- **Passivation thickness:** 1μm Si_3N_4 (on top).
- **N-well thickness:** 3.5μm.
- **Polymide thickness:** 4.5μm optional (not used).

Since the devices use bipolar transistors, low dose rate tests are necessary in addition to standard rate tests, in order to check ELDRS.



3 Test Fixtures

In order to test the SY1007A and SY1017A devices, specific test fixtures are required. These test fixtures consist of purpose-built PCBs on which the DUTs (SY1007A or SY1017A) and all required external components (passive components, baluns, matching transformers, etc.) are mounted. This means that each DUT requires its own test fixture. A heater resistor and a temperature sensor are mounted on the back side of the test fixtures to allow temperature measurement and control.

3.1 Test Fixtures Layouts

A photograph of the test fixtures for the SY1007A DUTs – named TB-1007A-COB V1.0 – and the SY1017A DUTs – named TB-ADULA V1.1 – are shown in Figure 3. A total of fourteen samples of the SY1007A and the SY1017A DUTs were prepared and mounted as described in Section 3.2 below, such that some redundancy is available.

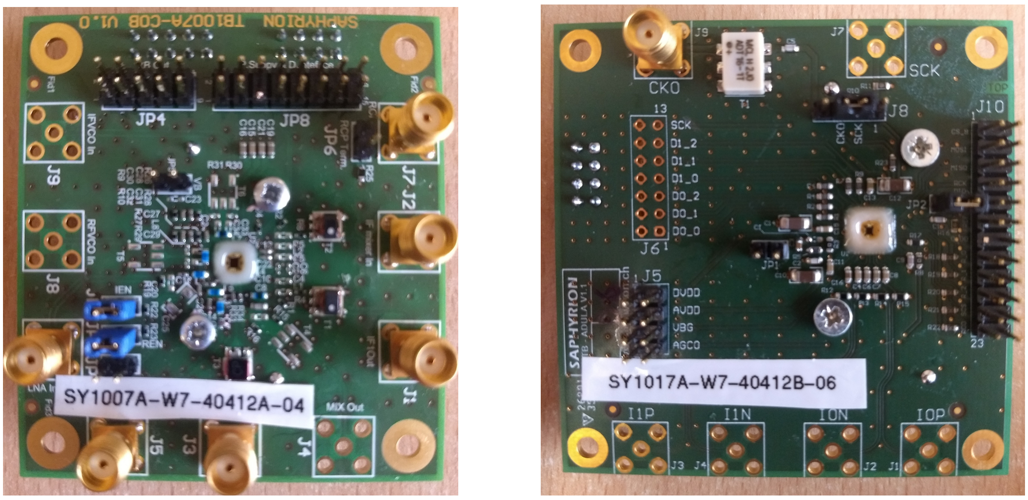


Figure 3: Photograph of the TB-1007A-COB V1.0 (left) and TB-ADULA V1.1 (right) test boards.

3.2 DUT Mounting

For these TID tests the same test fixtures prepared for the heavy ions testing [12] were used. The DUTs were mounted CoB – i.e. the ASIC dies have been attached and bonded directly to the PCBs – on the test fixtures and covered with glob-top material to protect them. The open cavities can be seen in the photographs appearing in Figure 3. To avoid damages during rigging, the open cavity devices were covered with plastic lids, as can be seen in Figure 8.

3.3 Schematic Diagram of the TB-1007A-COB V1.0 Fixture

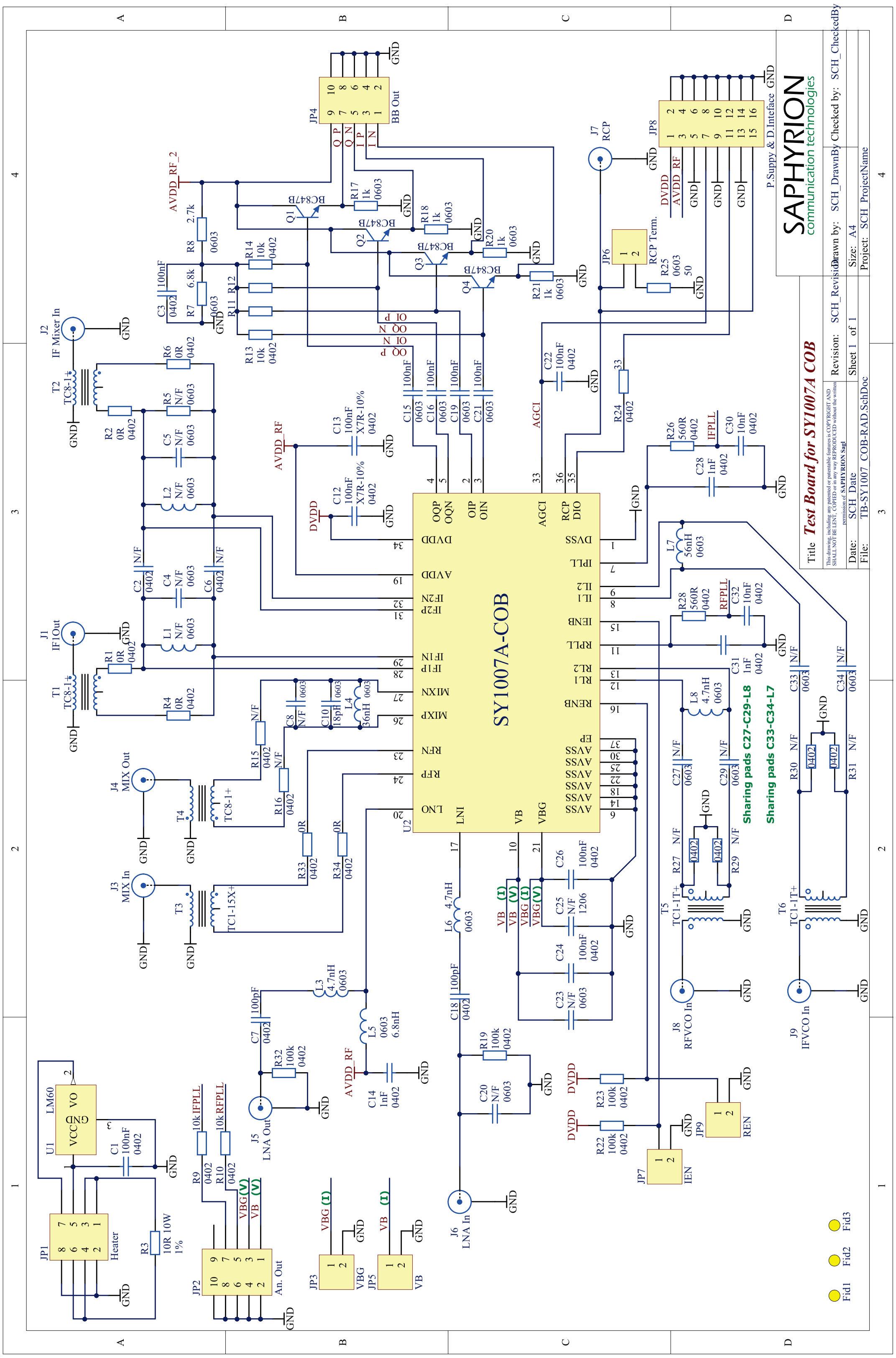


Figure 4: Schematic diagram of the TB-1007A-COB V1.0 test fixture.

3.4 Schematic Diagram of the TB-ADULA V1.1 Fixture

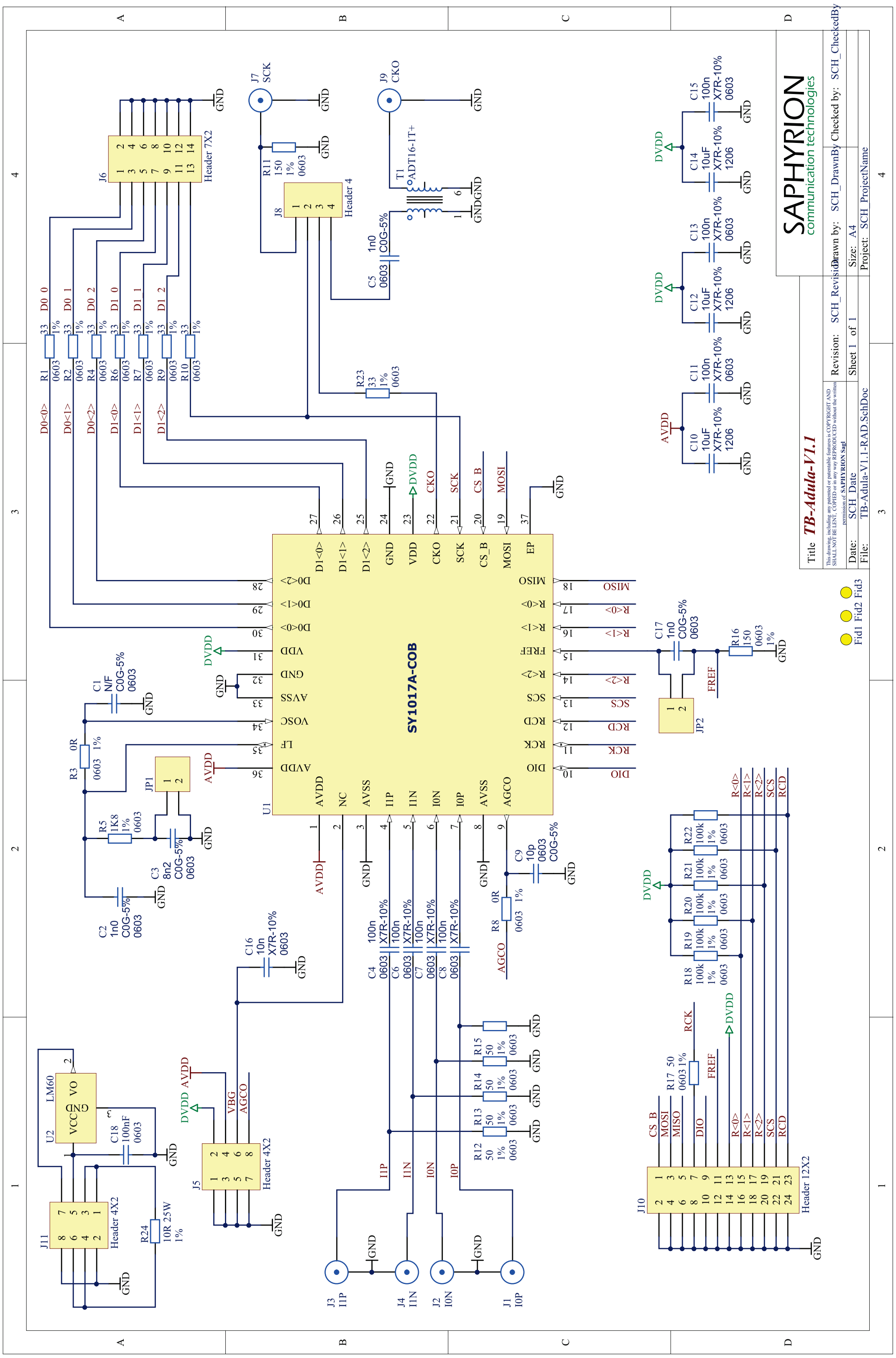


Figure 5: Schematic diagram of the TB-ADULA V1.1 test fixture.

4 Test Environment

The total dose tests were performed at the *ESTEC Co-60 irradiation laboratory, Keplerlaan 1, 2201 AZ Noordwijk, the Netherlands*. As ionizing radiation source a Co-60 gamma source is used.

In order to simplify test set-up and execution, as well as reduce the burden of carrying equipment to the test site, a purpose-built control and acquisition device – the SM314 interface board – was used instead of standard laboratory instruments. The test fixtures with the DUTs and their SM314 interface boards were mounted on a holder that was in turn mounted on the trolley within the radiation chamber (Section 4.4). The SM314 boards were shielded from gamma radiation with lead bricks.

4.1 SM314 Interface Board

The SM314 interface board is an acquisition device used to program and collect data from a DUT mounted on its test board. It offers various analogue and digital interfaces, temperature control and can be remote controlled by an host computer using a serial RS-232 port or an USB connection, via a terminal or the *SY10xxTester* driver application. The SM314 acquisition board provides the following I/Os:

- 2x heater controllers, used to control the temperature of the DUTs.
- 11x analogue inputs (8 external), with 10 bit resolution.
- 4x adjustable analogue outputs with current and voltage measurement.
- 1x SY10XXSPI controller, used to set the clock frequency of the DUT.
- Digital I/Os used to control the DUTs attached to the board.

This device therefore replaces several bench-top instruments at once and provides all the functionality needed to program and test the DUTs while controlling their temperature.

Figure 6 left shows the block diagram of the SM314 interface board, with the available I/Os and their purpose, while Figure 6 right shows a photograph of the board. The SM314, with size is 110mm x 90mm x 18mm, uses commercial off-the-shelf non radiation hardened components and a FR4 PCB substrate, it therefore shall be shielded from the gamma radiation with lead bricks. A complete description of the SM314 and its driver application (SY10xxTester) is included in its user's manual [5].

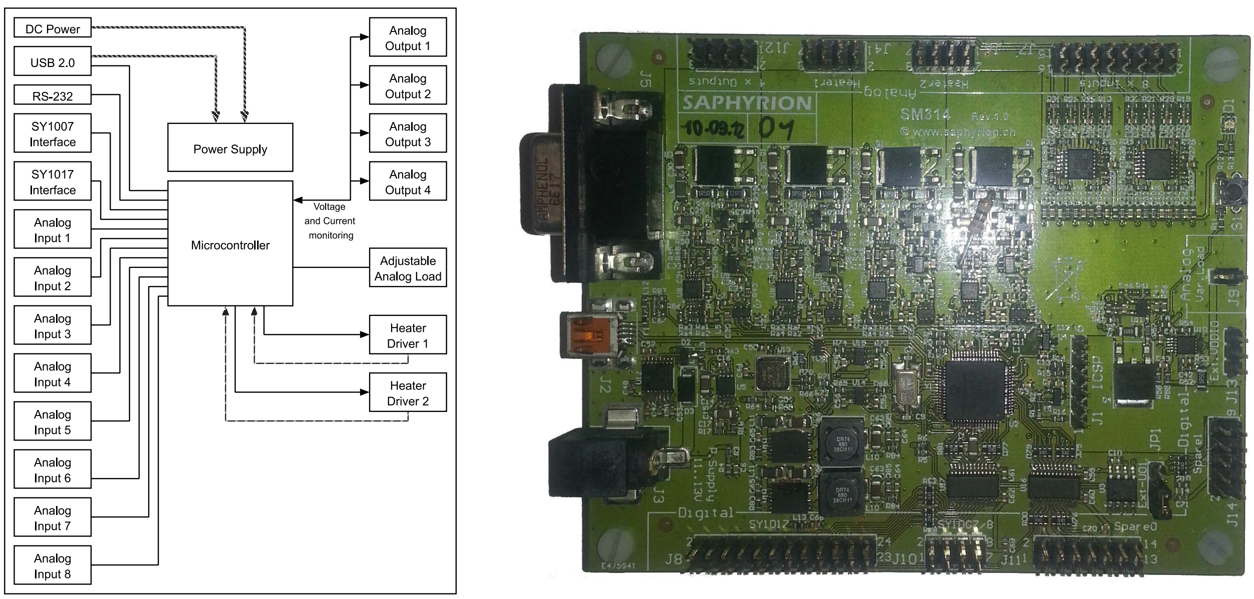


Figure 6: Block diagram (l) and photograph (r) of the SM314 interface board.

4.2 SY10xxTester Application

During this test the DUTs and the SM314 were controlled with the *SY10xxTester* application, which provides a GUI that allows the user to enter appropriate configurations to DUT and SM314 and to log all performed measurements to the computer's file system for subsequent analysis. The following functions are controlled:

- Select the DUT type (SY1007A, SY1017A).
- Select the clock frequency and amplitude.
- Program and read back all registers of the DUT.
- Define min/max limits for each measured value.
- Enable the temperature regulator, set the temperature and the coefficients of the PID regulator.
- Define the signals to be logged and the log interval.

Figure 7 shows screen-dumps of the GUI, i.e. DUT selection (top); temperature control, clock and log time interval (middle); registers of DUT and SM314, and min/max limits (bottom).

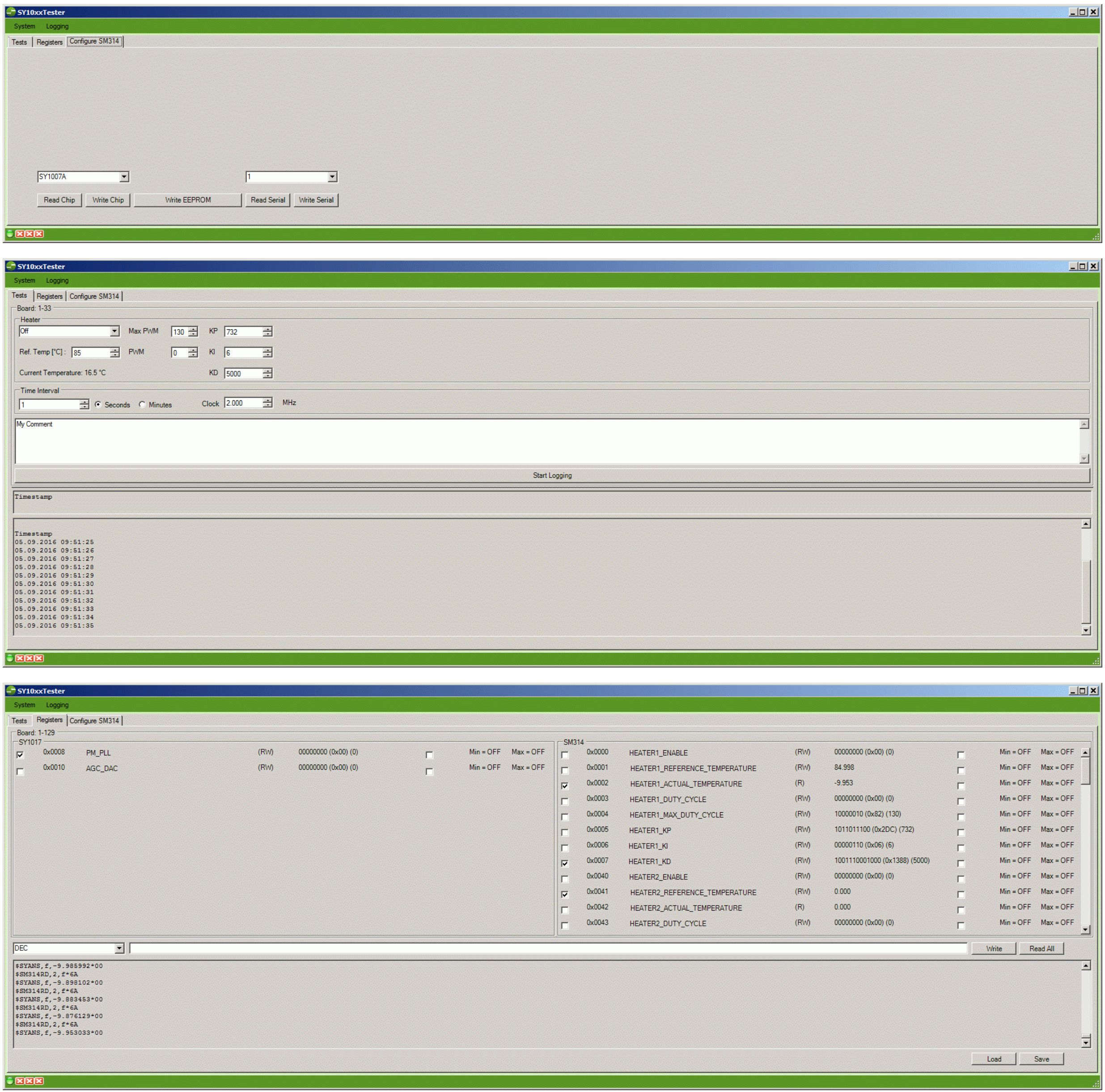


Figure 7: Screen-dumps of the SY10xxTester GUI.

4.3 Test Frame

In order to hold the test boards with the DUTs in the irradiation chamber, the test boards were mounted on a carrier plate. A photo of the plate, with a size of 420mm x 330mm, is shown in Figure 8.

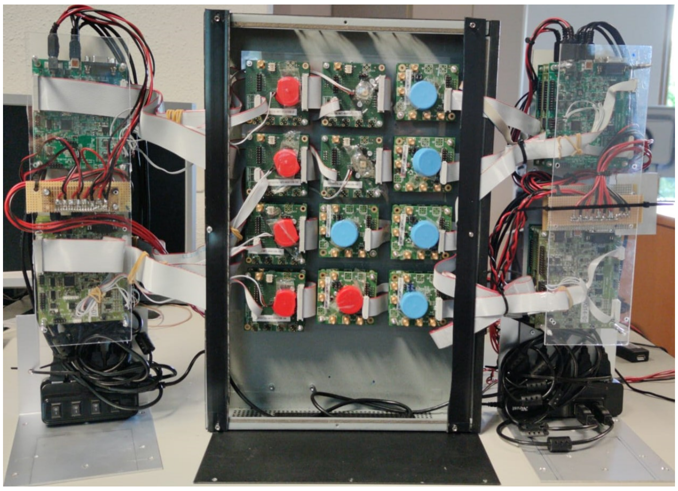


Figure 8: Photo of the complete test frame with the DUTs and SM314.

The DUTs are mounted as shown in the photo and the SM314 devices – six per side – are mounted on the edges of the holder plate. They will be protected against radiation with lead bricks during the test session.

4.4 Test Facility

The TID testing was performed using the ESTEC Co-60 facility. A sketch of the facility is shown in Figure 9. It consists of the radiation cell and a large external control room with 14 cable feed-throughs that enable the remote monitoring and controlling of experiments. The irradiation dose rates are changed by use of a remote positioning system consisting of a trolley on a rail system installed in the radiation cell. The radiation coverage angle of the cell is 26° H x 26° V. This means that the maximum size of the frame is limited, especially if large dose rates are required. The radiation facility has been reloaded on May 2016 with a 2000Ci Co-60 gamma source.

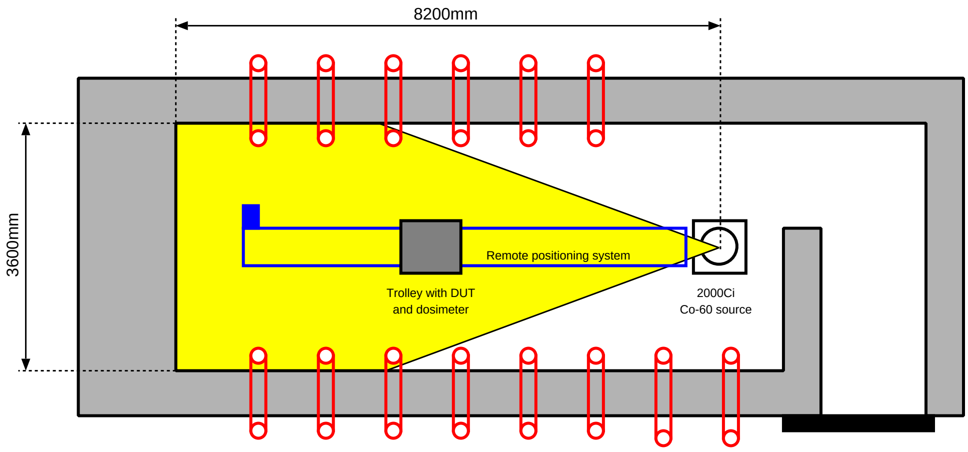


Figure 9: Sketch of the ESTEC Co-60 test facility.

Figure 10 shows the photographs of the Co-60 gamma source (left) and the test frame with DUTs mounted on the trolley (right). The SM314 interface boards are placed behind the Pb bricks that shield them from radiation and are thus not visible.

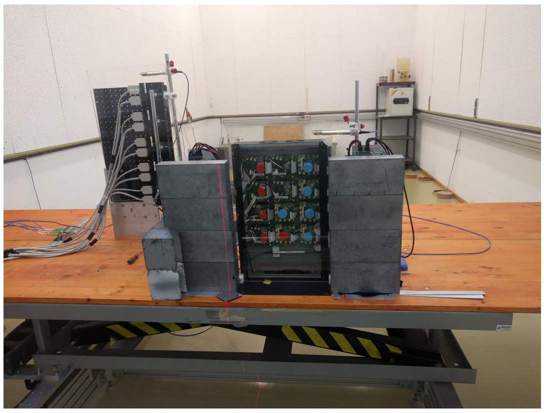



Figure 10: Photos of the test facility: Co-60 gamma source (l), test frame with DUTs (r).

4.5 Test Setup

Figure 11 shows the block diagram of the test set-up. Operation and data acquisition have been automated with a notebook computer (Dell Latitude D810) that is placed in the control room near the radiation cell.

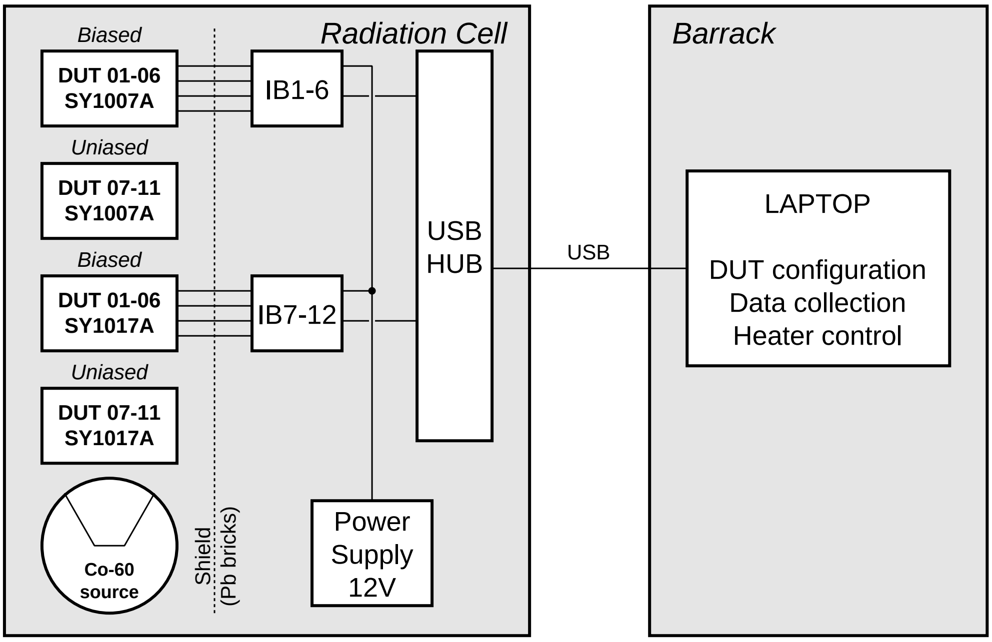


Figure 11: Block diagram of the test set-up.

5 Test Configuration

5.1 Radiation Rates

The tests were performed in July 2020 at the ESTEC Co-60 irradiation laboratory, Keplerlaan 1, 2201 AZ Noordwijk, the Netherlands. Since the DUTs are implemented in a SiGe BiCMOS process and may thus exhibit ELDRS, the total dose test was done for both *Window 1* (standard rate) and *Window 2* (low rate) of the ESCC basic specification No. 22900 [11]. The reference test plan [6] was used by ESA operators to prepare the irradiation laboratory and propose a final sequence depending on the actual Co-60 source availability. The actual dose rates used are shown below and in detail in Table 2 and 3.

Window 1:

- Dose rate $\approx$ 9Gy(Si)/h
- Distance = 118cm (unbiased DUTs), 115cm (biased DUTs)
- Run time = 119h
- Total dose $\approx$ 1000Gy(Si) per run

Window 2:

- Dose rate $\approx$ 3.34Gy(Si)/h
- Distance = 186.5cm (unbiased DUTs), 189.5cm (biased DUTs)
- Run time = 299h
- Total dose $\approx$ 1000Gy(Si) per run

5.2 Test Procedure

The purpose of this test session is to check sensitivity of the SY1007AS and SY1017AS DUTs to gamma irradiation at both high (Window 1) and low (Window 2) dose rates. Sample size and test conditions are selected according to ESCC 22900 [11]. The previous generation SY1007 and SY1017C devices have been successfully tested to a total dose of $>$1000Gy(Si), showing no failure and no detectable parametric drift. The test was actually stopped at 1350Gy(Si) for time and cost reasons rather than because of issues with the DUTs. The AMS S35 process used in the design of those parts, as well as the radiation hardening techniques used, have thus demonstrated that good radiation hardness can be achieved.

The SY1007AS and SY1017AS DUTs are designed using the same S35 process and use the same radiation hardening techniques as the previous parts, thus the same behavior is expected. A radiation test up to 2000Gy(Si) has been done on the new DUTs. In order to optimize resources and time, and owing to the good results of the previous generation devices, the complete electrical tests (that includes RF measurements) are only made after the 2000Gy(Si) radiation dose. Table 1 shows the sequence of the test procedure, the 11 + 11 samples are irradiated in 2 runs of 1000Gy(Si) each, up to a total of 2000Gy(Si).

Step	Description	Note
1	Initial electrical characterization (DC and RF measurements)	In Saphyrion laboratory prior shipment to ESTEC.
2	Start continuous data-log (DC measurements)	
3	1000Gy(Si) irradiation, window 2 (low dose rate)	
4	1000Gy(Si) irradiation, window 1 (high dose rate)	
5	Stop continuous data-log (DC measurements)	
6	Final electrical characterization (DC and RF measurements)	In Saphyrion laboratory after shipment from ESTEC in dry-ice.
7	168h Hot temperature annealing – T = 80°C	Performed only if final characterization shows parameters changes.
8	Post annealing electrical characterization.	

Table 1: Irradiation and electrical characterization test plan.

The test performed before and after irradiation (initial and final electrical measurements) are listed in Sections 6.1.1 and 7.1.1 for the SY1007AS and the SY1017AS respectively. During irradiation selected parameters are monitored and logged. Analogue parameters (voltages and currents) are measured with the SM314 interface board, and read back and logged on a computer by the SY10xxTester application. The analogue inputs are sampled every 2.2ms by the SM314 and the average of 512 samples is logged each 60s. The measured values are not allowed to drift more than 10% of the initial value. If a drift $>$10% is measured it will be flagged as an error. The selected parameters are shown in Table 10 (Section 6.2.1) for the SY1007AS device and in Table 17 (Section 7.2.1) for the SY1017AS device.

5.3 Test Campaign Details

The irradiation was started on the 10th of July 2020 at 16:08 at the ESTEC CO-60 facility. Table 3 shows the test runs in detail, the data are taken from the radiation test runs summary report from ESA [7]. The following two tables show the details of the irradiation test sessions for absorbed dose in Silicon (Si): Table 2 shows the values measured by the dosimeter positioned at the unbiased DUTs, while Table 3 shows the values measured by the dosimeter positioned at the biased DUTs.

Irrad. Run	Start Date	Start Time	Stop Date	Stop Time	TID [Rad]	Cumulative TID [Rad]	Dose rate [Gy/h]
1	10.07.2020	16:08:58	10.07.2020	17:10:09	317.26	317.26	3.11
2	10.07.2020	17:50:19	15.07.2020	16:57:57	39727.52	40044.78	3.34
3	15.07.2020	18:34:29	22.07.2020	09:44:47	53080.78	93125.56	3.34
4	22.07.2020	10:51:27	27.07.2020	10:10:20	107041.60	200167.16	8.97

Table 2: Irradiation dose rate and test campaign for the unbiased DUTs.

Irrad. Run	Start Date	Start Time	Stop Date	Stop Time	TID [Rad]	Cumulative TID [Rad]	Dose rate [Gy/h]
1	10-07-2020	16:08:58	10-07-2020	17:10:09	339.00	339.00	3.32
2	10-07-2020	17:50:19	15-07-2020	16:57:57	43175.84	43514.84	3.62
3	15-07-2020	18:34:29	22-07-2020	09:44:47	57624.66	101139.50	3.62
4	22-07-2020	10:51:27	27-07-2020	10:10:20	113776.60	214916.10	9.54

Table 3: Irradiation dose rate and test campaign for the biased DUTs.

5.4 Dry Ice Delivery

The complete electrical characterisation, which includes measurements of sensitive DC and RF parameters, has been executed in Saphyrion laboratory before and after irradiation.

Figure 12: Photos of the dry-ice shipment and temperature measurement inside the box.

Post-radiation tests must be done within *2 hours* after the radiation exposure according to the ESCC 22900 standard. In order to comply with this condition the whole test fixture with the DUTs was shipped *under dry-ice* with a 1 day shipment from ESA ESTEC to Sapyhrion in Switzerland. The box was filled with 24kg of dry-ice (for an estimated duration of 3 days). The package was sent on the *27th of July* and received on the *28th of July* at *11:00am*. Figure 12 shows the received box when it has been opened to initiate the post test session on the *28th of July* at *13:30am*. The internal temperature was $-71.9°$C.

6 SY1007AS Test Report

Twelve SY1007AS DUTs have been serialized as shown in the following Table 4. SY1007AS DUTs number *TB-RF12* is a spare board that has not been irradiated.

Test board name	Acronym	Test board name	Acronym
Biased		Unbiased	
SY1007A_W7_40412A_01	TB-RF01	SY1007A_W7_40412A_07	TB-RF07
SY1007A_W7_40412A_02	TB-RF02	SY1007A_W7_40412A_08	TB-RF08
SY1007A_W7_40412A_03	TB-RF03	SY1007A_W7_40412A_09	TB-RF09
SY1007A_W7_40412A_04	TB-RF04	SY1007A_W7_40412A_10	TB-RF10
SY1007A_W7_40412A_05	TB-RF05	SY1007A_W7_40412A_11	TB-RF11
SY1007A_W7_40412A_06	TB-RF06	SY1007A_W7_40412A_12	TB-RF12

Table 4: SY1007AS test board serialization naming.

6.1 Tests Before and After Irradiation

The SY1007AS DUTs have been characterized in Saphyrion's lab *before* and *after* the irradiation tests in order to spot possible parametric variations that could originate from irradiation damages.

6.1.1 Tests Performed and Conditions

A set of tests that are indicative of parametric variations and that can be done using a single configuration of the test boards (such that modifications and soldering work are avoided) were performed before and after irradiation. The following list outlines the tests performed:

- Current consumption: I(AVDD), I(DVDD).
- Band-gap reference and PLL voltages.
- RF-VCO and IF-VCO phase noise.
- LNA gain and noise figure.
- RF-mixer gain and noise figure.
- IF gain versus AGCI voltage.
- I/Q output amplitude and phase deviation.

The conditions for these tests are the following (Table 5).

Parameter	Value
AVDD, DVDD voltages	3.0V unless noted otherwise
Temperature	Room, ≈25°C
Reference clock frequency	f(RCP) = 4MHz
RF-PLL divider ratio	94
RF-PLL LO frequency	1504MHz
IF-PLL divider ratio	47
IF-PLL LO frequency	188MHz

Table 5: Conditions for the pre and post irradiation tests.

6.1.2 Current Consumption, Band-Gap and PLL Voltages

Current consumption measurements were made at AVDD = 3.0V, DVDD = 3.0V, and f(RCP) = 4.0MHz.

Parameter	TB-RF01		TB-RF02		TB-RF03		TB-RF04		Unit
	Pre	Post	Pre	Post	Pre	Post	Pre	Post	
I(AVDD)	16806.7	16875.5	17195.0	17252.2	16484.6	16547.8	16658.1	16713.1	μA
I(DVDD)	262.9	445.5	268.2	469.9	268.0	478.5	269.1	419.6	μA
VBG	1127.9	1128.1	1135.8	1134.7	1121.8	1121.4	1126.6	1126.3	mV
VB	1843.5	1843.7	1862.8	1861.2	1831.6	1831.1	1834.4	1834.0	mV
RF-PLL	1023.4	1025.3	1025.3	1025.8	1022.7	1025.1	1019.4	1020.9	mV
IF-PLL	1016.6	1016.6	1032.1	1031.2	1016.6	1016.3	1023.4	1022.7	mV
Parameter	TB-RF05		TB-RF06		TB-RF07		TB-RF08		Unit
	Pre	Post	Pre	Post	Pre	Post	Pre	Post	
I(AVDD)	16417.1	16467.1	16214.5	16283.3	17029.7	17201.4	16961.4	17093.1	μA
I(DVDD)	263.5	411.8	261.9	451.2	269.1	272.9	269.1	272.9	μA
VBG	1119.0	1118.9	1118.9	1119.0	1131.9	1131.7	1122.0	1123.5	mV
VB	1834.3	1833.8	1830.9	1830.9	1852.1	1851.7	1834.2	1836.4	mV
RF-PLL	1023.6	1025.2	1028.9	1031.0	1038.5	1040.5	1057.3	1060.8	mV
IF-PLL	1016.5	1015.9	1016.4	1016.1	1029.7	1031.0	1048.1	1050.6	mV
Parameter	TB-RF09		TB-RF10		TB-RF11		TB-RF12		Unit
	Pre	Post	Pre	Post	Pre	Post	Pre	Post	
I(AVDD)	17268.1	17484.7	16743.1	16878.1	16564.7	16698.1	16726.4	16803.0	μA
I(DVDD)	270.8	276.2	267.5	272.9	270.8	276.2	269.1	271.2	μA
VBG	1132.3	1132.2	1124.5	1125.5	1135.6	1134.9	1128.3	1128.9	mV
VB	1848.2	1847.9	1844.1	1845.7	1860.2	1859.8	1856.1	1856.8	mV
RF-PLL	1039.9	1042.2	1053.5	1057.1	1036.9	1038.8	1057.4	1059.3	mV
IF-PLL	1034.2	1035.5	1048.6	1051.1	1039.8	1039.9	1054.0	1056.2	mV

Table 6: Current consumption, band-gap and PLL voltages, pre and post irradiation.

6.1.3 PLL Phase Noise: Configuration

Phase noise measurements were done at a RF local oscillator frequency = 1504MHz, IF local oscillator frequency = 188MHz and reference frequency = 4MHz, which correspond to divider ratios of 376 for the RF PLL and 47 for the IF PLL. The measurements have been done with a spectrum analyzer Keysight (Agilent) E4404B at frequency offsets 5kHz/10kHz to 1MHz. The reference clock is provided on connector J7 with a function generator Keysight (Agilent) 33250A.

Since no direct VCO output is available on the SY1007AS DUTs, the VCO signals were down-converted to an IF using the DUT's on-chip mixers and a signal generator Keysight (Agilent) E4421B. For the phase noise measurement of the RF-PLL a CW signal at 1680MHz is applied to the RFN-RFP port via connector J3 and transformer T3, thus yielding an IF of 176 MHz. The output power of the signal generator was set to −30dBm to avoid saturation of the on-chip mixer, although this will lead to increased noise and lower resolution of the measurement. For the phase noise measurement of the IF-PLL a CW signal at 183MHz is applied to the IF2 port via connector J2 and transformer T2, thus yielding an IF of 5MHz. The output power of the signal generator was set to −20dBm to avoid saturation of the on-chip IF mixer. The PLL loop filter components used are the following:

- **RF-PLL:** C31 = 1nF, C32 = 10nF, R28 = 560Ω.
- **IF-PLL:** C28 = 1nF, C30 = 10nF, R26 = 560Ω.

Figures 13 to 16 show the RF-PLL phase noise measurement results, while Figures 17 to 20 show the IF-PLL phase noise measurement results, both before and after irradiation for DUTs TB-RF01 to TB-RF12 at +27°C. Green is *before* (pre) and blue is *after* (post) irradiation.

6.1.4 RF PLL: Phase Noise Measurements

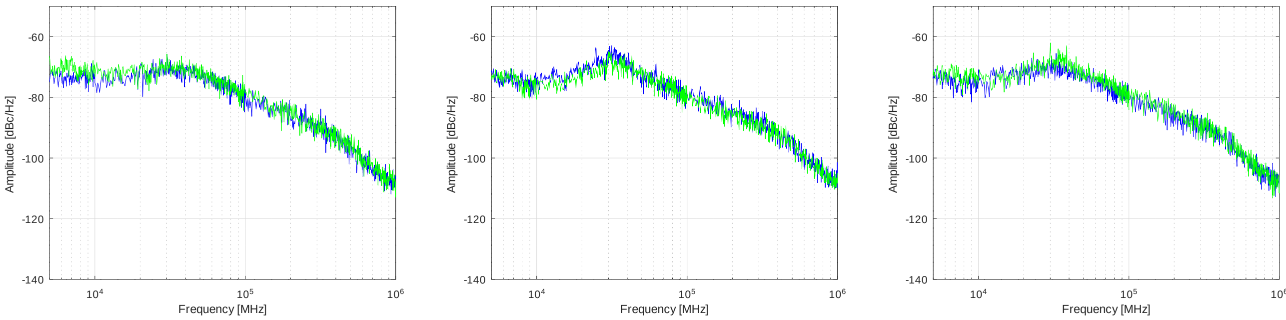


Figure 13: RF-VCO phase noise for TB-RF01 (l), TB-RF02 (c) and TB-RF03 (r).

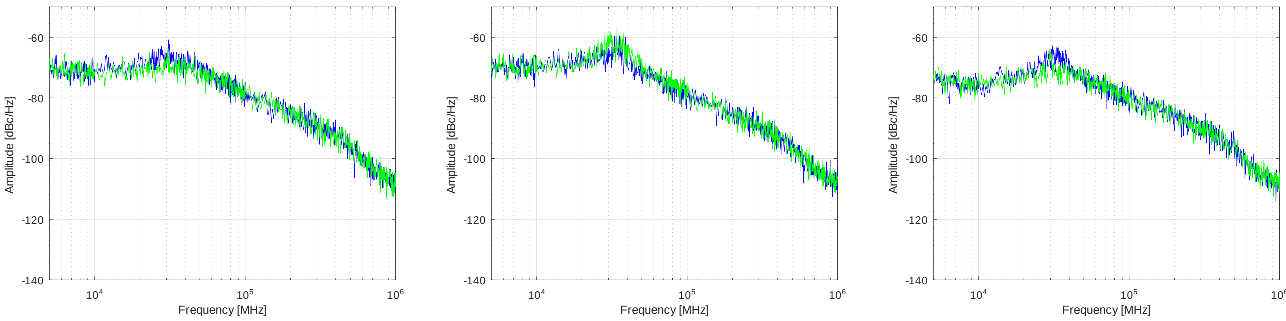


Figure 14: RF-VCO phase noise for TB-RF04 (l), TB-RF05 (c) and TB-RF06 (r).

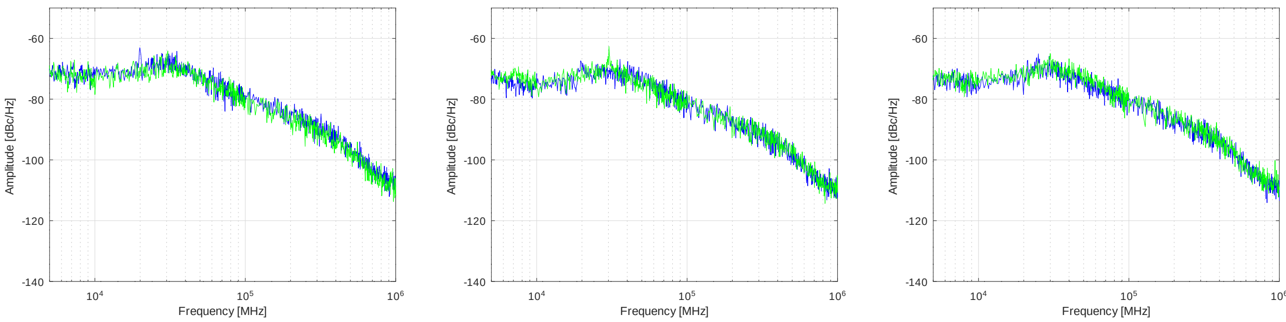


Figure 15: RF-VCO phase noise for TB-RF07 (l), TB-RF08 (c) and TB-RF09 (r).

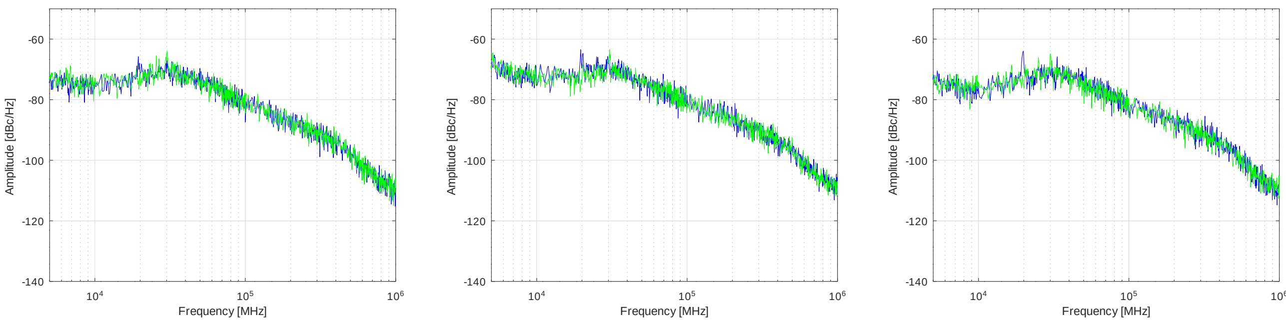


Figure 16: RF-VCO phase noise for TB-RF10 (l), TB-RF11 (c) and TB-RF12 (r).

6.1.5 IF PLL: Phase Noise Measurements

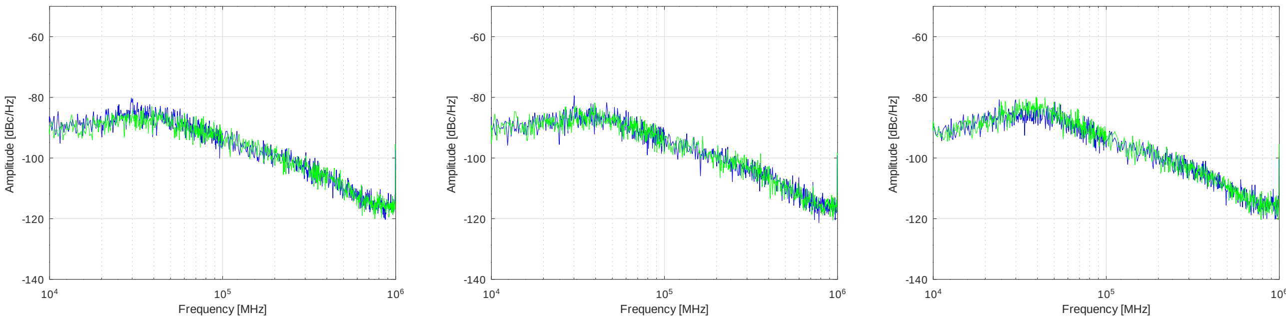


Figure 17: IF-VCO phase noise for TB-RF01 (l), TB-RF02 (c) and TB-RF03 (r).

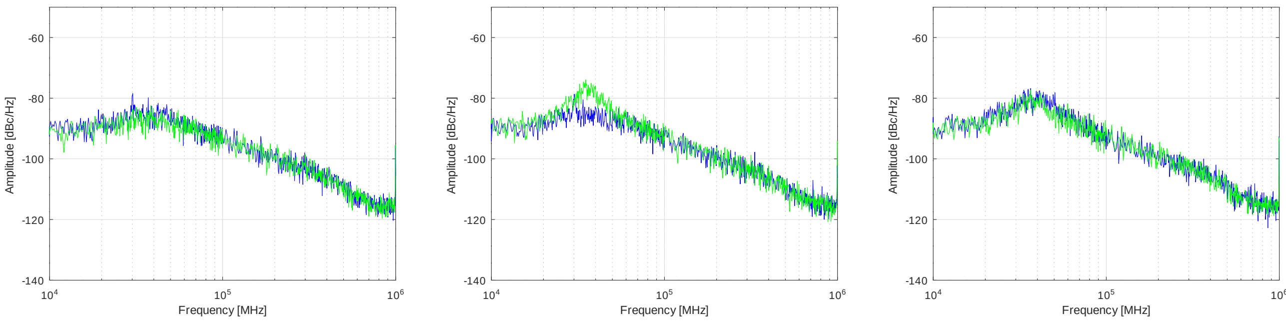


Figure 18: IF-VCO phase noise for TB-RF04 (l), TB-RF05 (c) and TB-RF06 (r).

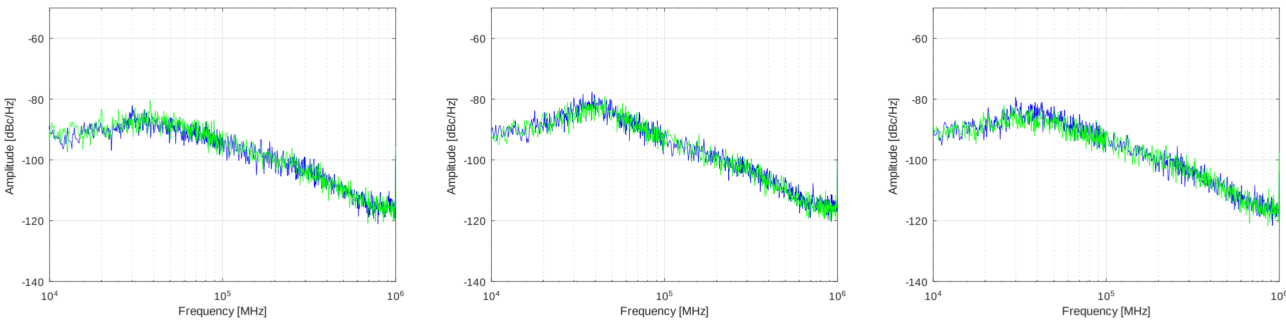


Figure 19: IF-VCO phase noise for TB-RF07 (l), TB-RF08 (c) and TB-RF09 (r).

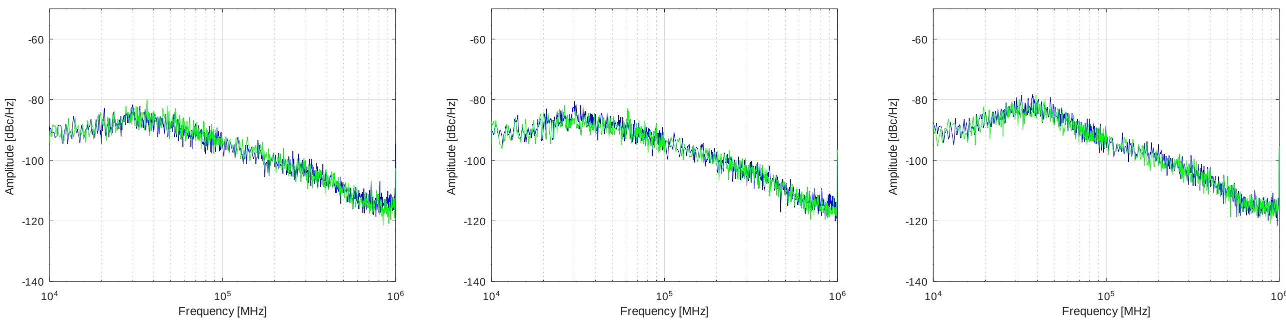


Figure 20: IF-VCO phase noise for TB-RF10 (l), TB-RF11 (c) and TB-RF12 (r).

6.1.6 LNA Gain and Noise Figure

The LNA requires matching networks at both its input and output, the components involved are L6-C20-R19 (input) and L3-L5 (output). The values mounted are the the same required by the SY1007, i.e.:

- **Input (NM):** L6 = 4.7nH, R19 and C20 not fitted.
- **Output:** L3 = 4.7nH, L5 = 6.8nH.

LNA gain and noise figure are measured at a temperature of $+27°$C and AVDD = 3.0V. The measurement is done with the noise figure analyzer Keysight (Agilent) N8973A and the noise source Keysight (Agilent) 346A. Table 7 shows the results at 1.5GHz and the minimum noise figure before and after irradiation. The minimum noise figure was obtained at 1.05GHz for all devices.

DUTs	Before irradiation Gain (1.50GHz)	NF (1.50GHz)	NFmin (1.05GHz)	After irradiation Gain (1.50GHz)	NF (1.50GHz)	NFmin (1.05GHz)	Unit
TB-RF01	20.05	2.18	1.46	19.52	2.16	1.56	dB
TB-RF02	20.70	2.15	1.47	19.92	2.17	1.50	dB
TB-RF03	19.95	2.18	1.48	19.60	2.21	1.47	dB
TB-RF04	19.87	2.16	1.56	19.63	2.32	1.57	dB
TB-RF05	20.07	2.00	1.43	19.54	2.23	1.52	dB
TB-RF06	19.57	2.14	1.43	19.43	2.21	1.52	dB
TB-RF07	20.20	2.20	1.46	19.75	2.22	1.58	dB
TB-RF08	20.53	2.15	1.41	20.05	2.33	1.65	dB
TB-RF09	21.12	2.20	1.47	20.50	2.41	1.60	dB
TB-RF10	20.12	2.15	1.46	19.72	2.31	1.60	dB
TB-RF11	19.25	2.23	1.52	18.92	2.30	1.60	dB
TB-RF12	19.77	2.17	1.47	19.60	2.21	1.60	dB

Table 7: Gain and noise figure of the LNA for TB-RF01 to TB-RF12.

6.1.7 RF-Mixer Gain and Noise Figure

The gain and noise figure of the RF mixer are measured as DSB values from port RFN-RFP to port IF1N-IF1P – i.e. including the 1st IF amp stage. The output of the mixer (port MIXN-MIXP) is loaded with a parallel LC resonator, L = 36nH, C = 18pF. The test is done at temperature = $+27°$C and AVDD = 2.4V.

The measurement is done at an IF frequency span between 150MHz and 200MHz, the gain and noise figure values are taken at 185MHz, with the noise figure analyzer Keysight (Agilent) N8973A and the noise source Keysight (Agilent) 346A. Since no image filter is used the measurements are DSB. In order to calculate the SSB values it is sufficient to subtract 3dB from the gain measurement and add 3dB to the noise figure measurement.

The insertion losses of the RF components that should be used to calculate the actual gain and noise figure out of the numbers shown in the tables, are:

- Cable loss = 0.3dB.
- Balun loss = 0.5dB.
- Matching transformer insertion loss = 1dB.
- Impedance conversion voltage loss = 9dB.
- Mixer gain loss due to loading = 8dB.
- IF filter LC loss = 1dB.

In order to calculate the actual SSB gain and noise figure of the RF-mixer from the DSB numbers indicated by the instrument therefore **16.8dB** shall be added to the gain and **2.2dB** shall be added to the NF.

Table 8 shows the measurement results before and after irradiation. The (uncompensated) DSB measurements as indicated by the instrument are shown in the DSB rows, while the actual calculated SSB values – already compensated – are shown in the SSB rows. All measurements are affected by some uncertainty due to the low ENR (about 5dB) of the 346A noise source, which leads to low SNR measurements.

Parameter	Pre	Post	Pre	Post	Pre	Post	Pre	Post	Unit	Note
	TB-RF01		**TB-RF02**		**TB-RF03**		**TB-RF04**			
DSB Gain	9.1	8.1	9.2	8.3	8.8	7.8	9.1	8.2	dB	Indicated by the instrument.
DSB NF	6.9	7.7	6.9	7.7	7.1	7.9	7.0	7.9	dB	
SSB Gain	25.9	24.9	26.0	25.0	25.6	24.6	25.9	25.0	dB	Calculated from DSB values.
SSB NF	9.1	9.9	9.1	9.9	9.3	10.1	9.2	10.1	dB	
	TB-RF05		**TB-RF06**		**TB-RF07**		**TB-RF08**			
DSB Gain	8.9	7.8	8.7	7.8	8.9	8.0	8.6	8.0	dB	Indicated by the instrument.
DSB NF	6.9	7.8	7.0	7.7	7.0	8.0	7.1	7.6	dB	
SSB Gain	25.0	24.6	25.5	24.6	25.7	24.8	25.4	24.8	dB	Calculated from DSB values.
SSB NF	9.1	10.0	9.2	9.9	9.2	10.2	9.3	9.8	dB	
	TB-RF09		**TB-RF10**		**TB-RF11**		**TB-RF12**			
DSB Gain	8.9	7.9	8.9	8.0	8.8	8.0	8.8	8.2	dB	Indicated by the instrument.
DSB Gain	6.9	7.9	6.9	8.0	6.9	7.8	7.0	7.7	dB	
SSB Gain	25.7	24.7	25.7	24.8	25.7	24.8	25.6	25.0	dB	Calculated from DSB values.
SSB Gain	9.1	10.1	9.1	10.2	9.1	10.0	9.2	9.9	dB	

Table 8: Measured DSB and calculated SSB gain and noise figure of the RF-mixer.

6.1.8 IF Gain vs. AGCI Voltage

In this test the 3-stage voltage controlled variable gain amplifier is measured. A CW signal at 187MHz is applied to the IF2 port via connector J2 and transformer T2, and the output amplitude at 1MHz is measured with a Keysight (Agilent) 54621 oscilloscope on capacitors C15, C16, C19 and C21. The voltage on pin AGCI is varied from 1.2V to 2.0V and the amplitude of the CW signal is adjusted to keep the output differential amplitude at 350mVpp. The resulting gain is then calculated.

Figures 21 to 24 show the measurement results *before and after irradiation* at $+27°$C for DUTs TB-RF01 to TB-RF12. Blue is *before* (pre) and green is *after* (post) irradiation.

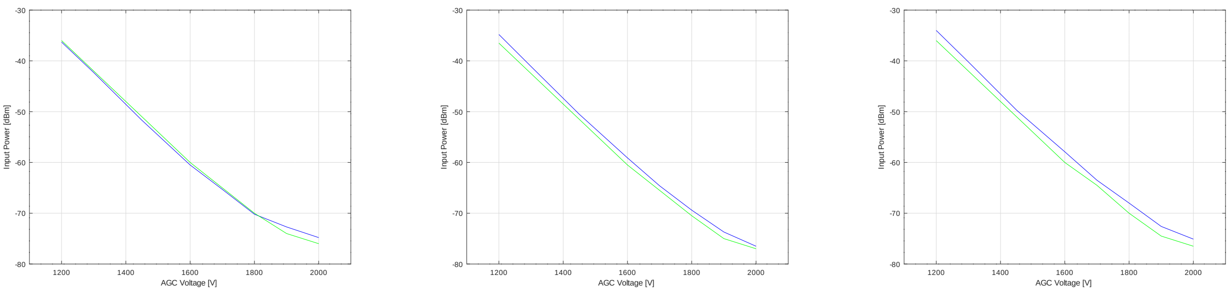


Figure 21: IF gain vs. AGCI control voltage for TB-RF01 (l), TB-RF02 (c) and TB-RF03 (r).

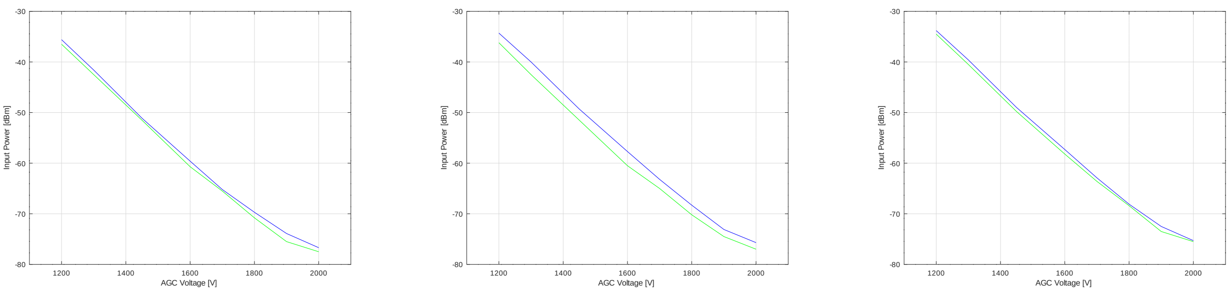


Figure 22: IF gain vs. AGCI control voltage for TB-RF04 (l), TB-RF05 (c) and TB-RF06 (r).

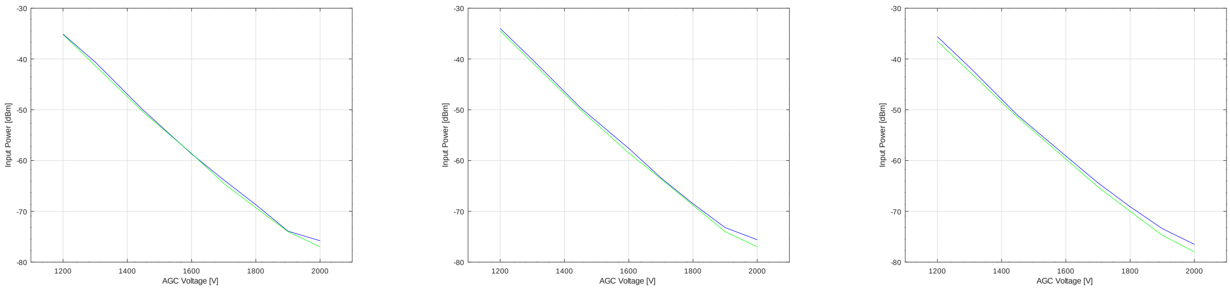


Figure 23: IF gain vs. AGCI control voltage for TB-RF07 (l), TB-RF08 (c) and TB-RF09 (r).

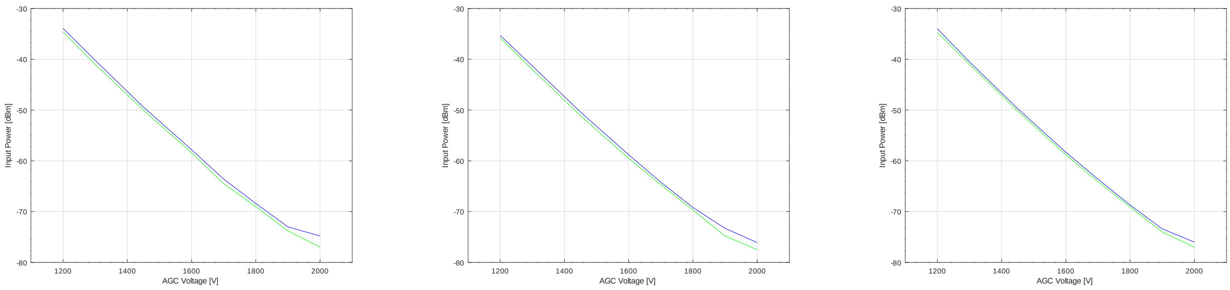


Figure 24: IF gain vs. AGCI control voltage for TB-RF10 (l), TB-RF11 (c) and TB-RF12 (r).

6.1.9 I/Q Output Amplitude and Phase Deviation

In this test the amplitude and phase mismatch between I and Q paths is measured. A CW signal at 187MHz is applied to the IF2 port via connector J2 and transformer T2, and the 1MHz output amplitude is measured with a Keysight (Agilent) 54621 oscilloscope on C15, C16, C19 and C21. The voltage on pin AGCI is set to 1.4V and the amplitude of the CW is adjusted to keep the output differential amplitude at 350mVpp.

Table 9 shows the measured results. The resolution of the phase measurement, imposed by the Keysight 54621 oscilloscope, is 0.71°.

DUT	Phase Pre		Amplitude Pre		Phase Post		Amplitude Post	
	P port	N port	P port	N port	P port	N port	P port	N port
TB-RF01	90.72°	90.00°	<3mV	<3mV	90.00°	90.72°	<3mV	<3mV
TB-RF02	89.28°	88.57°	<3mV	<3mV	89.28°	89.28°	<3mV	<3mV
TB-RF03	92.16°	91.43°	<3mV	<3mV	92.16°	92.16°	<3mV	<3mV
TB-RF04	90.72°	90.00°	<3mV	<3mV	90.72°	90.72°	<3mV	<3mV
TB-RF05	90.72°	90.00°	<3mV	<3mV	90.72°	90.72°	<3mV	<3mV
TB-RF06	92.16°	91.43°	<3mV	<3mV	92.16°	91.43°	<3mV	<3mV
TB-RF07	92.16°	91.43°	<3mV	<3mV	92.16°	91.43°	<3mV	<3mV
TB-RF08	91.44°	90.71°	<3mV	<3mV	90.72°	90.72°	<3mV	<3mV
TB-RF09	92.16°	91.43°	<3mV	<3mV	92.16°	91.43°	<3mV	<3mV
TB-RF10	90.72°	90.00°	<3mV	<3mV	90.72°	90.00°	<3mV	<3mV
TB-RF11	92.16°	91.43°	<3mV	<3mV	92.16°	91.43°	<3mV	<3mV
TB-RF12	90.72°	90.00°	<3mV	<3mV	90.72°	90.00°	<3mV	<3mV

Table 9: Amplitude and phase mismatch on DUTs TB-RF01 to TB-RF12.

- **Test Results:** All SY1007AS DUTs operate properly with no significant parametric drifts before and after irradiation, except for an increase in I(DVDD). The minor deviations seen in the various measurements are due to either normal measurement uncertainty or temperature effects rather than absorbed dose.

  These devices have therefore demonstrated *no sensitivity* to irradiation up to **1000Gy(Si)** and remained operative up to **2000Gy(Si)**, although an increase in I(DVDD) has been found.

6.2 Tests During Irradiation

The SY1007AS DUTs have been tested up to a TID = 2kGy(Si) in 2 separate runs of 1kGy(Si) each, one at high dose rate and one at low dose rate to test ELDRS effects. The conditions for these tests are shown in Table 1, while the details of the tests are shown in Tables 2 and 3 (Section 5).

6.2.1 Irradiation Test Execution

The SY1007AS DUT needs to be powered up, then initialized. Once the SY1007AS is ready, irradiation is started and measurements are made for the whole irradiation time. This is described in Table 10, where 'S' means a set-up and 'M' means a measurement to be performed.

	Description	Expected value
S	Set power supply to 3.0V.	
S	Set clock frequency to 4MHz.	
S	Load state 2 into power mode register (PLL-ON, turns bias circuitry and PLL on).	
S	Load value 47 into IF register.	
S	Load value 94 into RF register.	
M	Measure current consumption	I(AVDD) $<$ 30mA
M	Measure current consumption	I(DVDD) $<$ 1mA
M	Measure VBG and VB	1.13V and 1.84V
M	Measure RF PLL output	between 0.9-1.15V
M	Measure IF PLL output	between 0.9-1.15V

Table 10: Setup of the SY1007AS for the irradiation tests.

6.2.2 Data Logged During Irradiation

During the irradiation period data is logged. Several parameters have been selected as event indicators, these are shown in Table 11 and comprise both analog parameters and DUT register status. Data is logged once per second.

Register	Measurement or Setting
SM314 Registers	
ANALOG_OUT1_CURRENT	IDVDD [μA]
ANALOG_OUT1_VOLTAGE	DVDD [mV]
ANALOG_OUT2_CURRENT	IAVDD [μA]
ANALOG_OUT2_VOLTAGE	AVDD [mV]
ANALOG_IN1_AD_VALUE	VB [mV]
ANALOG_IN2_AD_VALUE	VBG [mV]
ANALOG_IN3_AD_VALUE	RF-PLL Voltage [mV]
ANALOG_IN4_AD_VALUE	IF-PLL Voltage [mV]
ANALOG_OUT3_VOLTAGE	AGC [mV]
SY1007AS Registers	
Power modes	Pwr-Modes = 2
RF-PLL main divider	RF-PLL = 94
IF-PLL main divider	IF-PLL = 47

Table 11: Data logged for SY1007AS DUTs during irradiation.

These parameters were selected because they tend to be the most sensitive parameters against irradiation. In particular the band-gap reference, which uses bipolar transistors in a circuit with relatively high gain and is used to bias all circuits in the DUTs, is a sensitive indicator of degradation, especially ELDRS if present. A drift of the band-gap reference would be reflected on the performances of the whole DUT.

6.2.3 Parametric Drifts

The purpose of these tests is to find any parametric drifts that may occur under irradiation. These are DC measurements and were made according to the conditions given in Table 10. During the irradiation period the following parameters were measured and logged (Table 11):

- **SY1007AS:** I(AVDD), I(DVDD), VBG, VB, V(RF-PLL), V(IF-PLL).

The following traces show the measured parameters over the 0Gy to 2.2kGy(Si) irradiation range.

I(AVDD): Figures 25 and 26 show AVDD current consumption for the SY1007AS devices TB-RF01 to TB-RF06.

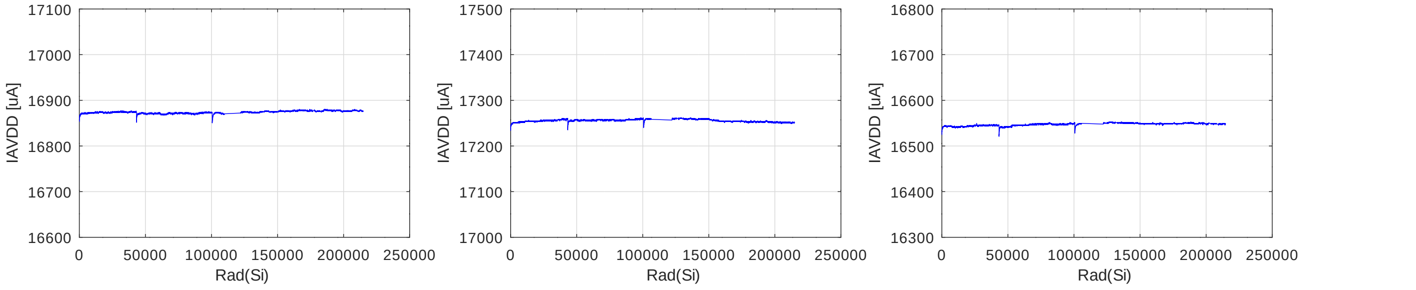


Figure 25: AVDD current consumption during irradiation: TB-RF01 (l), TB-RF02 (c) and TB-RF03 (r).

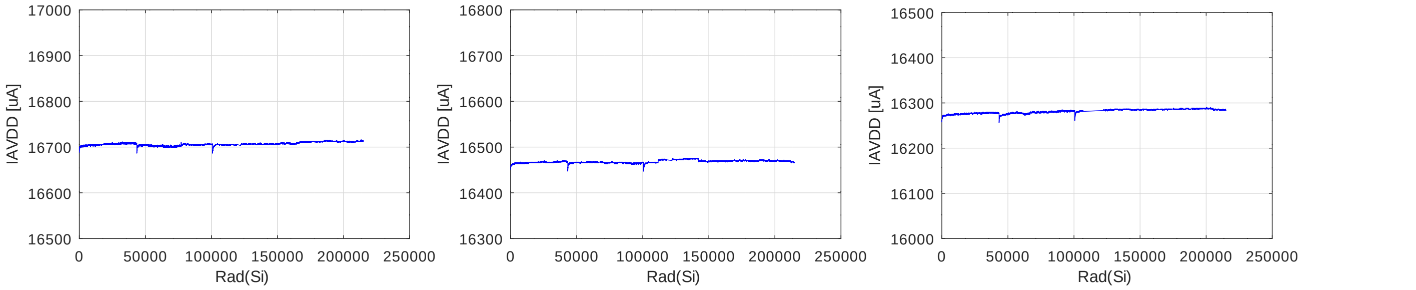


Figure 26: AVDD current consumption during irradiation: TB-RF04 (l), TB-RF05 (c) and TB-RF06 (r).

AVDD current consumption remains *constant* over the whole irradiation range, which indicates *no sensitivity* to irradiation. The 3 visible jumps correspond to the irradiation step from run 2 to 3 and from run 3 to 4. The I(AVDD) current measurements show quantization noise due to the 1.67μA resolution of the AD-converters of the SM314 boards.

I(DVDD): Figures 27 and 28 show DVDD current consumption for the SY1007AS devices TB-RF01 to TB-RF06.

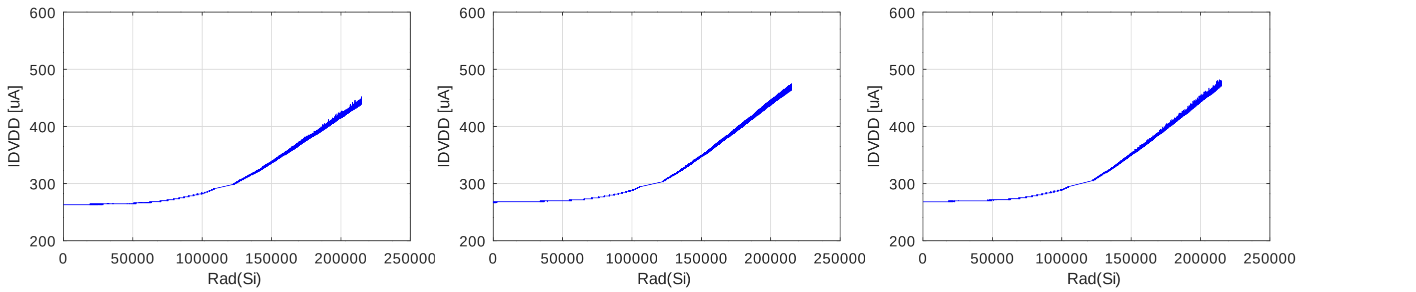


Figure 27: DVDD current consumption during irradiation: TB-RF01 (l), TB-RF02 (c) and TB-RF03 (r).

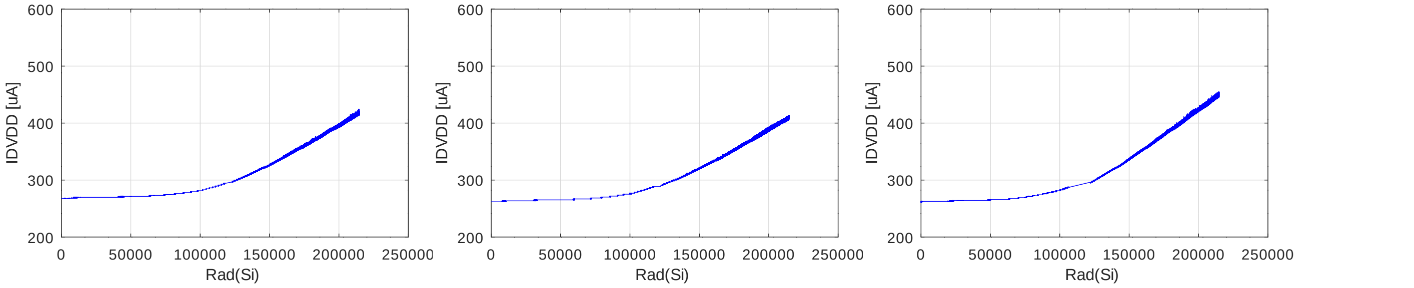


Figure 28: DVDD current consumption during irradiation:: TB-RF04 (l), TB-RF05 (c) and TB-RF06 (r).

DVDD current consumption remains *substantially constant* over the first 1kGy(Si) irradiation session, then *increases linearly* until radiation is stopped. The DVDD current increase is *bias dependent* and is confirmed also by the post-irradiation tests shown in Table 6. Unbiased irradiated devices show no DVDD current increase. The I(DVDD) current measurements show quantization noise due to the 1.67μA resolution of the AD-converters of the SM314 boards.

VBG: Figures 29 and 30 show the band-gap reference (VBG) voltages for the SY1007AS devices TB-RF01 to TB-RF06.

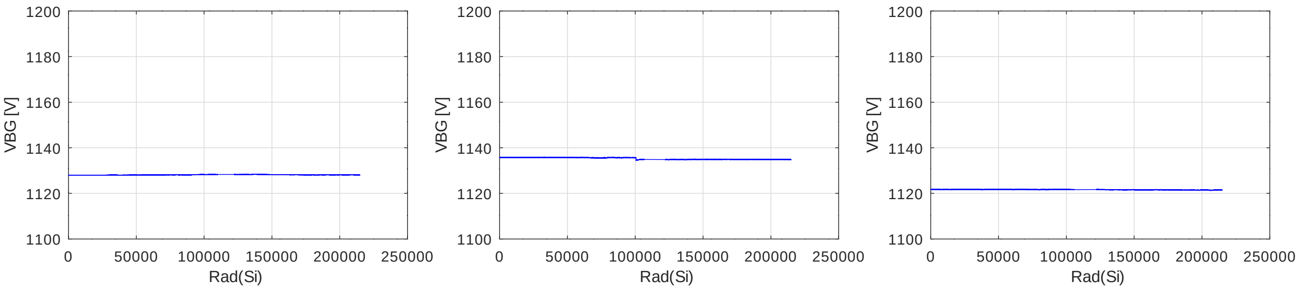


Figure 29: VBG voltage during irradiation: TB-RF01 (l), TB-RF02 (c) and TB-RF03 (r).

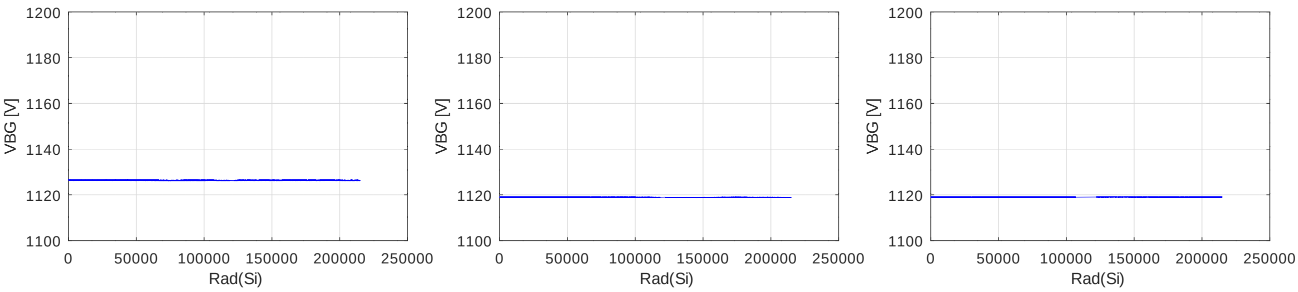


Figure 30: VBG voltage during irradiation: TB-RF04 (l), TB-RF05 (c) and TB-RF06 (r).

The VBG voltage is *essentially constant* for all DUTs, which indicates *no sensitivity* to irradiation.

VB: Figures 31 and 32 show the LDO regulator voltage for the SY1007AS devices TB-RF01 to TB-RF06.

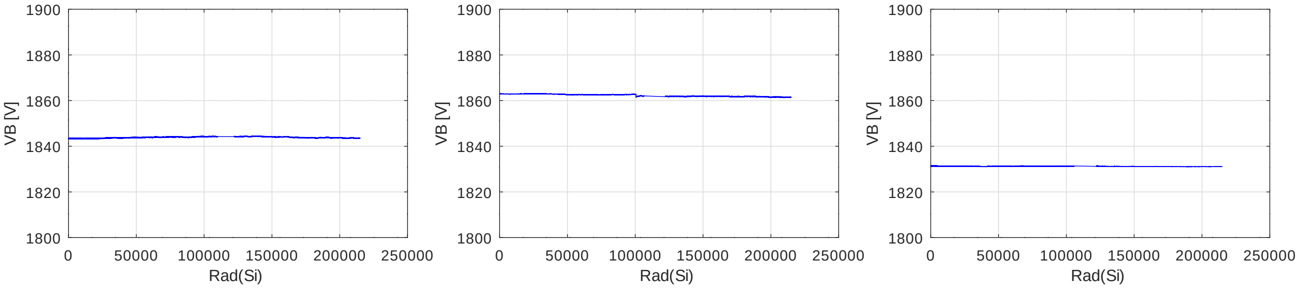


Figure 31: VB voltage during irradiation: TB-RF01 (l), TB-RF02 (c) and TB-RF03 (r).

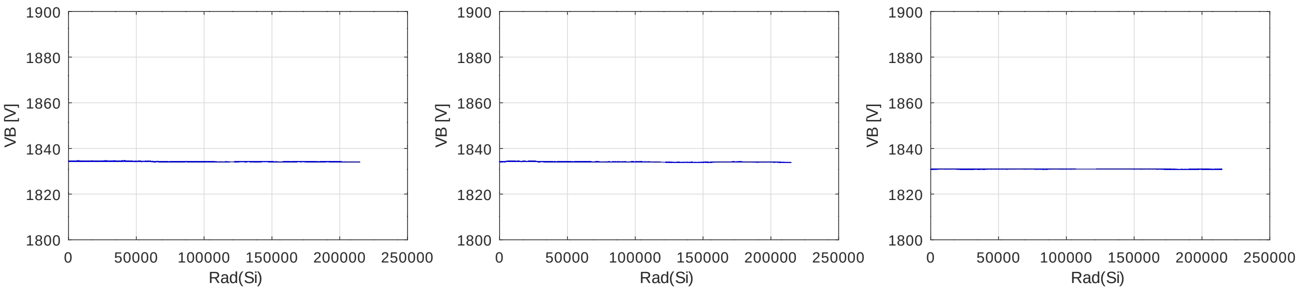


Figure 32: VB voltage during irradiation: TB-RF04 (l), TB-RF05 (c) and TB-RF06 (r).

Also the VB voltage is *essentially constant* for all DUTs, which indicates *no sensitivity* to irradiation.

V(RF-PLL): Figures 33 and 34 show the RF PLL loop filter voltages for the SY1007AS devices TB-RF01 to TB-RF06.

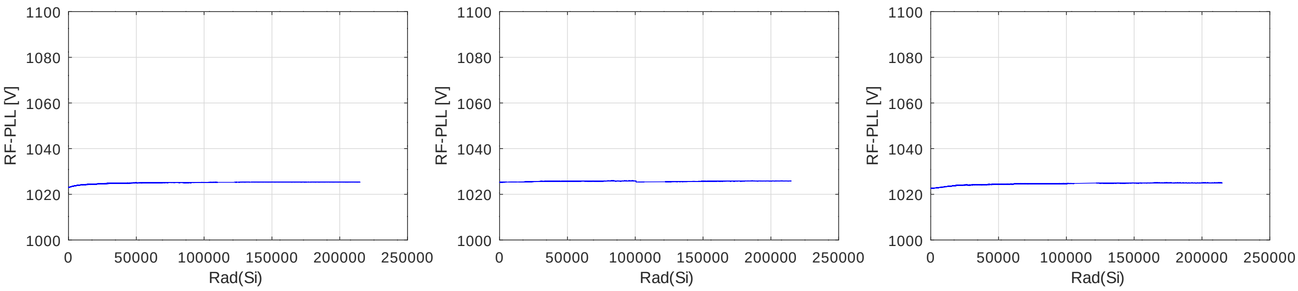


Figure 33: RF-PLL voltage during irradiation: TB-RF01 (l), TB-RF02 (c) and TB-RF03 (r).

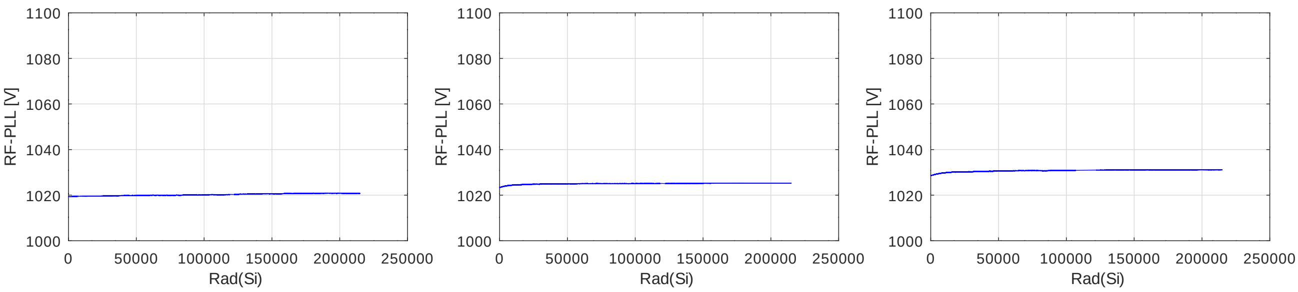


Figure 34: RF-PLL voltage during irradiation: TB-RF04 (l), TB-RF05 (c) and TB-RF06 (r).

V(IF-PLL): Figures 35 and 36 show the IF PLL loop filter voltages for the SY1007AS devices TB-RF01 to TB-RF06.

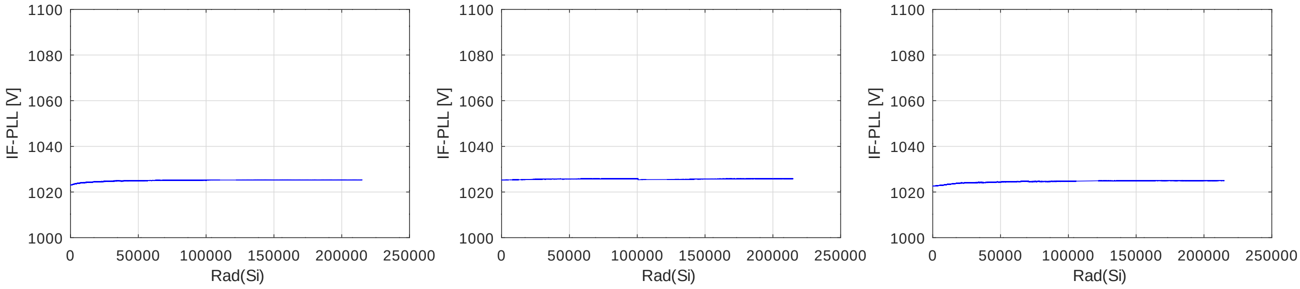


Figure 35: IF-PLL voltage during irradiation: TB-RF01 (l), TB-RF02 (c) and TB-RF03 (r).

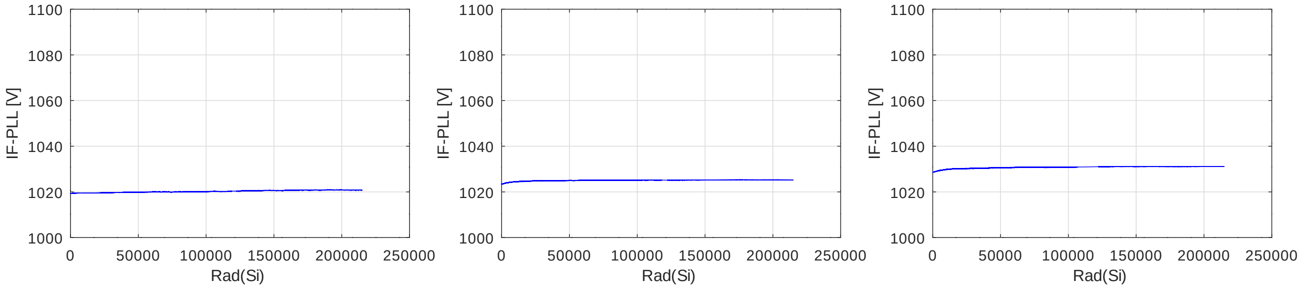


Figure 36: IF-PLL voltage during irradiation: TB-RF04 (l), TB-RF05 (c) and TB-RF06 (r).

Both RF and IF PLL voltages are *essentially constant* for all DUTs, which indicates *no sensitivity* to irradiation.

- **Test Results:** All SY1007AS DUTs operate properly with no significant parametric drifts during irradiation. The monitored parameters are stable, except for I(DVDD), which increases linearly above 1kGy(Si). The DVDD supply current increase however caused no malfunctions to the DUTs, which continued to operate properly. The minor deviations seen in the various measurements are due to either normal measurement uncertainty or temperature effects rather than absorbed dose.

  These devices have therefore demonstrated *no sensitivity* to irradiation up to **1000Gy(Si)** and remained operative up to **2000Gy(Si)**, although an increase in I(DVDD) has been found.

7 SY1017AS Test Report

Twelve SY1017AS DUTs have been serialized as shown in the following Table 12. SY1017AS DUTs number *TB-AD12* is a spare board that has not been irradiated.

Test board name	Acronym	Test board name	Acronym
Biased		**Unbiased**	
SY1017A_W7_40412B_01	TB-AD01	SY1017A_W7_40412B_07	TB-AD07
SY1017A_W7_40412B_02	TB-AD02	SY1017A_W7_40412B_08	TB-AD08
SY1017A_W7_40412B_03	TB-AD03	SY1017A_W7_40412B_09	TB-AD09
SY1017A_W7_40412B_04	TB-AD04	SY1017A_W7_40412B_10	TB-AD10
SY1017A_W7_40412B_05	TB-AD05	SY1017A_W7_40412B_11	TB-AD11
SY1017A_W7_40412B_06	TB-AD06	SY1017A_W7_40412B_12	TB-AD12

Table 12: SY1017AS test board serialization naming.

7.1 Tests Before and After Irradiation

The SY1017AS DUTs have been characterized in Saphyrion's lab *before* and *after* the irradiation tests in order to spot possible parametric variations that could originate from irradiation damages.

7.1.1 Tests Performed and Conditions

A set of tests that are indicative of parametric variations and that can be done using a single configuration of the test boards (such that modifications and soldering work are avoided) were performed before and after irradiation. The following list outlines the tests performed:

- Current consumption: I(AVDD), I(DVDD).
- DA-converter full-scale (0x00) and PLL voltages.
- VCO phase noise (at large offset).
- VCO frequency range.
- VCO max free-running frequency and frequency range.

The conditions for these tests are the following (Table 13).

Parameter	Value
AVDD, DVDD voltages	3.0V unless noted otherwise
Temperature	Room, $\approx 25^\circ$C
Reference clock frequency	f(FREF) = 4MHz
SCKO frequency band	Low band, 50MHz (SCS = 0)
Reference divider ratio	2 (R2[2:0] = 1)
PLL main divider ratio	25 (PM&PLL = 230)

Table 13: Conditions for the pre and post irradiation tests.

7.1.2 Current Consumption, DA-Converter and PLL Voltages

Current consumption measurements were made at AVDD = 3.0V, DVDD = 3.0V, and f(FREF) = 4.0MHz. Current consumtion on the DVDD power supply is rather unpredictable since it depends on the activity of the outputs of the AD-converters, which is random since their inputs are left open (internally biased).

Parameter	**TB-AD01**		**TB-AD02**		**TB-AD03**		**TB-AD04**		**Unit**
	Pre	Post	Pre	Post	Pre	Post	Pre	Post	
I(AVDD)	8082	8137	8076	8138	8112	8152	8102	8165	μA
I(DVDD)	2889	2991	3602	3022	3953	4083	3537	3018	μA
DAC Voltage (AGCO)	1048	1048	1041	1040	1053	1054	1043	1044	mV
PLL Voltage (VC)	1466	1464	1462	1467	1462	1463	1452	1457	mV
Parameter	**TB-AD05**		**TB-AD06**		**TB-AD07**		**TB-AD08**		**Unit**
	Pre	Post	Pre	Post	Pre	Post	Pre	Post	
I(AVDD)	8121	8182	8045	8107	7876	8042	7907	8049	μA
I(DVDD)	2896	2983	2927	3019	2411	2912	2456	2482	μA
DAC Voltage (AGCO)	1048	1048	1039	1038	1048	1048	1035	1036	mV
PLL Voltage (VC)	1447	1453	1472	1476	1513	1517	1509	1512	mV
Parameter	**TB-AD09**		**TB-AD10**		**TB-AD11**		**TB-AD12**		**Unit**
	Pre	Post	Pre	Post	Pre	Post	Pre	Post	
I(AVDD)	7881	7889	7992	7952	7761	8027	8009	8035	μA
I(DVDD)	1599	2933	2436	2948	2488	2885	1593	3553	μA
DAC Voltage (AGCO)	1045	1044	1040	1040	1044	1045	1036	1038	mV
PLL Voltage (VC)	1510	1512	1491	1488	1480	1476	1467	1462	mV

Table 14: Current consumption, DAC and PLL voltages, pre and post irradiation.

7.1.3 Phase Noise at Large Offsets

Phase noise measurements were done for frequency offsets from 10kHz to 1MHz with a spectrum analyzer Keysight (Agilent) E4404B.

The 4MHz reference clock is provided by a function generator Keysight (Agilent) E33250A on pin FREF, the phase noise is measured on the SCKO output (connector J9) at 50MHz and $+27°$C. Figures 37 to 40 show the phase noise measurement results before and after irradiation for DUTs TB-AD01 to TB-AD12 at $+27°$C. Blue is *before* (pre) and green is *after* (post) irradiation. *No drift* due to irradiation damages is visible, the minor differences are due to normal measurement uncertainty.

Measurements closer to the carrier were not done. Since the purpose of this test is to detect damages due to irradiation and not to characterize the SY1017A devices, such measurements are not needed. Radiation damages would have been detected safely with the measurements done here.

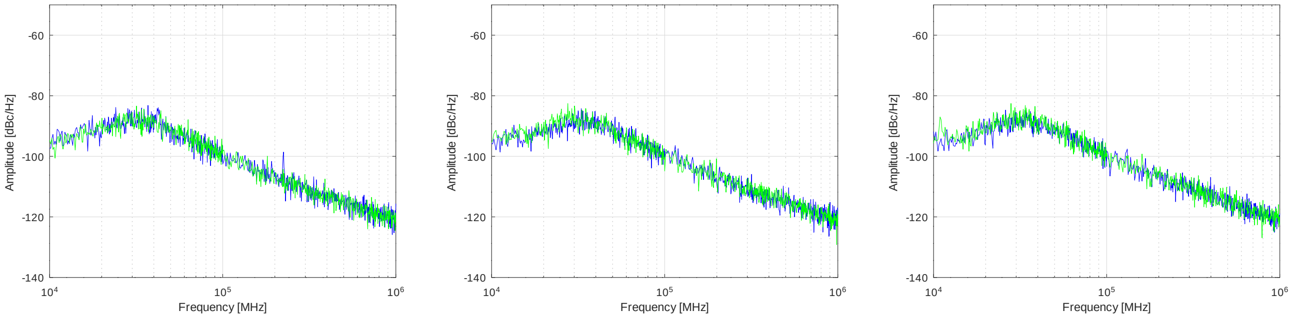


Figure 37: Phase noise at 50MHz for TB-AD01 (l), TB-AD02 (c) and TB-AD03 (r).

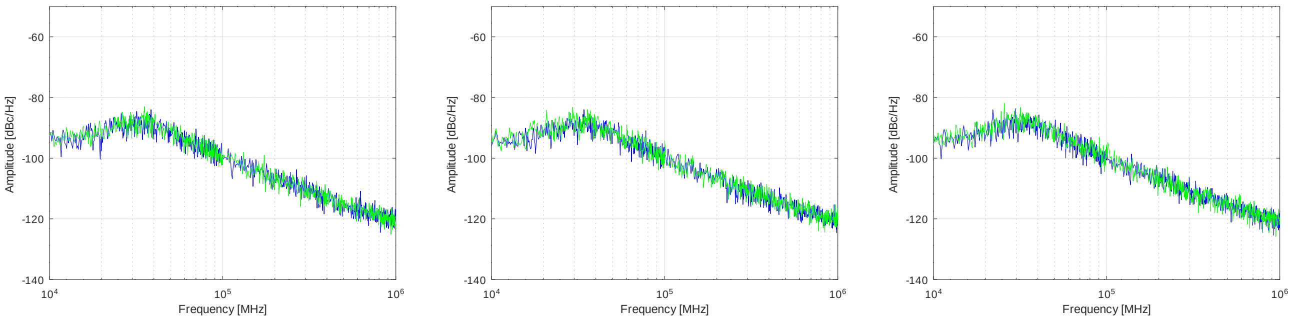


Figure 38: Phase noise at 50MHz for TB-AD04 (l), TB-AD05 (c) and TB-AD06 (r).

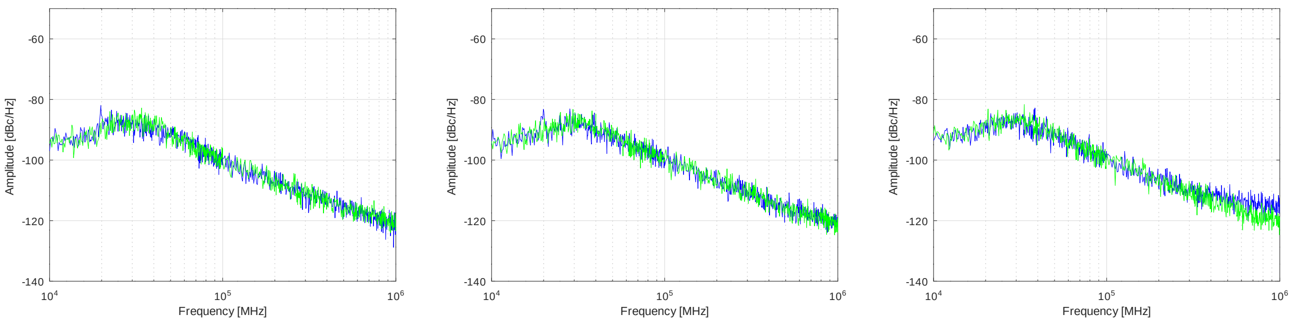


Figure 39: Phase noise at 50MHz for TB-AD07 (l), TB-AD08 (c) and TB-AD09 (r).

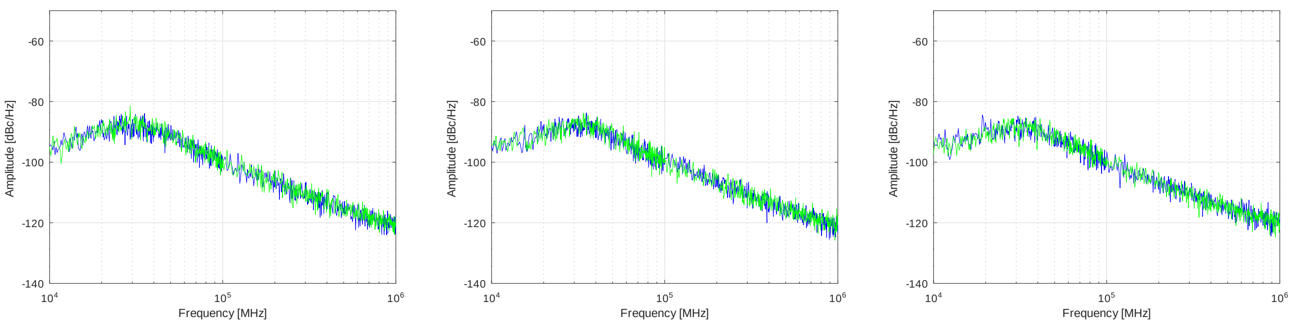


Figure 40: Phase noise at 50MHz for TB-AD10 (l), TB-AD11 (c) and TB-AD12 (r).

7.1.4 VCO Frequency Range

In this test the control voltage of the PLL is measured (connector JP1) while the reference clock frequency (on pin FREF) is varied from ≈0Hz to 10MHz, such that the whole control range of the VCO is covered.

Figures 41 to 44 show the measured VCO frequency vs. PLL voltage for DUTs TB-AD01 to TB-AD12 before and after irradiation. Blue is *before* (pre) and green is *after* (post) irradiation. *No drift* due to irradiation damages is visible in these measurements.

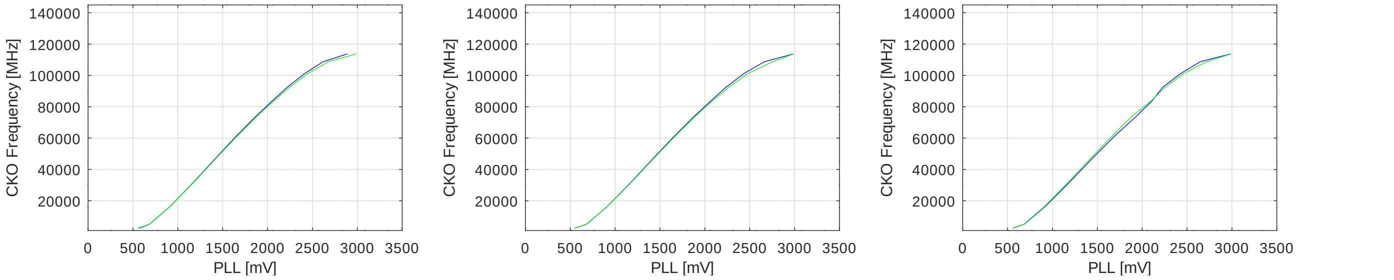


Figure 41: VCO frequency vs. PLL voltage for TB-AD01 (l), TB-AD02 (c) and TB-AD03 (r).

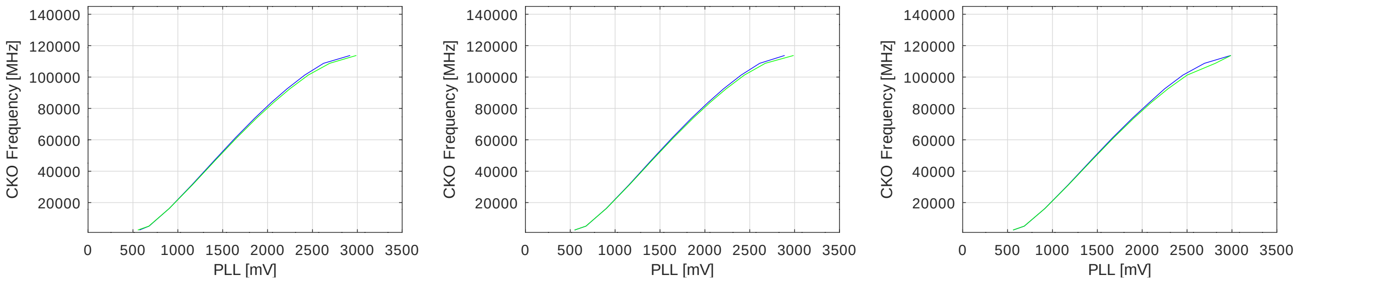


Figure 42: VCO frequency vs. PLL voltage for TB-AD04 (l), TB-AD05 (c) and TB-AD06 (r).

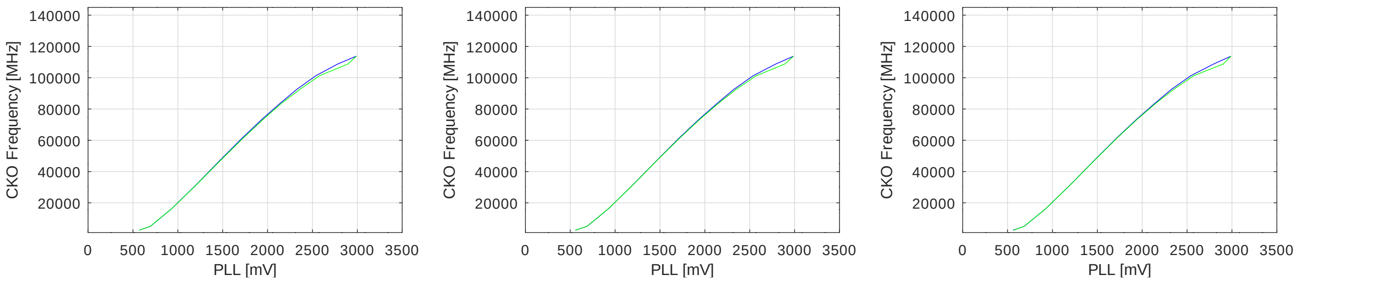


Figure 43: VCO frequency vs. PLL voltage for TB-AD07 (l), TB-AD08 (c) and TB-AD09 (r).

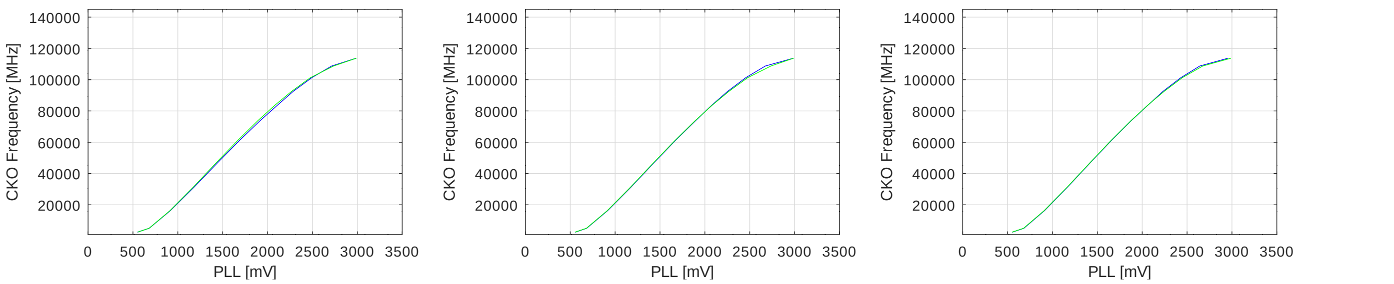


Figure 44: VCO frequency vs. PLL voltage for TB-AD10 (l), TB-AD11 (c) and TB-AD12 (r).

7.1.5 VCO Maximum Frequency (Free Running)

In this test the maximum free-running frequency of the VCO is measured. The measurement is done on the CKO output with a Keysight (Agilent) 53131A frequency counter. To obtain free running conditions without modifying the test boards the reference clock is increased until the PLL loses lock. The configuration of the DUTs is as follows:

- **SCKO frequency band:** low band, 50MHz (SCS = 0).
- **AVDD supply voltage:** 3.6V.

The VCO control voltage VC is basically 3.6V during this test. Table 15 shows the measured frequency on the CKO (row f(CKO)) and the calculated VCO frequency (row f(VCO) = 8x f(CKO)).

Parameter	TB-AD01		TB-AD02		TB-AD03		TB-AD04		Unit
	Pre	Post	Pre	Post	Pre	Post	Pre	Post	
f(CKO)	136.07	134.30	134.05	132.25	134.71	133.05	135.99	133.70	MHz
f(VCO)	1088.56	1074.40	1072.40	1058.00	1077.68	1064.40	1087.60	1072.00	MHz
Parameter	**TB-AD05**		**TB-AD06**		**TB-AD07**		**TB-AD08**		**Unit**
	Pre	Post	Pre	Post	Pre	Post	Pre	Post	
f(CKO)	135.95	134.00	133.32	131.50	133.23	131.05	132.83	130.90	MHz
f(VCO)	1087.60	1072.00	1066.56	1052.00	1065.84	1048.40	1062.64	1047.20	MHz
Parameter	**TB-AD09**		**TB-AD10**		**TB-AD11**		**TB-AD12**		**Unit**
	Pre	Post	Pre	Post	Pre	Post	Pre	Post	
f(CKO)	132.50	130.80	134.65	132.70	134.62	132.80	135.25	134.35	MHz
f(VCO)	1060.00	1046.40	1077.20	1061.60	1076.96	1062.40	1082.00	1074.80	MHz

Table 15: Maximum free running VCO frequency for TB-AD01 to TB-AD12.

7.1.6 Band-Gap Reference – DAC Full-Scale

The output of the band-gap reference is an internal node of the SY1017AS chip and is not accessible to the outside. Although the band-gap reference is not directly accessible, it can still be accessed indirectly through the DA-converter's output.

The DA-converter is programmed to 0x00, which gives the full-scale output voltage (ideally 2.092V). The test is done with AVDD = 3.0V. Table 16 shows the measured values.

DUT	DAC Voltage		DUT	DAC Voltage		DUT	DAC Voltage		Unit
	Pre	Post		Pre	Post		Pre	Post	
TB-AD01	2091	2093	TB-AD05	2088	2090	TB-AD09	2075	2075	mV
TB-AD02	2083	2080	TB-AD06	2089	2084	TB-AD10	2068	2070	mV
TB-AD03	2098	2099	TB-AD07	2084	2082	TB-AD11	2079	2083	mV
TB-AD04	2074	2074	TB-AD08	2065	2067	TB-AD12	2072	2077	mV

Table 16: DAC output voltage at full scale for TB-AD01 to TB-AD12.

- **Test Results:** All SY1017AS DUTs operate properly with no significant parametric drifts before and after irradiation. The minor deviations seen in the various measurements are due to either normal measurement uncertainty or temperature effects rather than absorbed dose.

  These devices have therefore demonstrated *no sensitivity* to irradiation up to **2000Gy(Si)**.

7.2 Tests During Irradiation

The SY1017AS DUTs have been tested up to a TID = 2kGy(Si) in 2 separate runs of 1kGy(Si) each, one at high dose rate and one at low dose rate to test ELDRS effects. The conditions for these tests are shown in Table 1, while the details of the tests are shown in Tables 2 and 3 (Section 5).

7.2.1 Irradiation Test Execution

The SY1017AS DUT needs to be powered up, then initialized. Once the SY1017AS is ready, irradiation is started and measurements are made for the whole irradiation time. This is described in Table 17, where 'S' means a set-up and 'M' means a measurement to be performed.

	Description	Expected value
S	Set power supply to 3.0V	
S	Set clock frequency to 4MHz.	
S	Load value 230 into PLL register (power modes active and PLL divider set to 25).	
S	Load value 127 into ADC register.	
M	Measure current consumption	I(AVDD) $<$ 13mA
M	Measure current consumption	I(DVDD) $<$ 10mA
M	Measure PLL output	between 1.4-1.7V
M	Measure DAC output	between 1.0-1.1V

Table 17: Set-up of the SY1017AS for the irradiation tests.

7.2.2 Data Logged During Irradiation

During the irradiation period data is logged. Several parameters have been selected as event indicators, these are shown in Table 18 and comprise both analog parameters and DUT register status. Data is logged once per second.

Register	Measurement or Setting
SM314 Registers	
ANALOG_OUT1_CURRENT	IDVDD [μA]
ANALOG_OUT1_VOLTAGE	DVDD [mV]
ANALOG_OUT2_CURRENT	IAVDD [μA]
ANALOG_OUT2_VOLTAGE	AVDD [mV]
ANALOG_IN1_AD_VALUE	DAC Voltage [mV]
ANALOG_IN2_AD_VALUE	PLL Voltage [mV]
SY1017AS Registers	
PLL and Power Modes	PM&PLL = 230
AGC DA-converter	AGC-DAC = 127

Table 18: Data logged for SY1017AS DUTs during irradiation.

These parameters were selected because they tend to be the most sensitive parameters against irradiation. In particular the band-gap reference, which uses bipolar transistors in a circuit with relatively high gain and is used as voltage reference for the DA-converter and to bias all circuits in the DUTs, is a sensitive indicator of degradation, especially ELDRS if present. A drift would be reflected on the performances of the whole DUT.

7.2.3 Parametric Drifts

The purpose of these tests is to find any parametric drifts that may occur under irradiation. These are DC measurements and were made according to the conditions given in Table 17. The following parameters were measured and logged (Table 18):

- **SY1017AS:** I(AVDD), I(DVDD), DAC Voltage, PLL Voltage.

The following traces show the measured parameters over the 0Gy to 2.2kGy(Si) irradiation range.

I(AVDD): Figures 45 and 46 show AVDD current consumption for the SY1017AS devices TB-AD01 to TB-AD06.

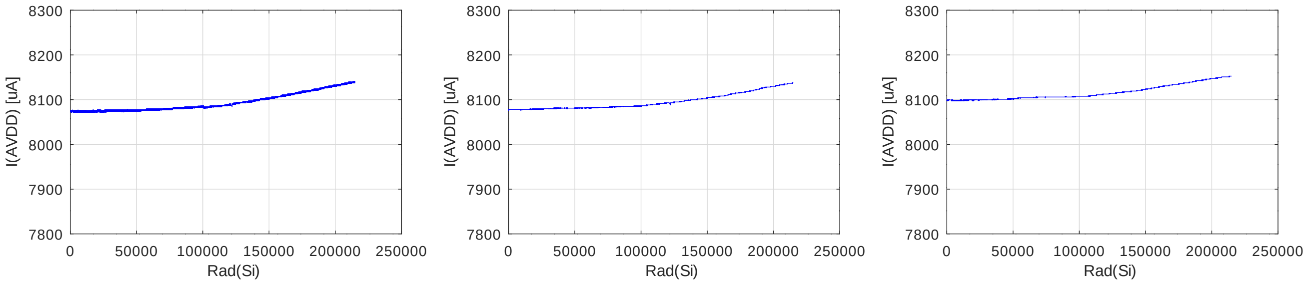


Figure 45: AVDD current consumption during irradiation: TB-AD01 (l), TB-AD02 (c) and TB-AD03 (r).

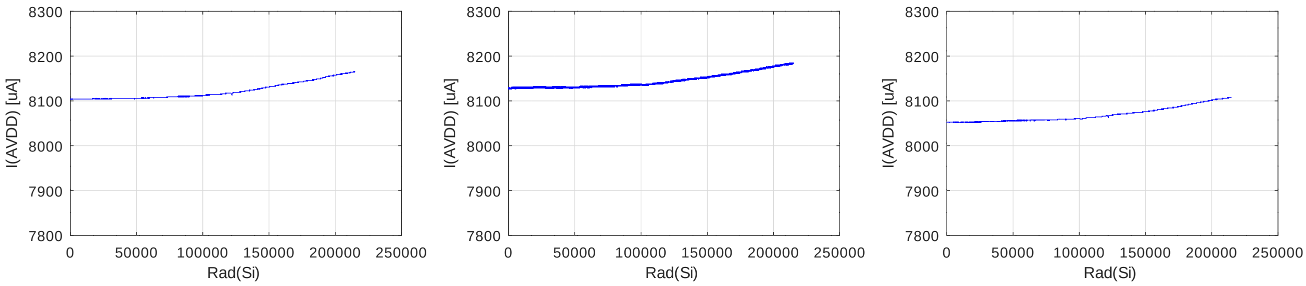


Figure 46: AVDD current consumption during irradiation: TB-AD04 (l), TB-AD05 (c) and TB-AD06 (r).

AVDD current consumption remains *substantially constant* over the first 1kGy(Si) irradiation session, then it shows a *slight increase* until radiation is stopped. The I(AVDD) current measurements show quantization some noise due to the 1.67μA resolution of the AD-converters of the SM314 boards.

I(DVDD): Figures 47 and 48 show DVDD current consumption for the SY1017AS devices TB-AD01 to TB-AD06.

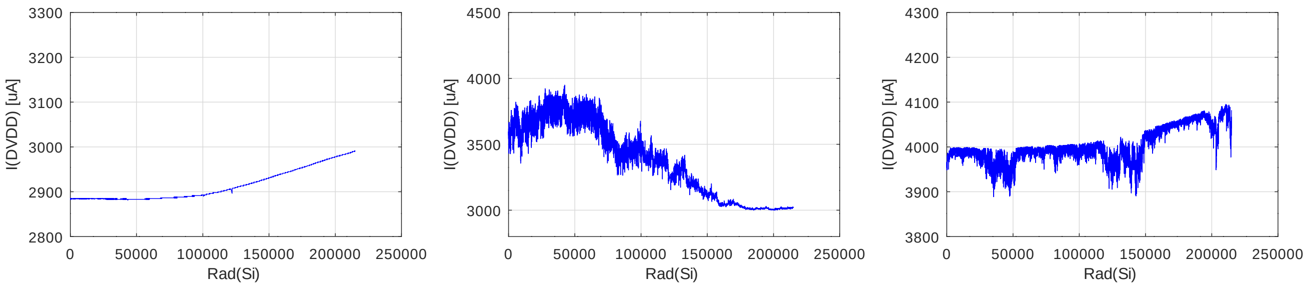


Figure 47: DVDD current consumption during irradiation: TB-AD01 (l), TB-AD02 (c) and TB-AD03 (r).

DVDD current consumption remains *substantially constant* over the first 1kGy(Si) irradiation session, then *increases linearly* until radiation is stopped. DUTs TB-AD02, TB-AD03, and TB-AD04 shows jumps and noise

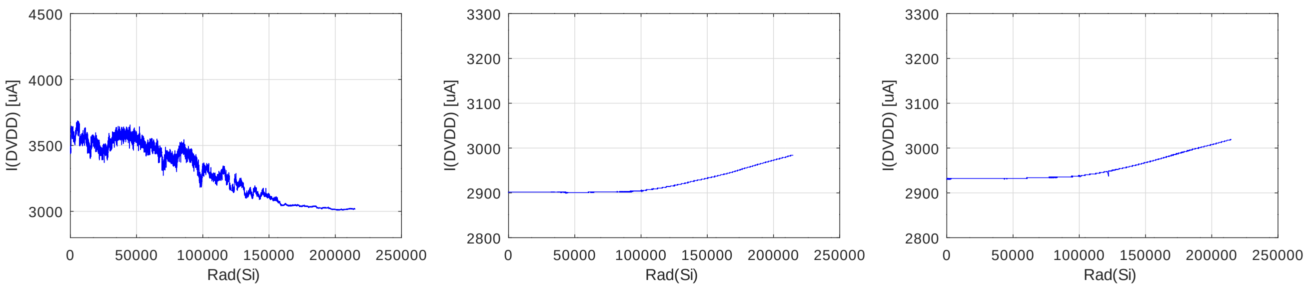


Figure 48: DVDD current consumption during irradiation: TB-AD04 (l), TB-AD05 (c) and TB-AD06 (r).

due to the changing activity of the AD-converter's outputs. This is an expected behaviour, given that the inputs of the AD-converters are left floating and thus unpredictable activity of the digital port will result. Such effect is also visible in the I(DVDD) measurements shown in Table 14.

DAC Voltage: Figures 49 and 50 show the output voltage of the AGC DA-converter (pin AGCO) for the SY1017AS devices TB-AD01 to TB-AD06.

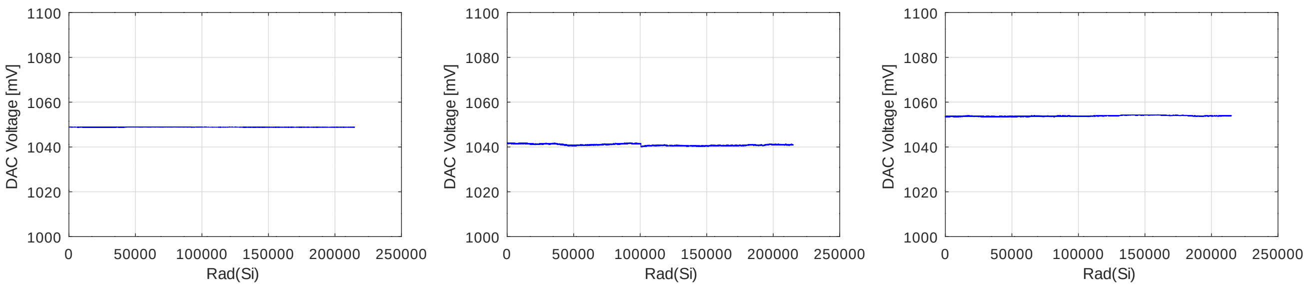


Figure 49: DAC output voltage during irradiation: TB-AD01 (l), TB-AD02 (c) and TB-AD03 (r).

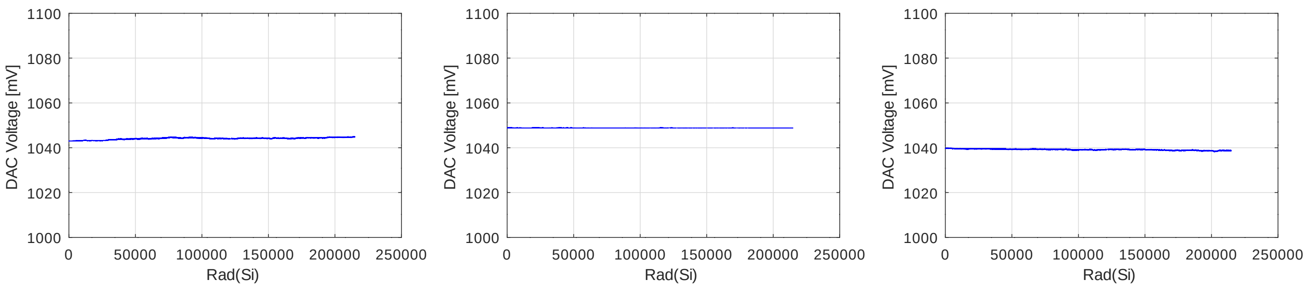


Figure 50: DAC output voltage during irradiation: TB-AD04 (l), TB-AD05 (c) and TB-AD06 (r).

The DAC voltage is *essentially constant* for all DUTs over the whole irradiation range, which indicates *no sensitivity* to irradiation of both the DA-converter and the band-gap reference.

PLL Voltage: Figures 51 and 52 show the PLL control voltage for the SY1017AS devices TB-AD01 to TB-AD06.

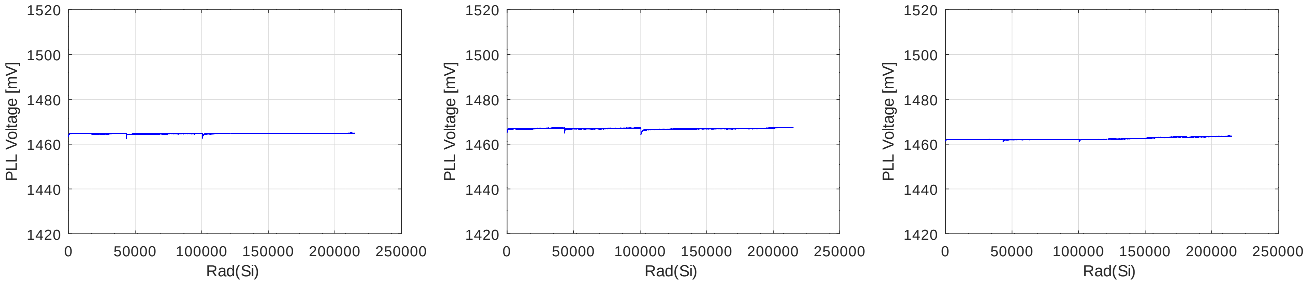


Figure 51: PLL voltage during irradiation: TB-AD01 (l), TB-AD02 (c) and TB-AD03 (r).

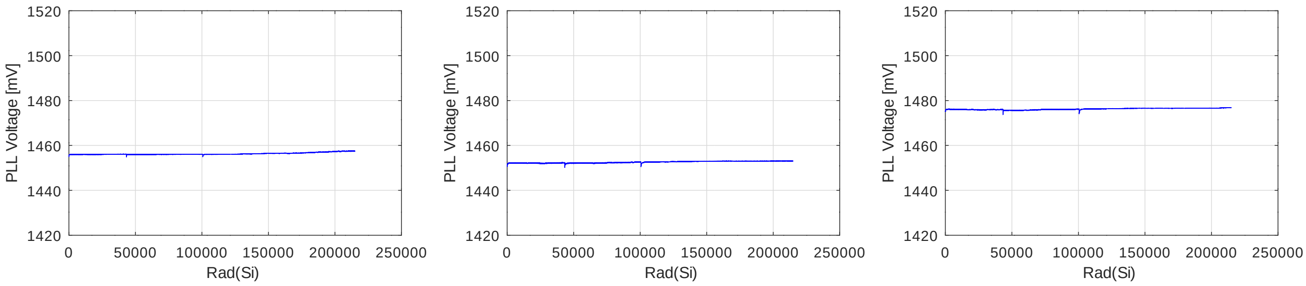


Figure 52: PLL voltage during irradiation: TB-AD04 (l), TB-AD05 (c) and TB-AD06 (r).

The minor variations over time of the PLL control voltage are most likely due to temperature effects rather than irradiation.

- **Test Results:** All SY1017AS DUTs operate properly with no significant parametric drifts during irradiation, the monitored parameters are stable, except for the supply currents that show some increase above 1kGy(Si). The minor deviations seen in the various measurements are due to either normal measurement uncertainty or temperature effects rather than absorbed dose. Variations and noise on the I(DVDD) measurement are due to the changing activity of the AD-converter's outputs.

  These devices have therefore demonstrated *no sensitivity* to irradiation up to **1000Gy(Si)** and remained operative up to **2000Gy(Si)**, although some increase in supply currents has been found.

8 Conclusions

The TID tests up to a total dose of 2000Gy(Si) in 2 sessions of 1000Gy(Si) each were conducted on the SY1007A and SY1017A devices at the ESTEC Co-60 irradiation laboratory to evaluate their sensitivity to radiation. Since the DUTs use bipolar transistors in their design, ELDRS has been also evaluated. The tests gave the following results:

- The SY1007A and SY1017A DUTs remained operational and showed *no failure or damage* due to irradiation up to a total radiation exposure up to 2000Gy(Si).
- *No significant drift* of the measured parameters could be ascertained for both devices due to irradiation.
- *Some increase of supply current* has been noticed for exposures above 1000Gy(Si). Such increase however resulted in *no failures* and *no parametric deviations*. The DUTs remained fully functional and showed no degradation of performances.
- *No ELDRS effects* were found up to a low dose rate exposure of 1000Gy(Si).

The pre-irradiation and post-irradiation tests gave basically identical results for both the SY1007A and the SY1017A DUTs. The variations detected are caused by normal measurement tolerances, quantization effects or temperature differences, not by drifts of the DUTs.

This test session therefore has demonstrated that both SY1007A and SY1017A DUTs have *no sensitivity* to irradiation up to at least **1000Gy(Si)** at low dose rate and **2000Gy(Si)** in total, if the increase in supply current is accepted.

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